

MOSFET - Power, Single N-Channel, DUAL COOL[®], DFN8 5x6

40 V, 0.40 mΩ, 540 A

NTMF5CH0D4N04XM

Features

- Advanced Dual-Side Cool Package with Enhanced Heat Dissipation Molding Compound
- Soft Recovery Body Diode
- Ultra Low $R_{DS(on)}$ Optimization to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free, BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Management System Protection
- ORing

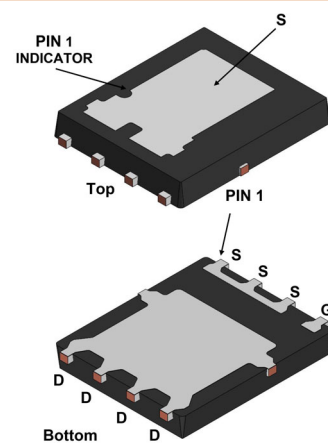
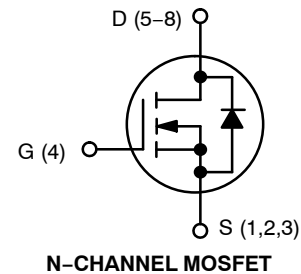
MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	540
	$T_C = 100\text{ }^{\circ}\text{C}$		382
Power Dissipation (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	208
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	1664
Pulsed Source Current (Body Diode)		I_{SM}	1664
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	234
Single Pulse Avalanche Energy ($I_{PK} = 116\text{ A}$)	E_{AS}	807	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^{\circ}\text{C}$

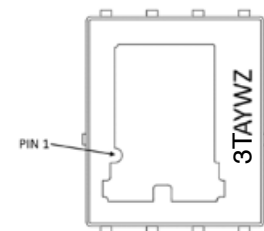
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal and electromechanical application board design.
- EAS of 807 mJ is based on started $T_J = 25\text{ }^{\circ}\text{C}$, $I_{AS} = 116\text{ A}$, $V_{DD} = 32\text{ V}$, $V_{GS} = 10\text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.40 mΩ @ 10 V	540 A



MARKING DIAGRAM



- 3T = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.78	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, ref to $25\text{ }^{\circ}\text{C}$		8.8		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 25\text{ }^{\circ}\text{C}$			10	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		0.31	0.40	m Ω
		$V_{GS} = 7\text{ V}, I_D = 30\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		0.42	0.62	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 350\text{ }\mu\text{A}, T_J = 25\text{ }^{\circ}\text{C}$	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 350\text{ }\mu\text{A}$		-7.3		mV/ $^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 30\text{ A}$		191		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		9126		pF
Output Capacitance	C_{OSS}			6475		
Reverse Transfer Capacitance	C_{RSS}			131		
Output Charge	Q_{OSS}			195		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 7\text{ V}, V_{DD} = 20\text{ V}, I_D = 30\text{ A}$		110		nC
		$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}, I_D = 30\text{ A}$		151		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}, I_D = 30\text{ A}$		29		
Gate-to-Source Charge	Q_{GS}			47		
Gate-to-Drain Charge	Q_{GD}			33		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.36		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 20\text{ V},$ $I_D = 30\text{ A}, R_G = 2.5\text{ }\Omega$		40		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			67		
Fall Time	t_f			15		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		0.77	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 30\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		0.61		

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $di/dt = 100\text{ A}/\mu\text{s}$, $I_S = 30\text{ A}$, $V_{DD} = 20\text{ V}$		108		ns
Charge Time	t_a			57		
Discharge Time	t_b			52		
Reverse Recovery Charge	Q_{RR}			214		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

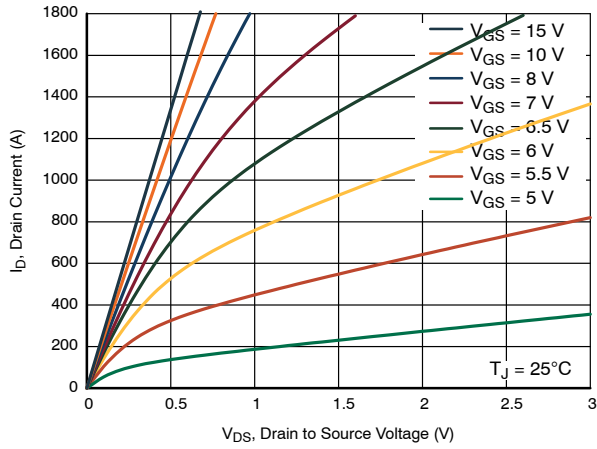


Figure 1. On-Region Characteristics

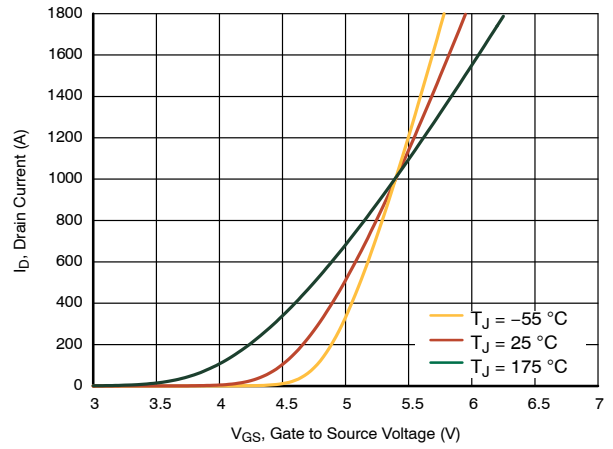


Figure 2. Transfer Characteristics

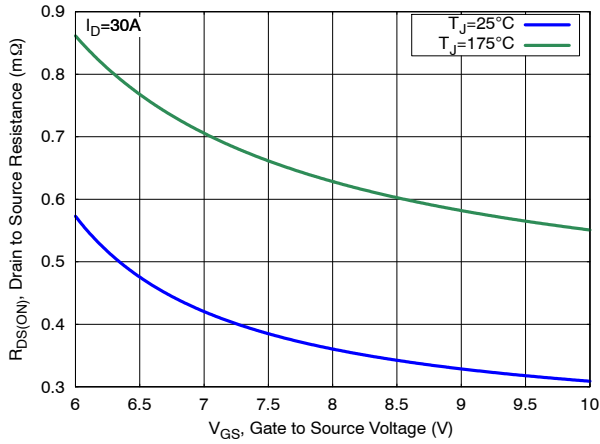


Figure 3. On-Resistance vs. Gate Voltage

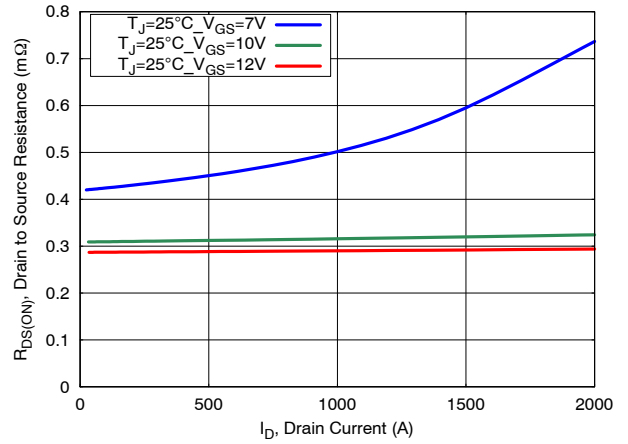


Figure 4. On-Resistance vs. Drain Current

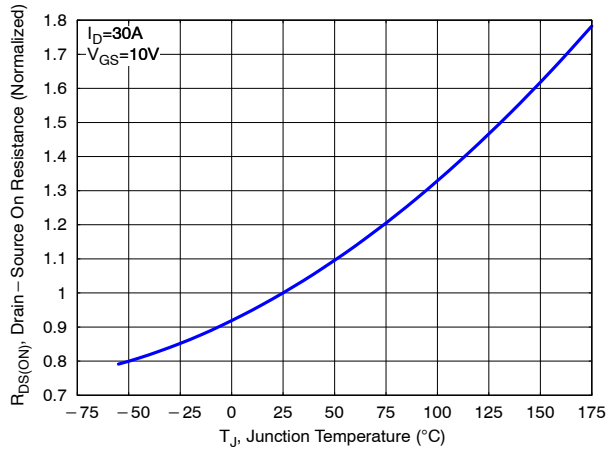


Figure 5. Normalized ON Resistance vs. Junction Temperature

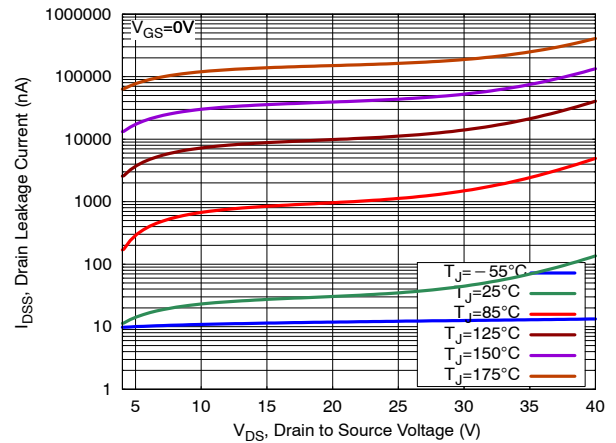


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

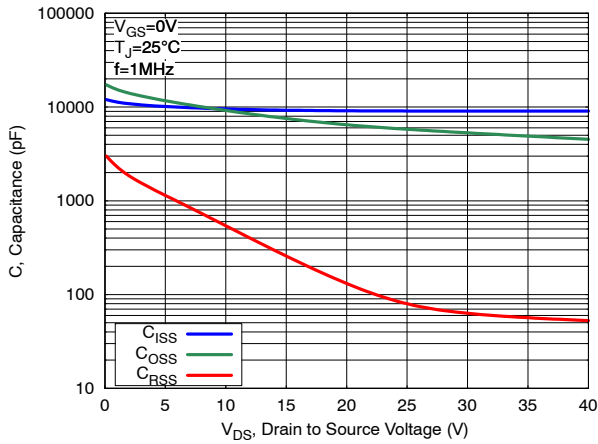


Figure 7. Capacitance Characteristics

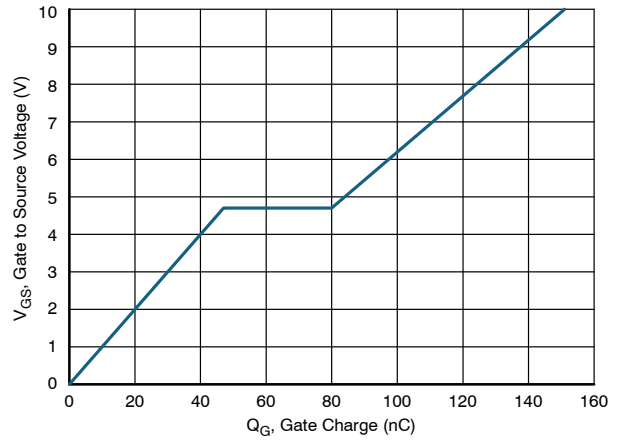


Figure 8. Gate Charge Characteristics

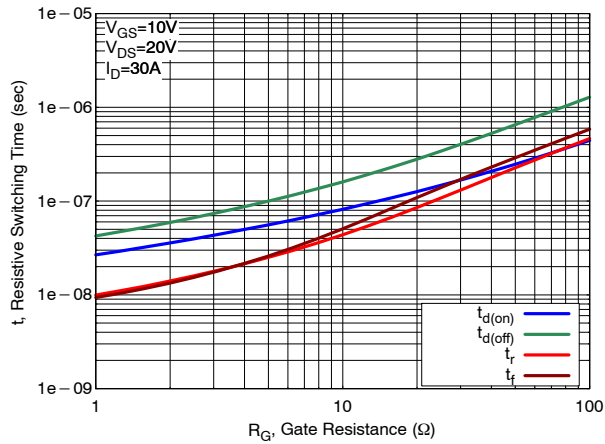


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

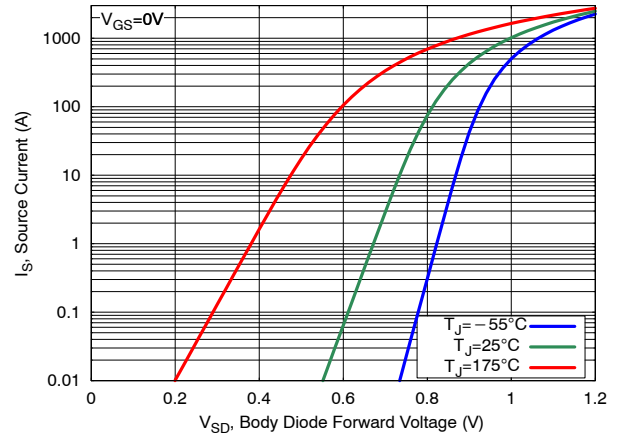


Figure 10. Diode Forward Characteristics

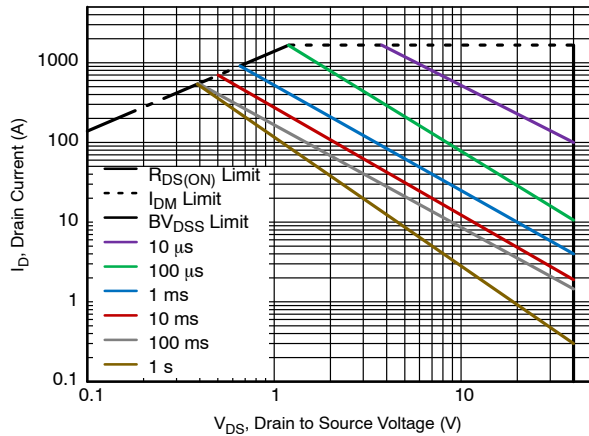


Figure 11. Safe Operating Area (SOA)

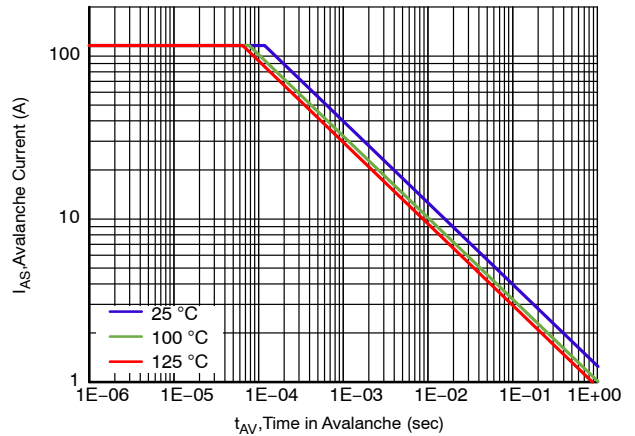


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

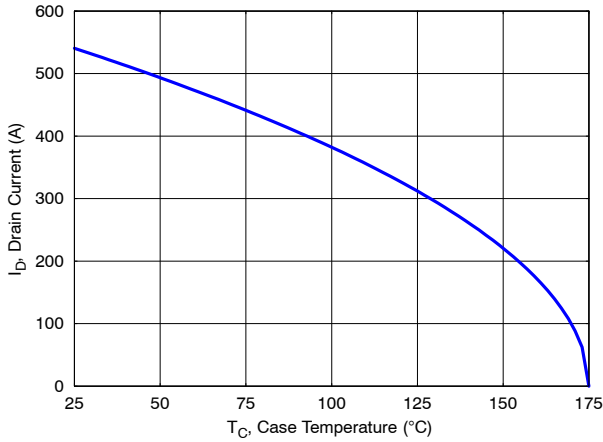


Figure 13. Maximum Current vs. Case Temperature

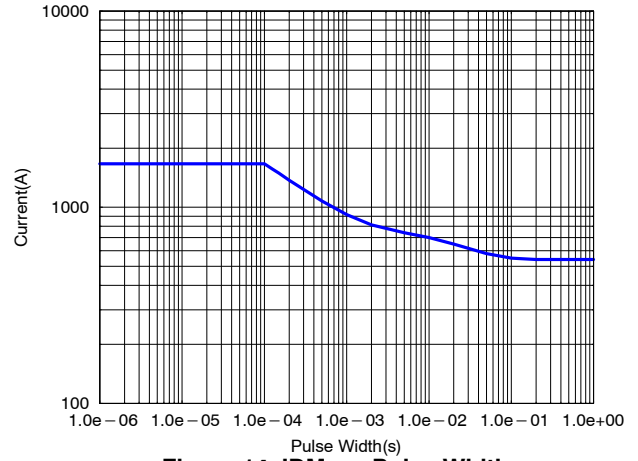


Figure 14. IDM vs. Pulse Width

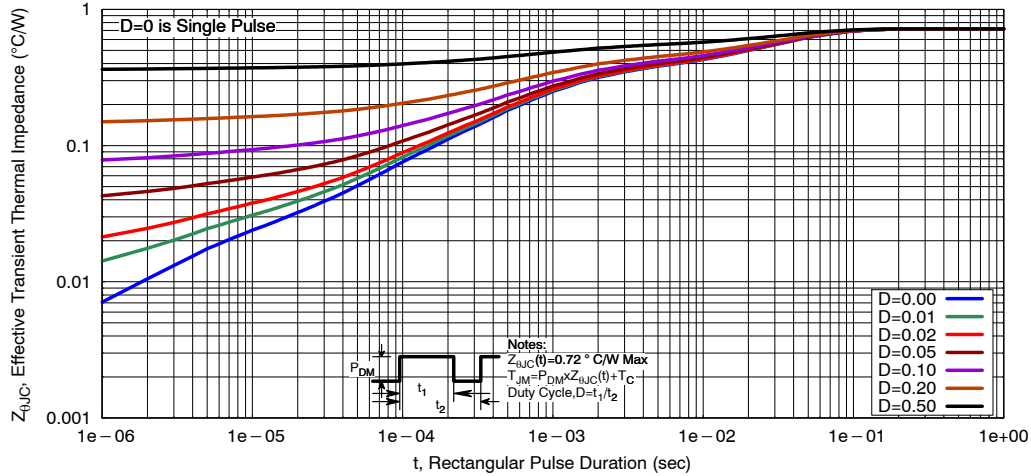


Figure 15. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCH0D4N04XMTWG	3T	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

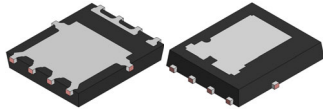
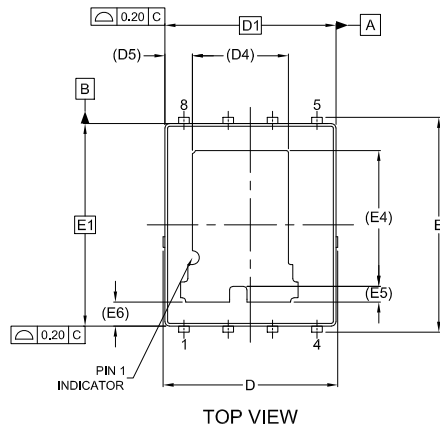
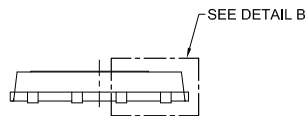
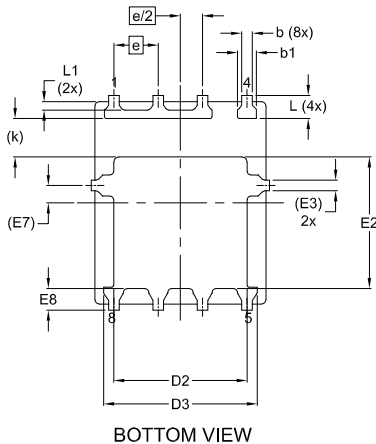
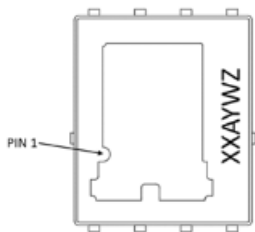
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REVISION HISTORY

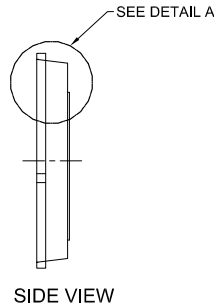
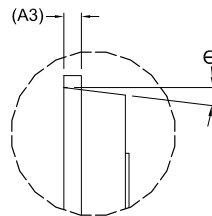
Revision	Description of Changes	Date
1	Final version release.	08/18/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


DFN8 4.90x5.80x0.90, 1.27P
CASE 506FF
ISSUE D
DATE 21 MAR 2025

TOP VIEW

FRONT VIEW

BOTTOM VIEW
GENERIC MARKING DIAGRAM*


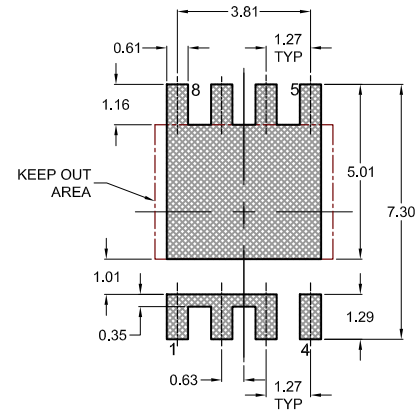
XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.


SIDE VIEW

DETAIL A
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.30 REF		
E4	3.89 REF		
E5	0.45 REF		
E6	0.69 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	--	7°

DOCUMENT NUMBER: 98AON54466H

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DESCRIPTION: DFN8 4.90x5.80x0.90, 1.27P

PAGE 1 OF 1

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