

# MOSFET - Power, Single N-Channel, STD Gate, DUAL COOL® DFN8 5x6 80 V, 2.6 mΩ, 154 A

## NTMFSC2D6N08X

### Features

- Advanced Dual-Sided Cooled Packaging
- Low  $Q_{RR}$ , Soft Recovery Body Diode
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives

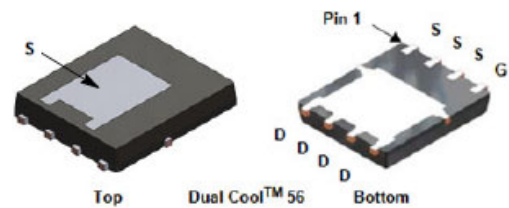
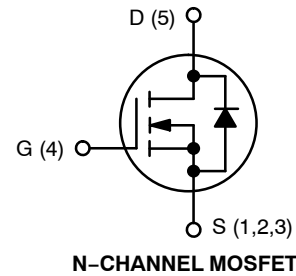
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	80	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	154
		$T_C = 100^\circ\text{C}$	109
Power Dissipation (Note 1)	$T_C = 25^\circ\text{C}$	$P_D$	133
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 100 \mu\text{s}$	$I_{DM}$	634
Pulsed Source Current (Body Diode)		$I_{SM}$	634
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	201	A
Single Pulse Avalanche Energy ( $I_{PK} = 53 \text{ A}$ ) (Note 3)	$E_{AS}$	140	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

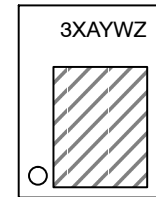
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3.  $E_{AS}$  of 140 mJ is based on started  $T_J = 25^\circ\text{C}$ ,  $I_{AS} = 53 \text{ A}$ ,  $V_{DD} = 64 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ , 100% avalanche tested

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	2.6 mΩ @ 10 V	154 A



DFN8 5x6.15  
CASE 506EG

### MARKING DIAGRAM



- 3X = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NTMFSC2D6N08X

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Bottom	$R_{\theta JC}$	1.12	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case, Top	$R_{\theta JC}$	1.7	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	$^{\circ}\text{C}/\text{W}$

4. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad, 1 oz. Cu.
5.  $R_{\theta JA}$  is determined by the user's board design.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$ . Referenced to $25^{\circ}\text{C}$		31.6		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, T_J = 25^{\circ}\text{C}$			10	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, T_J = 125^{\circ}\text{C}$			250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 37\text{ A}$		2.2	2.6	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 18\text{ A}$		3.3	5.2	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 184\ \mu\text{A}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 184\ \mu\text{A}$		-7.5		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 37\text{ A}$		115		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		3200		$\mu\text{F}$	
Output Capacitance	$C_{OSS}$			930			
Reverse Transfer Capacitance	$C_{RSS}$			14			
Output Charge	$Q_{OSS}$	$V_{GS} = 6\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		66		nC	
Total Gate Charge	$Q_{G(TOT)}$			28			
Threshold Gate Charge	$Q_{G(TH)}$			45			
Gate-to-Source Charge	$Q_{GS}$		$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		10		
Gate-to-Drain Charge	$Q_{GD}$				15		
Gate Plateau Voltage	$V_{GP}$			7			
Gate Resistance	$R_G$	$f = 1\text{ MHz}$		4.7		V	
				0.8		$\Omega$	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 37\text{ A}, R_G = 2.5\ \Omega$		24		ns
Rise Time	$t_r$			8		
Turn-Off Delay Time	$t_{d(OFF)}$			35		
Fall Time	$t_f$			6		

# NTMFSC2D6N08X

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SOURCE-TO-DRAIN DIODE CHARACTERISTICS</b>						
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 25^\circ\text{C}$		0.82	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 1000\text{ A}/\mu\text{s},$ $I_S = 37\text{ A}, V_{DD} = 40\text{ V}$		23		ns
Charge Time	$t_a$			13		
Discharge Time	$t_b$			11		
Reverse Recovery Charge	$Q_{RR}$			163		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NTMFSC2D6N08X

## TYPICAL CHARACTERISTICS

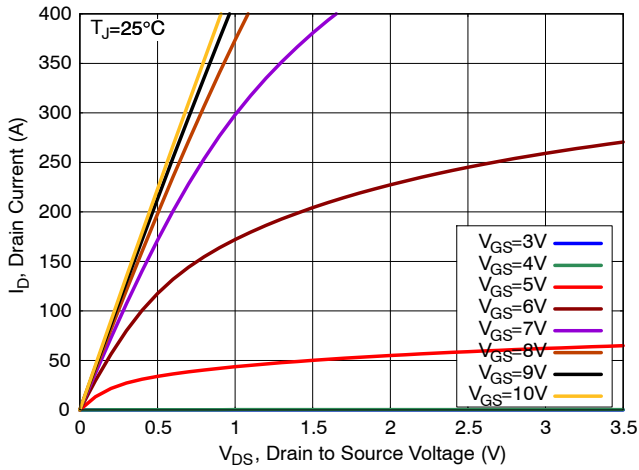


Figure 1. On-Region Characteristics

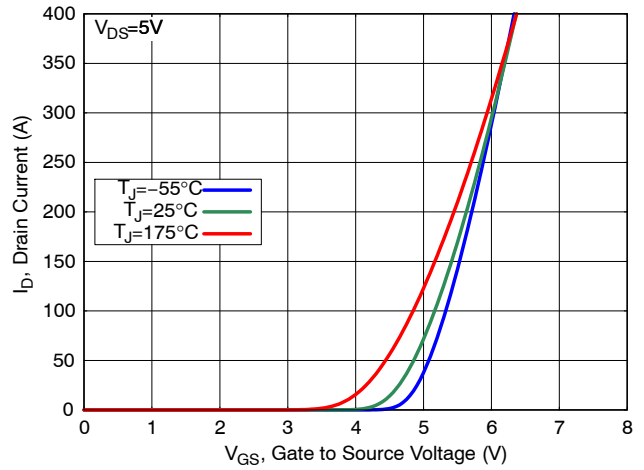


Figure 2. Transfer Characteristics

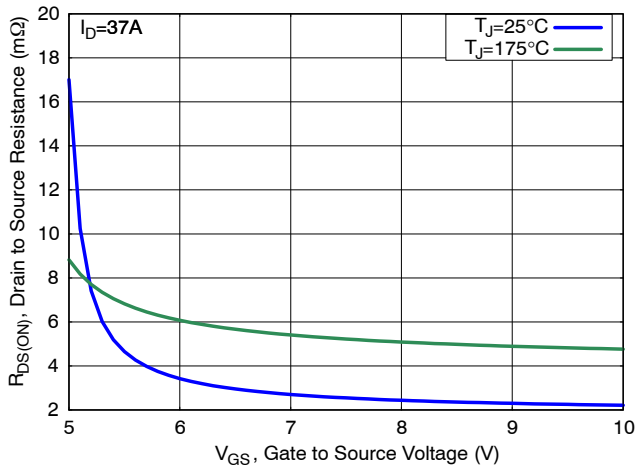


Figure 3. On-Resistance vs. Gate Voltage

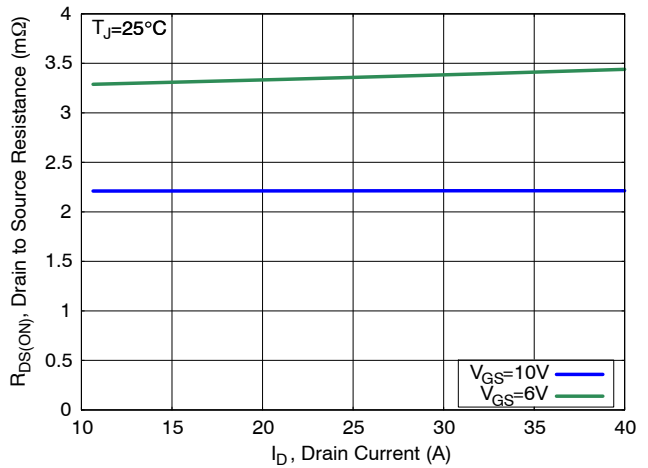


Figure 4. On-Resistance vs. Drain Current

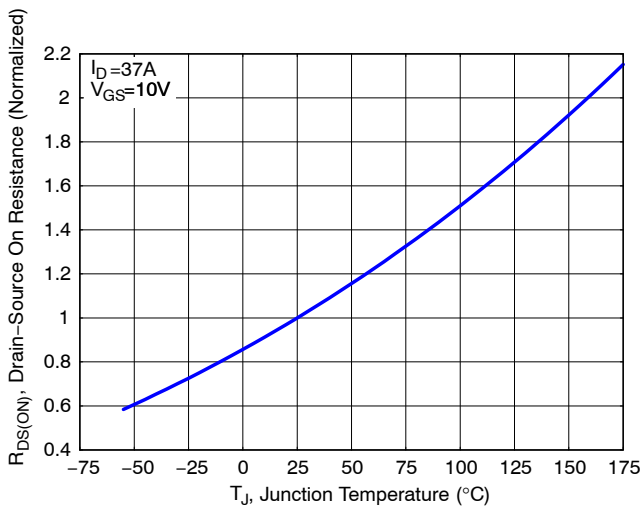


Figure 5. Normalized ON Resistance vs. Junction Temperature

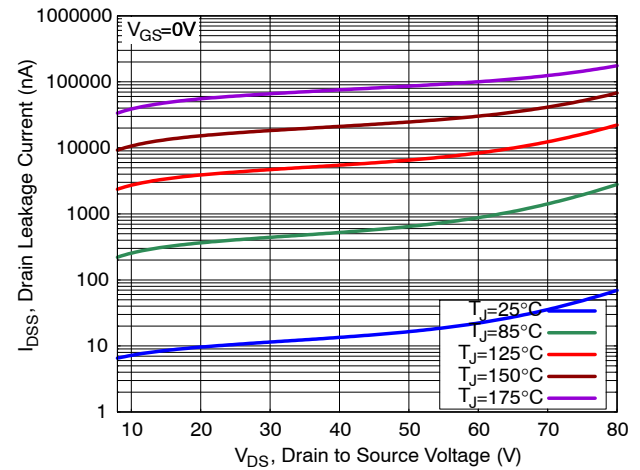


Figure 6. Drain Leakage Current vs. Drain Voltage

# NTMFSC2D6N08X

## TYPICAL CHARACTERISTICS

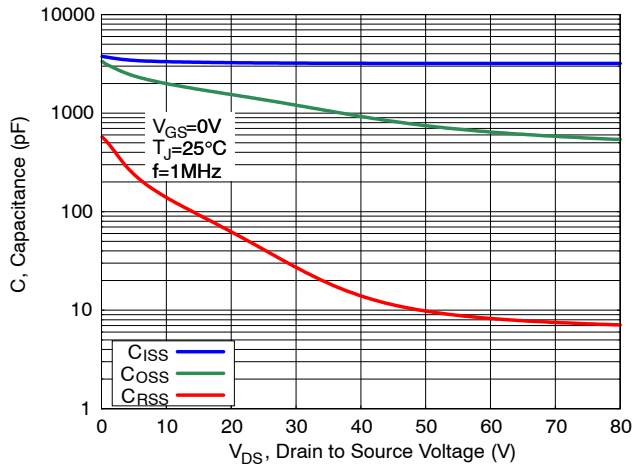


Figure 7. Capacitance Characteristics

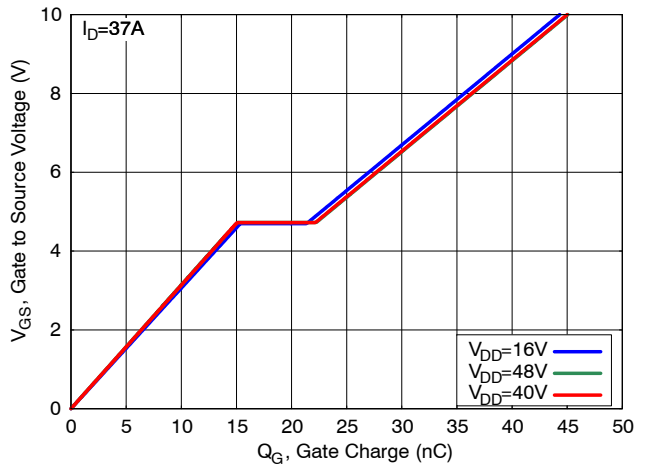


Figure 8. Gate Charge Characteristics

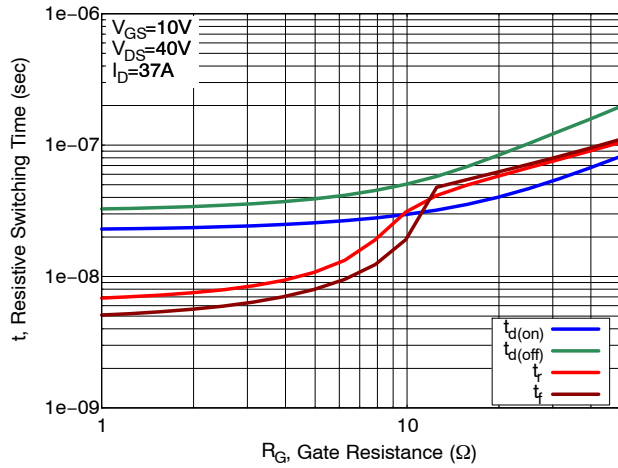


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

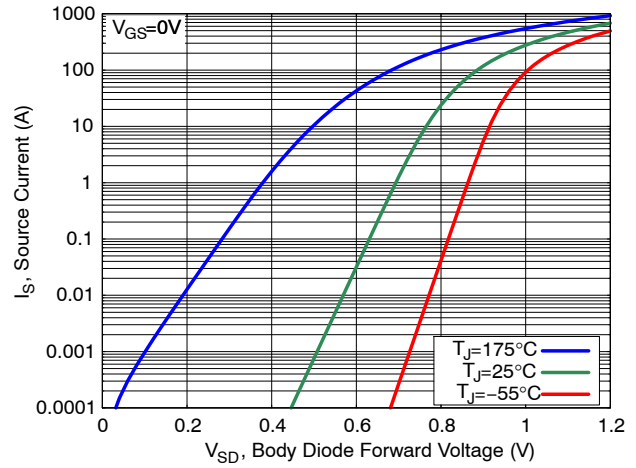


Figure 10. Diode Forward Characteristics

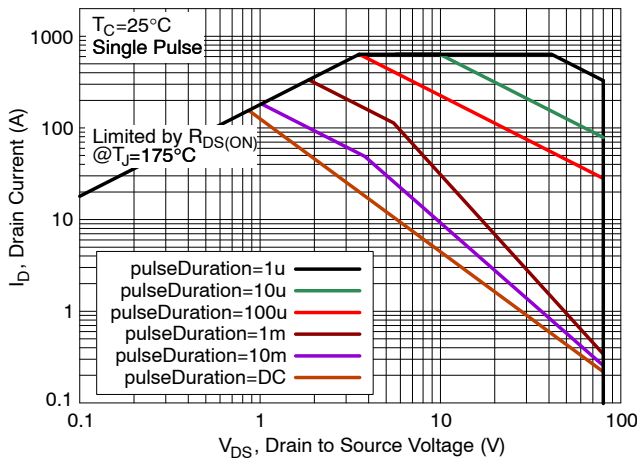


Figure 11. Safe Operating Area (SOA)

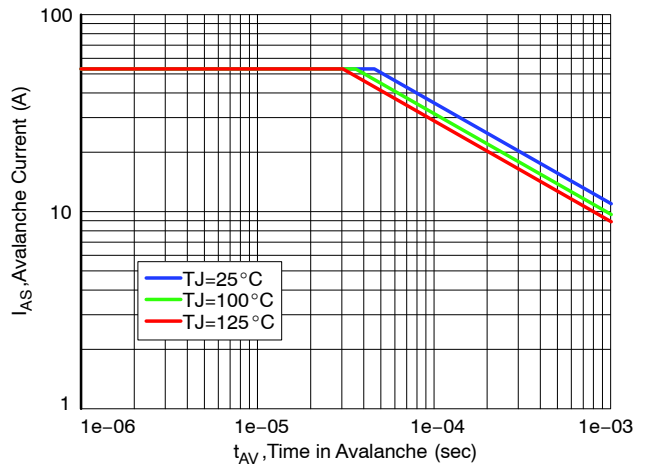
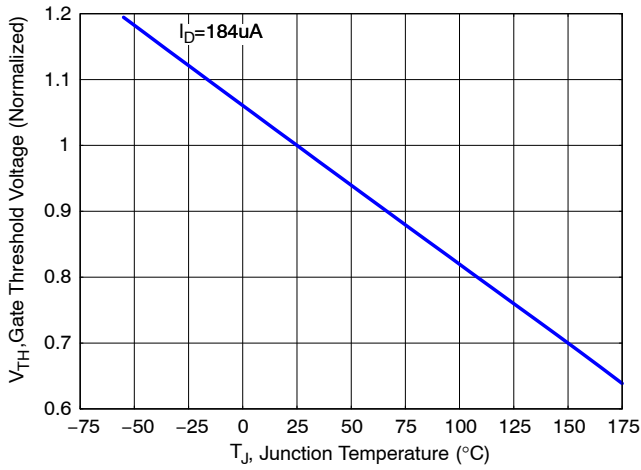


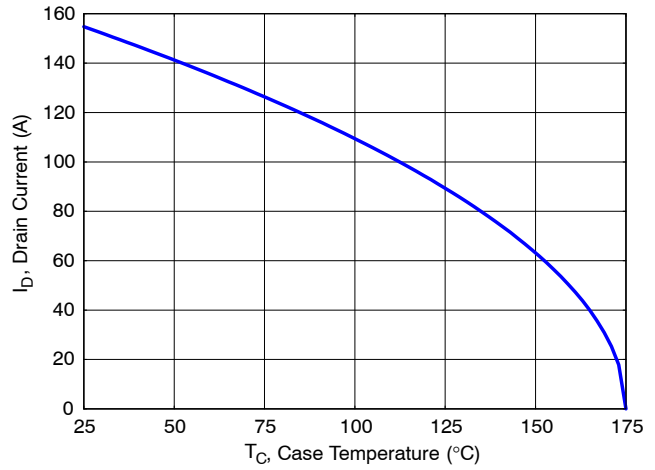
Figure 12. Avalanche Current vs. Pulse Time (UIS)

# NTMFSC2D6N08X

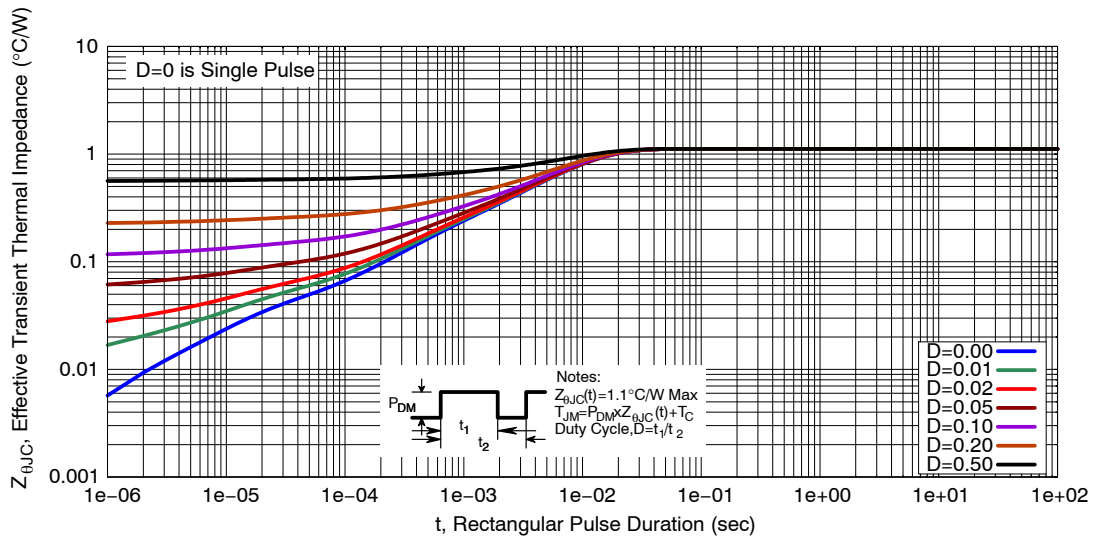
## TYPICAL CHARACTERISTICS



**Figure 13. Gate Threshold Voltage vs. Junction Temperature**



**Figure 14. Maximum Current vs. Case Temperature**



**Figure 15. Transient Thermal Response**

### ORDERING INFORMATION

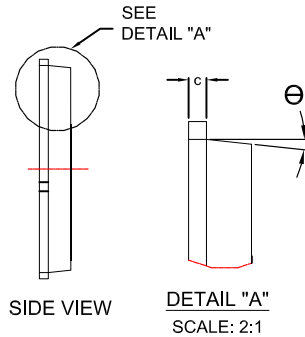
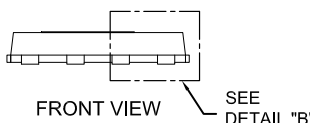
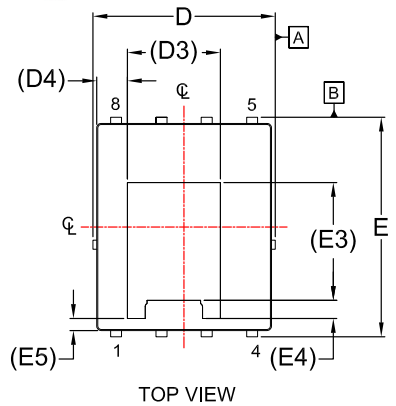
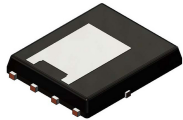
Device Order Number	Device Marking	Package Type	Shipping†
NTMFSC2D6N08XTWG	3X	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

DUAL COOL are registered trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

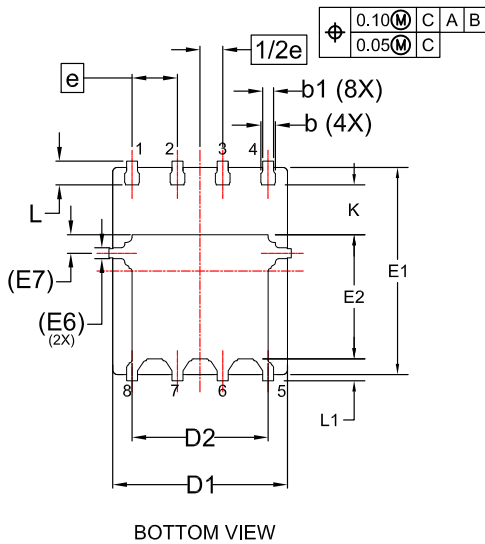
DFN8 5x6.15, 1.27P, DUAL COOL  
CASE 506EG  
ISSUE D

DATE 25 AUG 2020

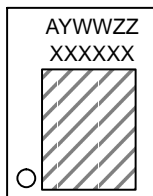


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

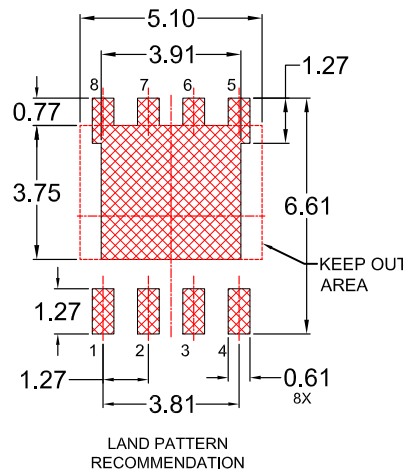
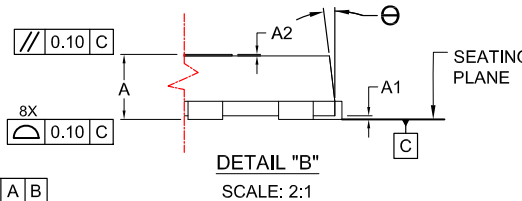


GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

DOCUMENT NUMBER:	98AON84257G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8 5x6.15, 1.27P, DUAL COOL	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)