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MOSFET - N-Channel Shielded Gate PowerTrench®

150 V, 7.9 mΩ, 95.6 A

NTMFS7D5N15MC

ON Semiconductor®

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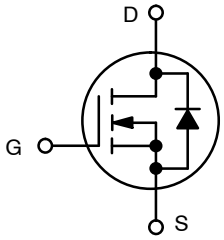
Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- 100% UIL Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

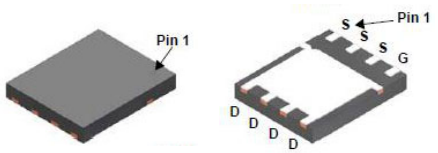
Typical Applications

- Synchronous Rectification
- AC−DC and DC−DC Power Supplies
- AC−DC Adapters (USB PD) SR
- Load Switch

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	7.9 mΩ @ 10 V	95.6 A



N−CHANNEL MOSFET



Top Bottom

PQFN8 5x6
CASE 483AF

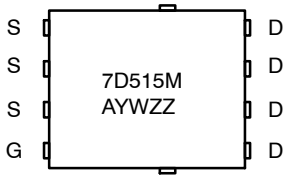
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	150	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	95.6	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	166.7	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	13.5	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.3	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs		I_{DM}	478	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy (I_L = 18 A_{pk}, L = 3 mH)			E_{AS}	486	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM



7D515M = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS7D5N15MC (Pb−Free/Halogen Free)	Power 56 (PQFN8)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Notes 1, 2)	$R_{\theta JA}$	45	

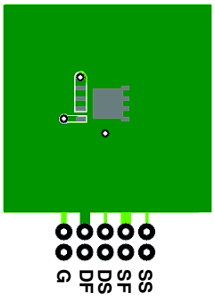
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	150			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C		83		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V, T_J = 25°C			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 295 μA	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 295 μA, ref to 25°C		−8.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 54 A		6.4	7.9	mΩ
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 8 V, I_D = 27 A		6.9	9.2	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 54 A		91		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 75 V		3835		pF
Output Capacitance	C_{OSS}			1070		
Reverse Transfer Capacitance	C_{RSS}			11		
Gate−Resistance	R_G			0.6	1.2	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 75 V; I_D = 54 A		46		nC
Threshold Gate Charge	$Q_{G(TH)}$			12		
Gate−to−Source Charge	Q_{GS}			20		
Gate−to−Drain Charge	Q_{GD}			7		
Plateau Voltage	V_{GP}			6		V
Output Charge	Q_{OSS}	V_{DD} = 75 V, V_{GS} = 0 V		116		nC
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 75 V, I_D = 54 A, R_G = 6 Ω		27		ns
Rise Time	t_r			6		
Turn−Off Delay Time	$t_{d(OFF)}$			32		
Fall Time	t_f			5		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 54 A, T_J = 25°C		0.87	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V, dI_S/dt = 100 A/μs, I_S = 54 A		59		ns
Reverse Recovery Charge	Q_{RR}			111		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V, dI_S/dt = 1000 A/μs, I_S = 54 A		44		ns
Reverse Recovery Charge	Q_{RR}			616		nC

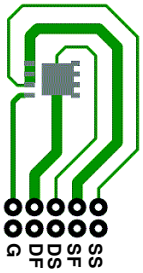
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

3. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 115°C/W when mounted on a minimum pad of 2 oz copper.

TYPICAL CHARACTERISTICS

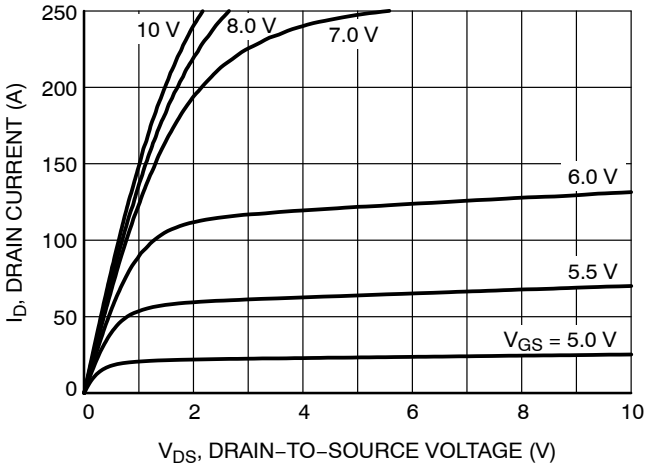


Figure 1. On−Region Characteristics

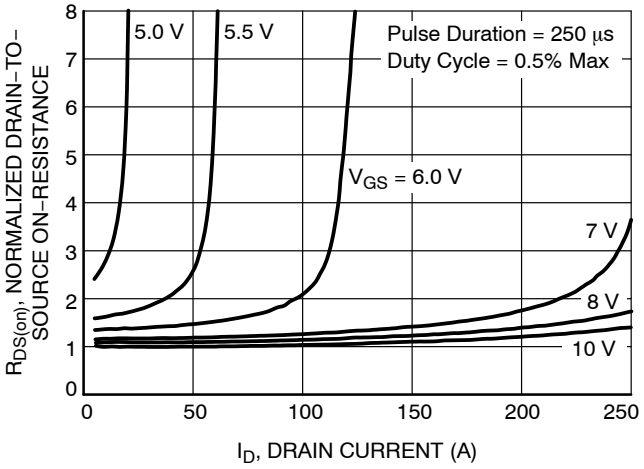


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

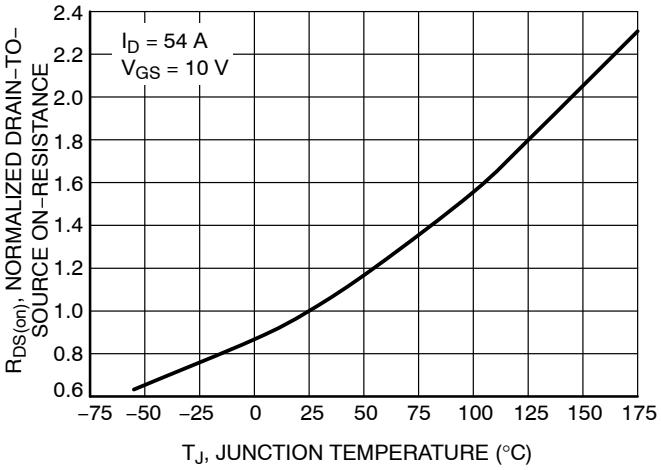


Figure 3. Normalized On−Resistance vs. Junction Temperature

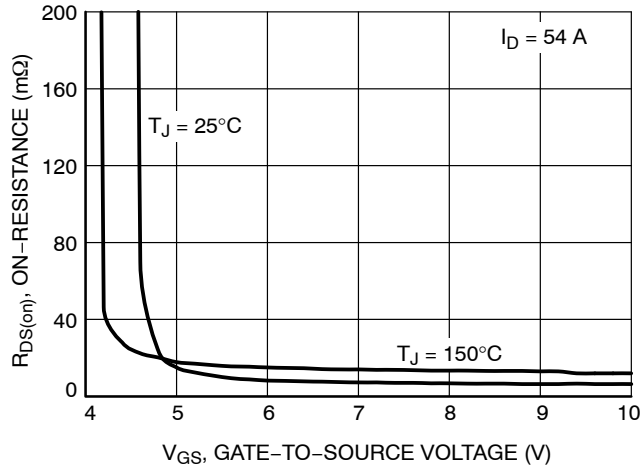


Figure 4. On−Resistance vs. Gate−to−Source Voltage

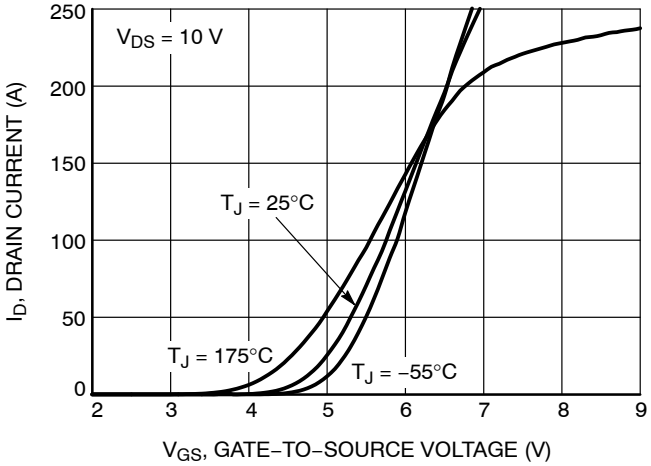


Figure 5. Transfer Characteristics

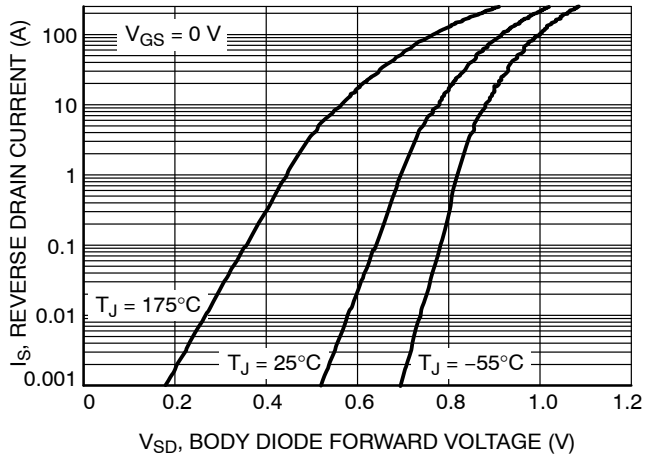


Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

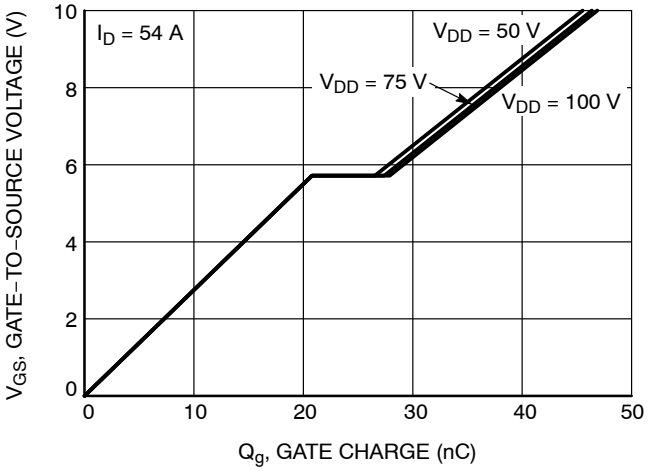


Figure 7. Gate Charge Characteristics

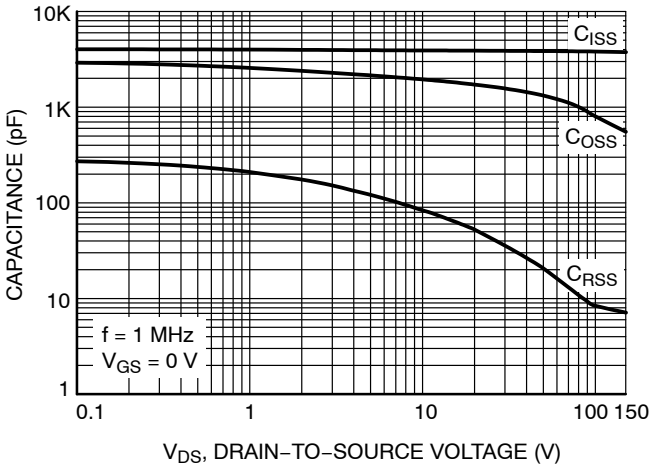


Figure 8. Capacitance vs. Drain−to−Source Voltage

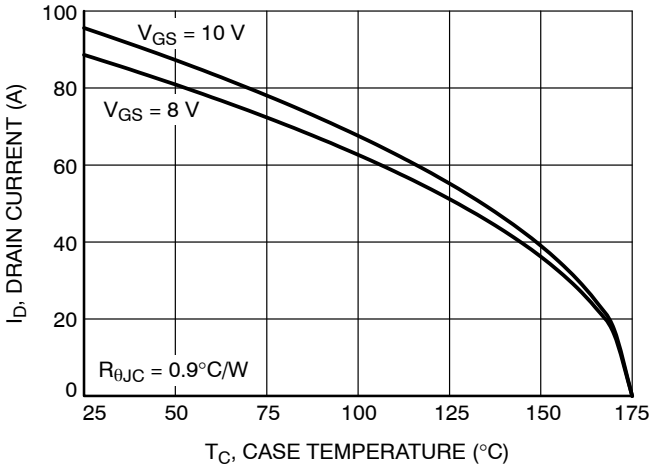


Figure 9. Drain Current vs. Case Temperature

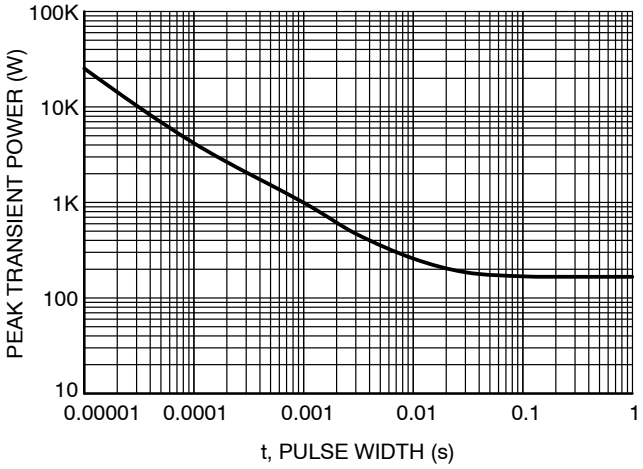


Figure 10. Peak Power

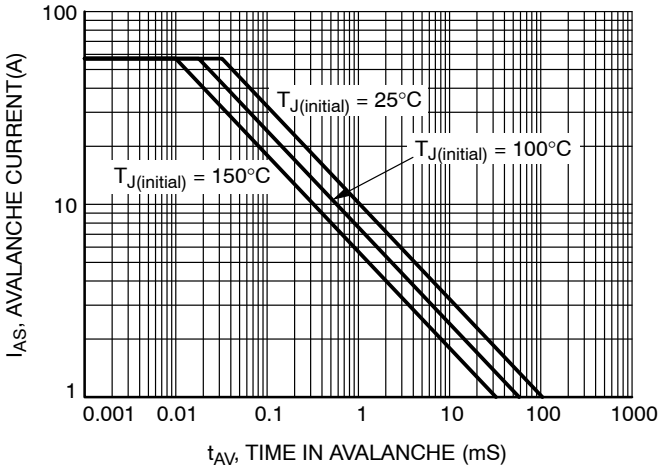


Figure 11. Unclamped Inductive Switching Capability

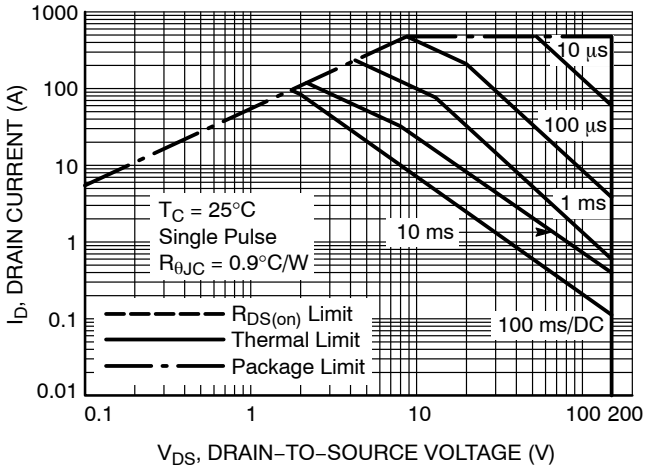


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

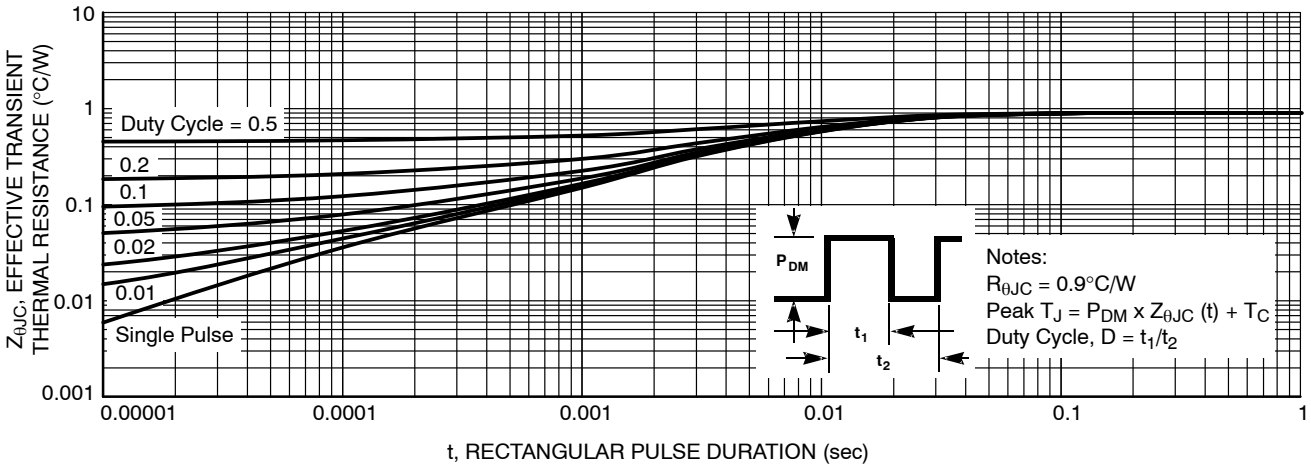
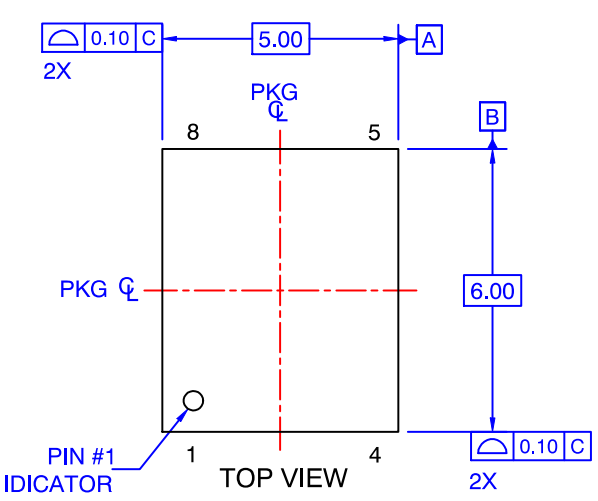
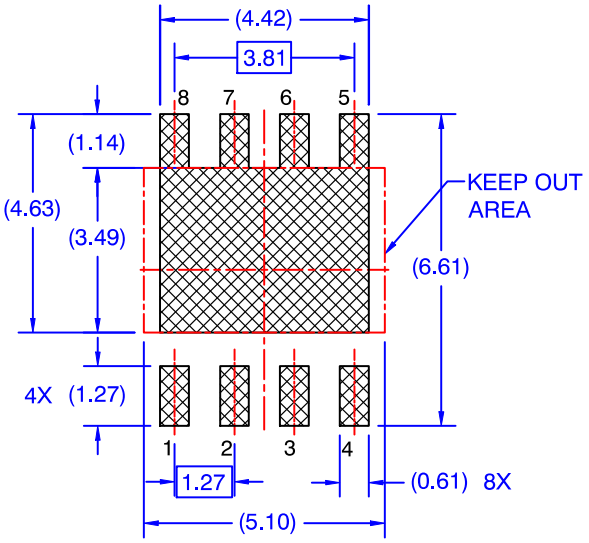


Figure 13. Transient Thermal Impedance

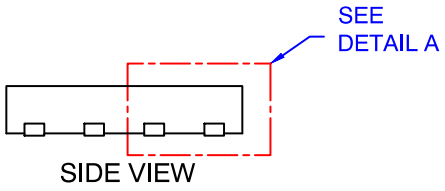
PACKAGE DIMENSIONS

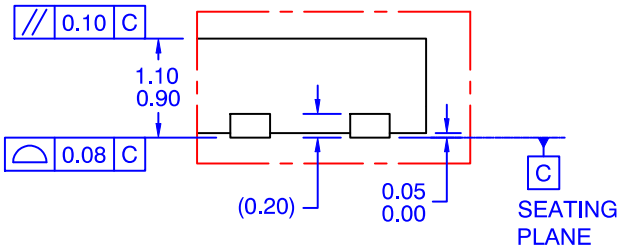
PQFN8 5X6, 1.27P
CASE 483AF
ISSUE O



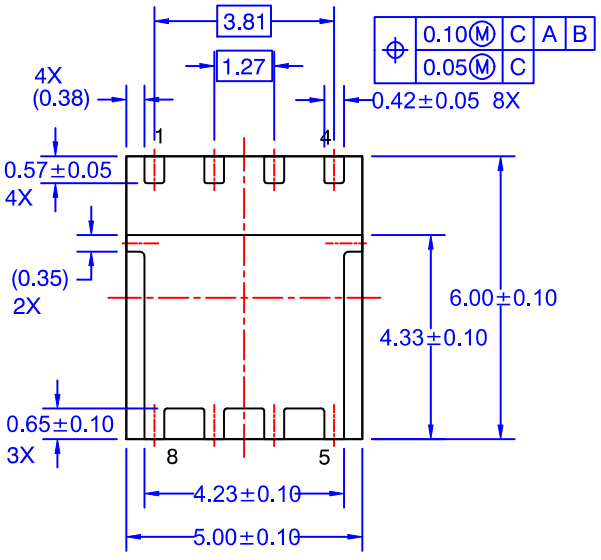


LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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