MOSFET - Power, Single N-Channel, SO8-FL

30 V, 0.58 mΩ, 462 A

NTMFS0D55N03CG

Features

- Wide SOA to Improve Inrush Current Management
- Advanced Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25°C	I_D	462	A
		T_C =100°C		326	
Power Dissipation $R_{\theta JC}$ (Note 3)		T_C = 25°C	P_D	199	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	65	A
		T_A = 100°C		46	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	3.9	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	35	A
		T_A = 100°C		25	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	1.1	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Source Current (Body Diode)			I_S	166	A
Single Pulse Drain−to−Source Avalanche Energy (I_L = 45.5 A_{pk})			E_{AS}	1346	mJ
Operating Junction and Storage Temperature Range			T_J, T_{STG}	−55 to +175	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in^2 pad, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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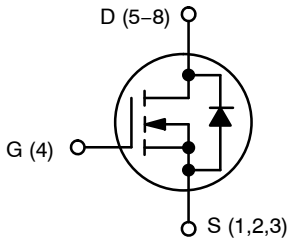
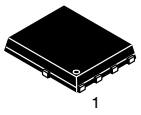
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	0.58 mΩ @ 10 V	462 A

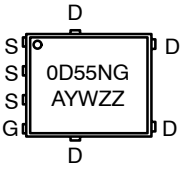


N−CHANNEL MOSFET



DFN5 (SO−8FL)
CASE 506EZ

MARKING DIAGRAMS



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	0.75	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	38	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	133	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA. ref to 25°C			12		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 330 μA		1.3		2.2	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 330 μA. ref to 25°C			−5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.5	0.58	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 3 V, I_D = 30 A			108		S
Gate Resistance	R_G	T_A = 25°C			0.4	3.0	Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		10150	14500	18500	pF
Output Capacitance	C_{OSS}			4501	6430	8359	
Reverse Transfer Capacitance	C_{RSS}			48	120	222	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 30 A		121.1	173	224.9	nC
Threshold Gate Charge	$Q_{G(TH)}$			15.4	22	28.6	
Gate−to−Source Charge	Q_{GS}			27.3	39	50.7	
Gate−to−Drain Charge	Q_{GD}			4.4	11	20.5	
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			30		ns
Rise Time	t_r				13		
Turn−Off Delay Time	$t_{d(OFF)}$				98		
Fall Time	t_f				20		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.75	1.2	V
			T_J = 125°C		0.62		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, V_{DS} = 15 V, I_S = 30 A			104		ns
Reverse Recovery Charge	Q_{RR}				177		nC

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

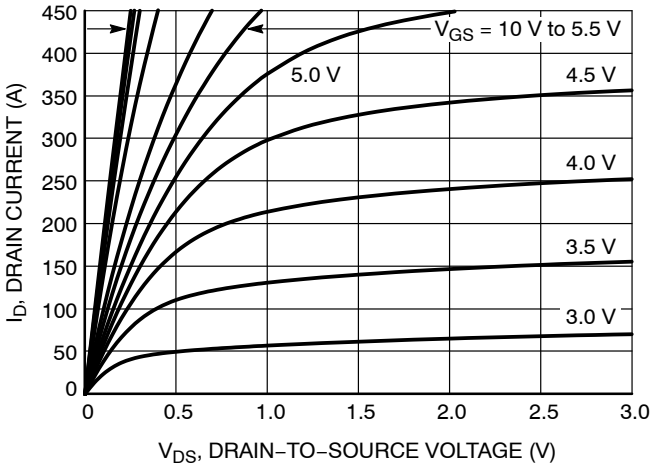


Figure 1. On−Region Characteristics

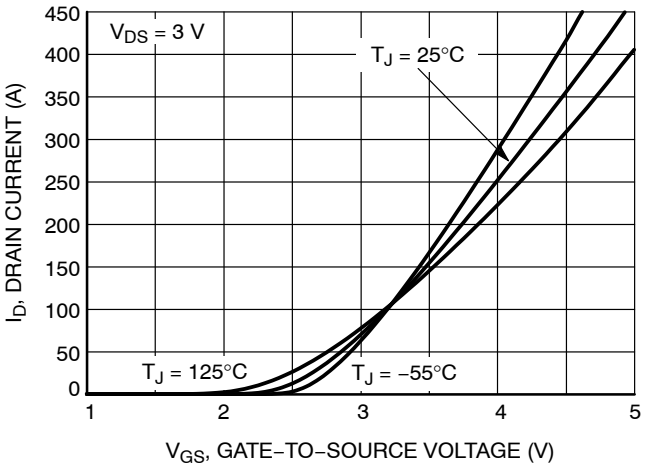


Figure 2. Transfer Characteristics

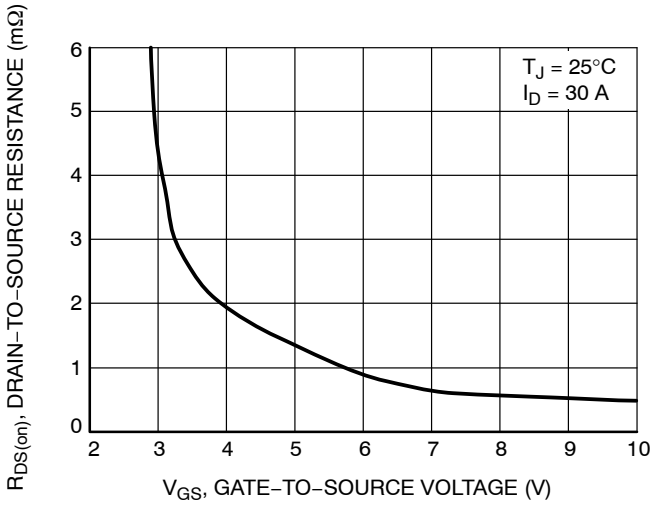


Figure 3. On−Resistance vs. Gate−to−Source Voltage

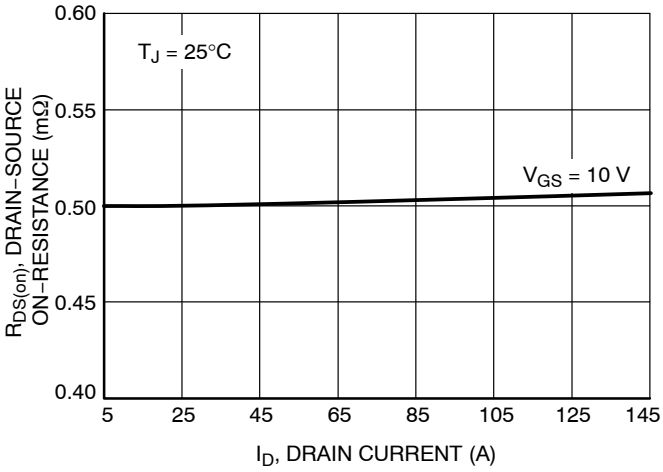


Figure 4. On−Resistance vs. Drain Current

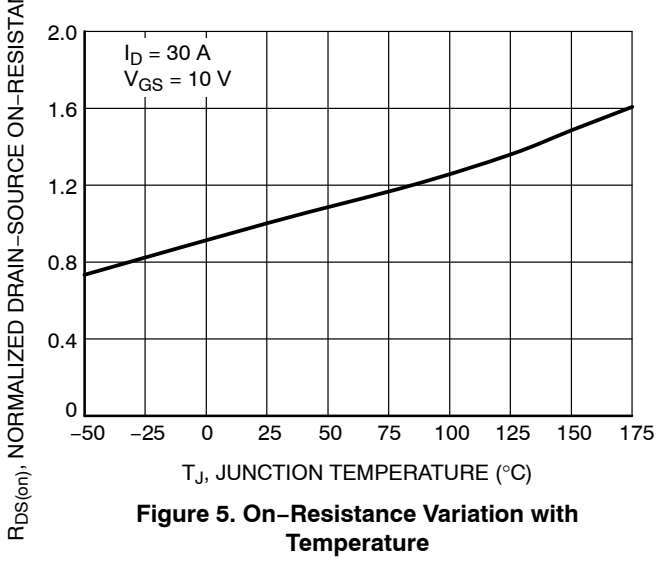


Figure 5. On−Resistance Variation with Temperature

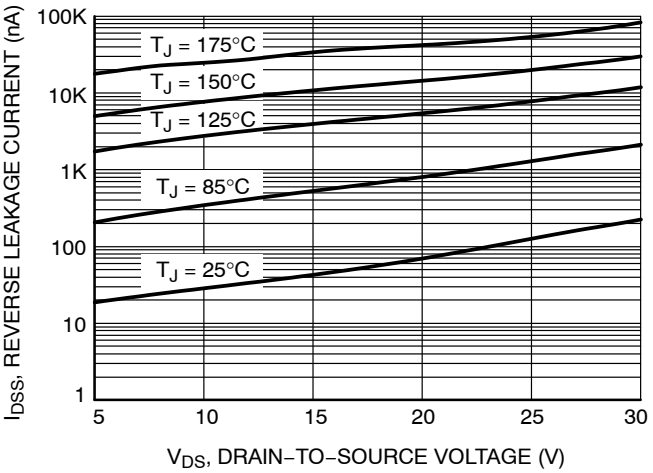


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

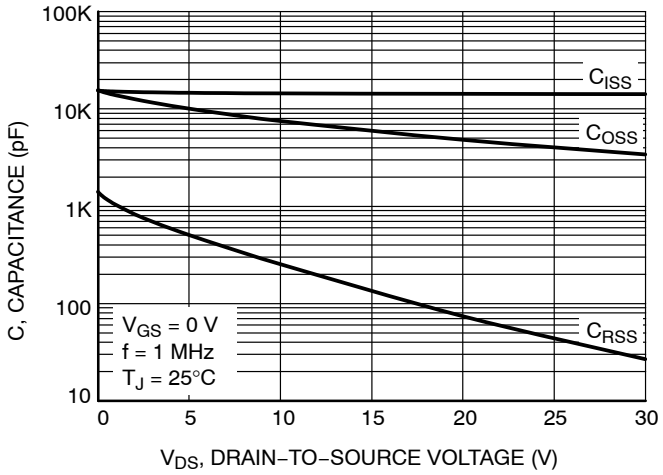


Figure 7. Capacitance Variation

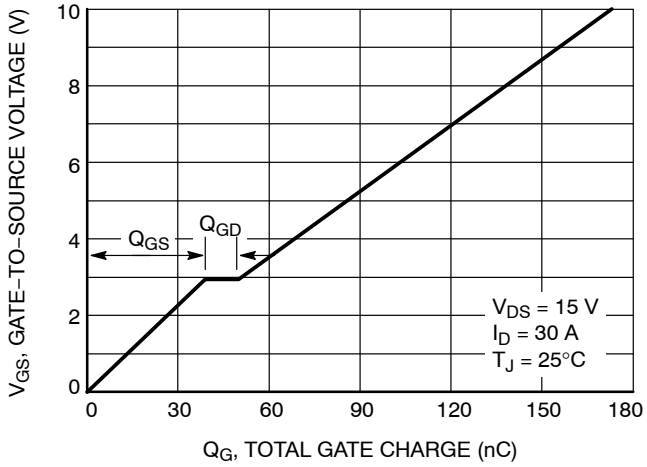


Figure 8. Gate−to−Source Voltage vs. Total Charge

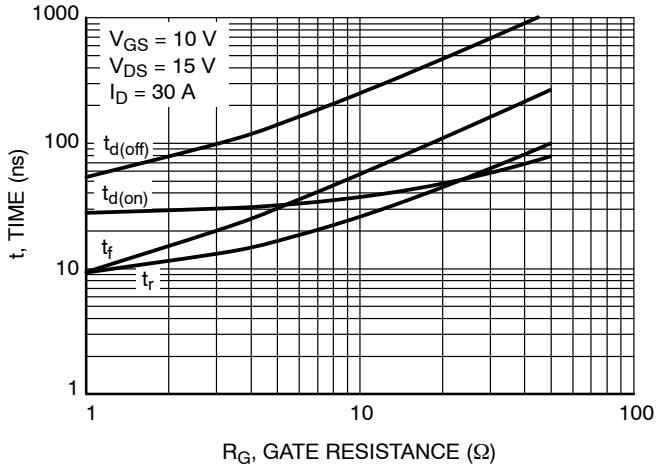


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

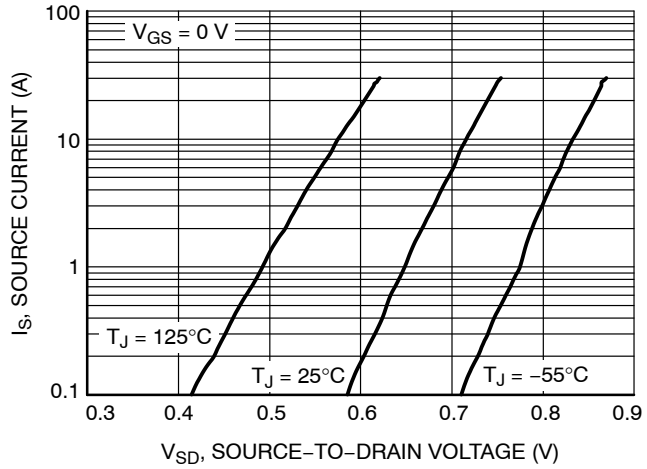


Figure 10. Diode Forward Voltage vs. Current

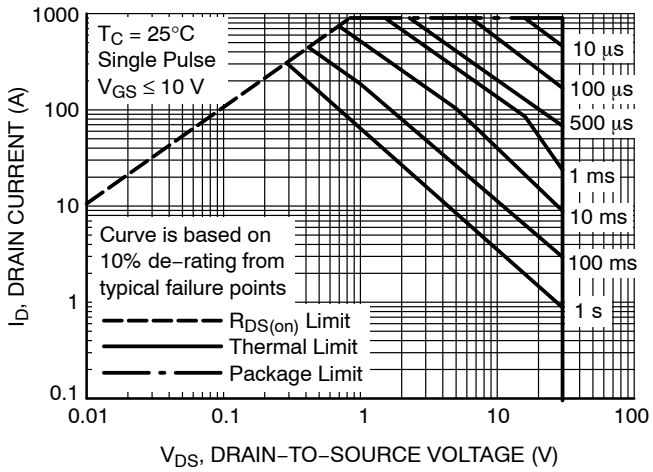


Figure 11. Safe Operating Area

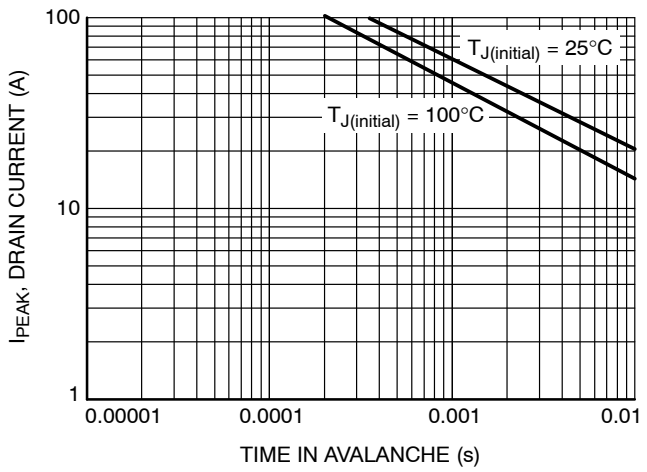


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

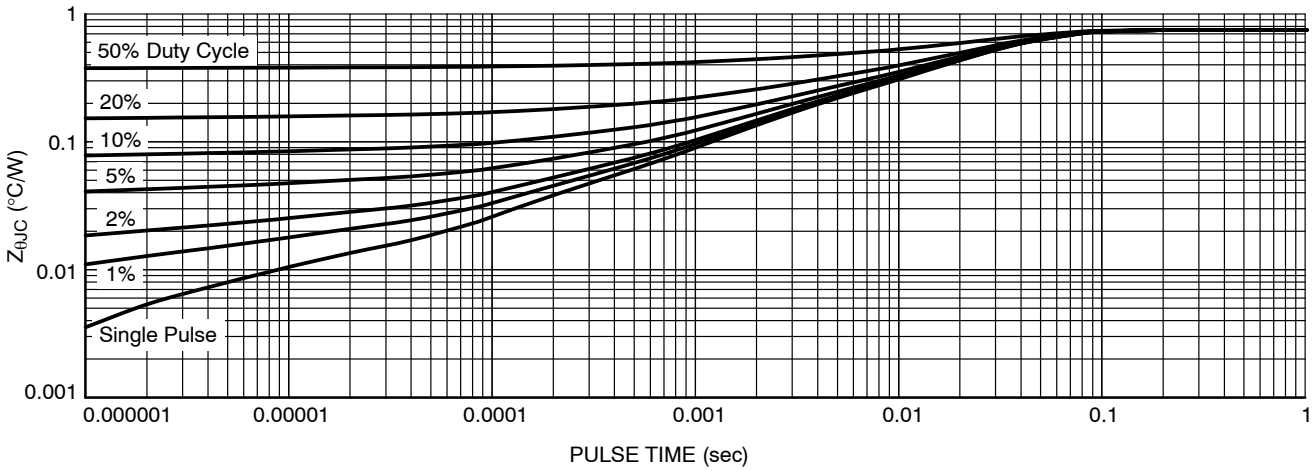


Figure 13. Junction−to−Case Transient Thermal Response

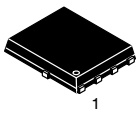
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS0D55N03CGT1G	0D55NG	DFN5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



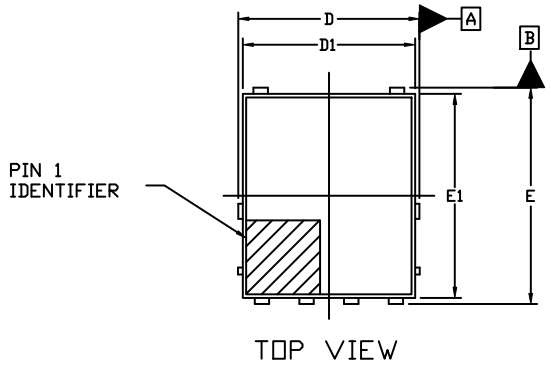
SCALE 2:1

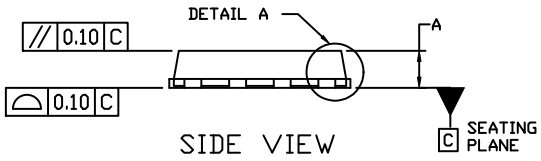
DFN5 5x6, 1.27P (SO−8FL)
CASE 506EZ
ISSUE A

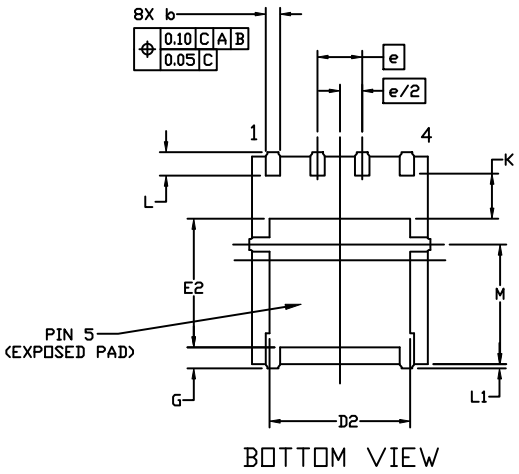
DATE 25 AUG 2021

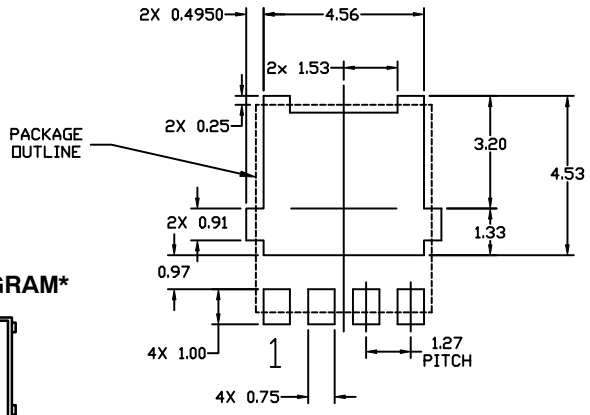
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



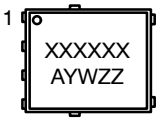






* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON24855H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

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