

MOSFET - N-Channel Shielded Gate PowerTrench® 150 V, 14 mΩ, 61 A



ON Semiconductor®

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NTMFS015N15MC

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

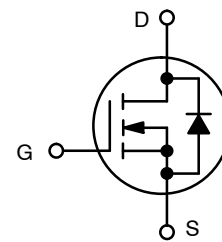
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	150	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	61	A	
Power Dissipation $R_{\theta JC}$ (Note 2)				P_D
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	9.2	A	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)				P_D
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 100 \mu\text{s}$	I_{DM}	302	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 10 A_{pk}, L = 3 \text{ mH}$)	E_{AS}	150	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

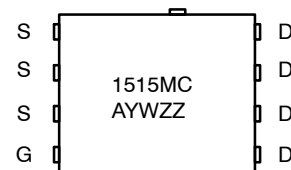
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	14 mΩ @ 10 V	61 A



N-CHANNEL MOSFET



MARKING DIAGRAM



1515MC = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS015N15MC (Pb-Free/Halogen Free)	Power 56 (PQFN8)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	1.15	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		109		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 162\ \mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 162\ \mu\text{A}$, ref to 25°C		-7.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		10.2	14	m Ω
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 8\text{ V}, I_D = 15\text{ A}$		11.1	16.2	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 29\text{ A}$		56		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2120		pF
Output Capacitance	C_{OSS}			595		
Reverse Transfer Capacitance	C_{RSS}			10.5		
Gate-Resistance	R_G			0.6	1.2	Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 29\text{ A}$		27		nC
Threshold Gate Charge	$Q_{G(TH)}$			7		
Gate-to-Source Charge	Q_{GS}			11		
Gate-to-Drain Charge	Q_{GD}			4		
Plateau Voltage	V_{GP}			5.5		
Output Charge	Q_{OSS}	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		66		nC

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 29\text{ A}, R_G = 6\ \Omega$		16		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			4		

DRAIN-SOURCE DIODE CHARACTERISTICS

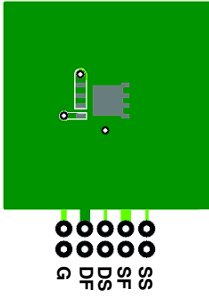
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$	$T_J = 25^\circ\text{C}$		0.86	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			49		ns
Reverse Recovery Charge	Q_{RR}				197		nC
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			34		ns
Reverse Recovery Charge	Q_{RR}				345		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

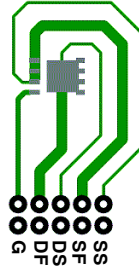
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NOTES:

3. Switching characteristics are independent of operating junction temperatures.
4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

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TYPICAL CHARACTERISTICS

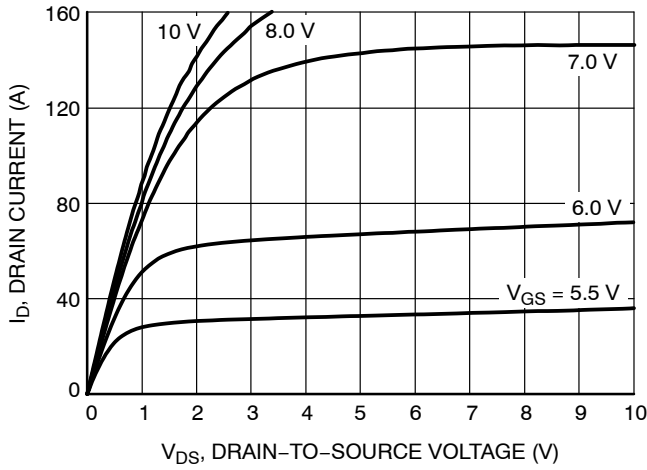


Figure 1. On-Region Characteristics

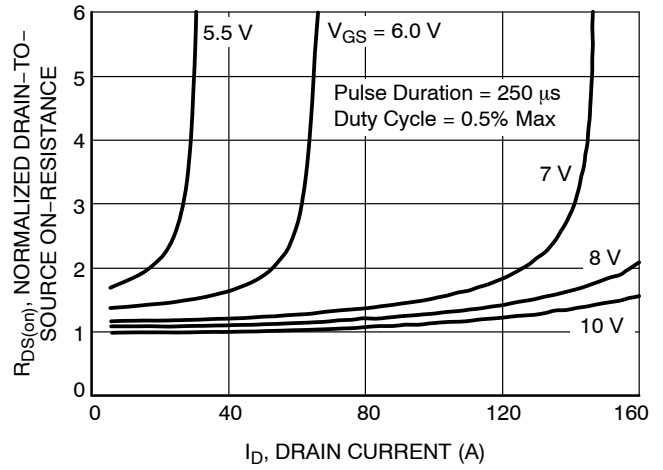


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

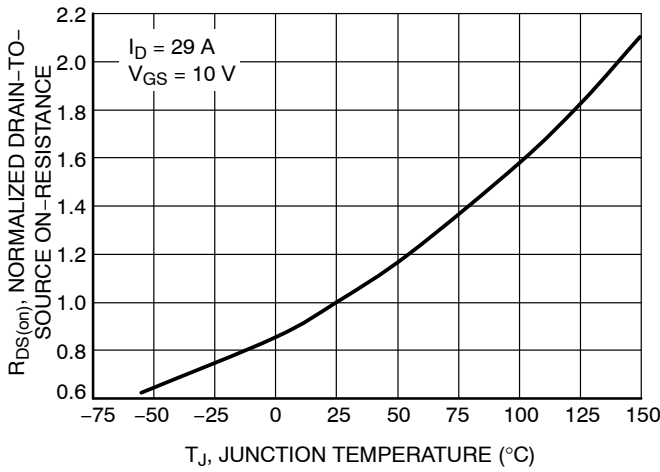


Figure 3. Normalized On-Resistance vs. Junction Temperature

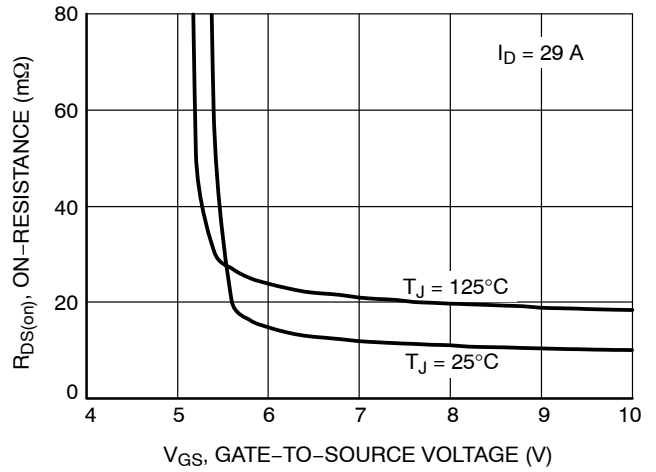


Figure 4. On-Resistance vs. Gate-to-Source Voltage

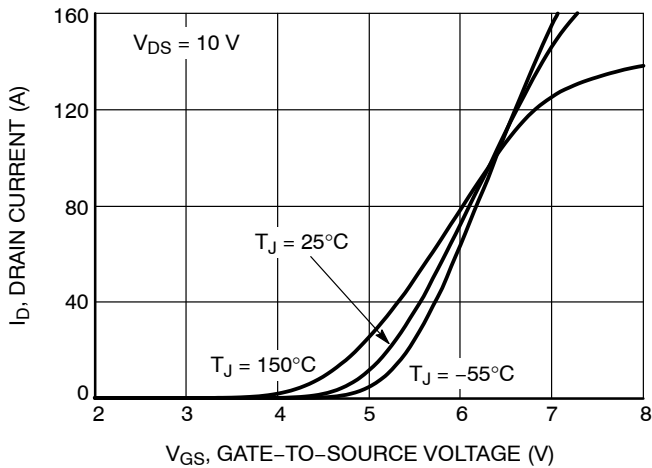


Figure 5. Transfer Characteristics

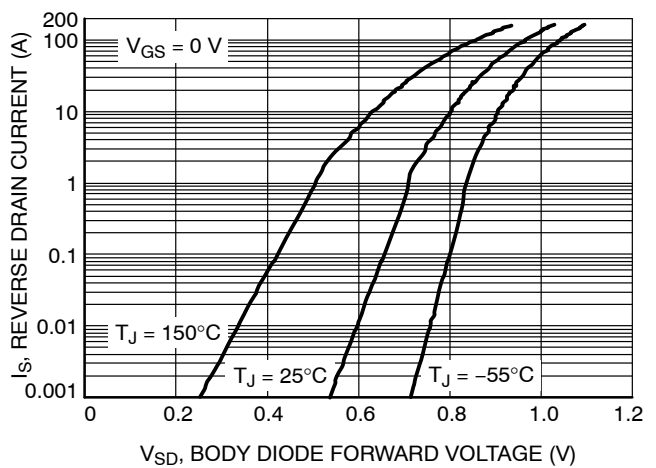


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

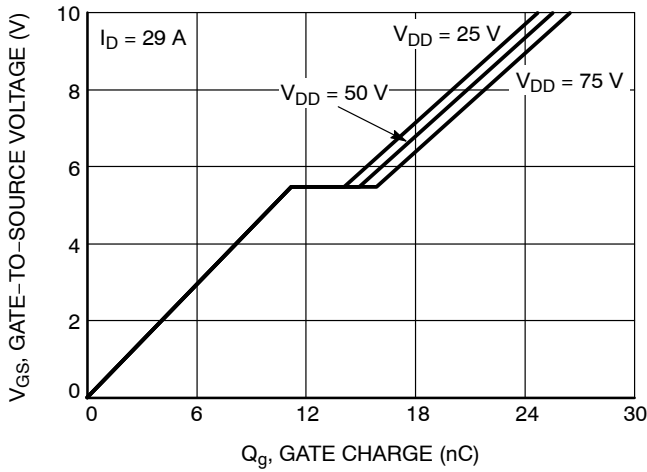


Figure 7. Gate Charge Characteristics

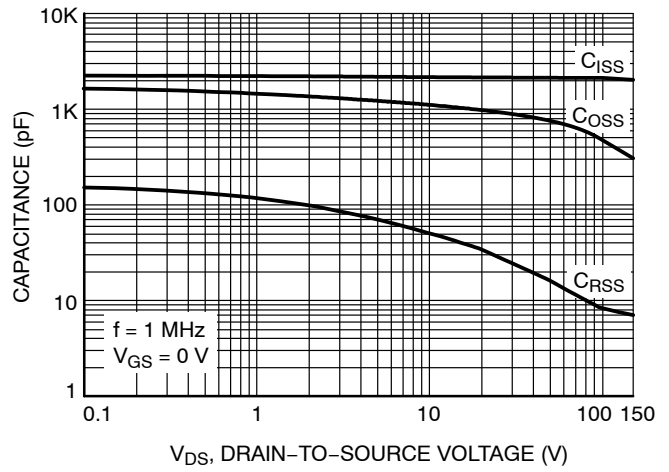


Figure 8. Capacitance vs. Drain-to-Source Voltage

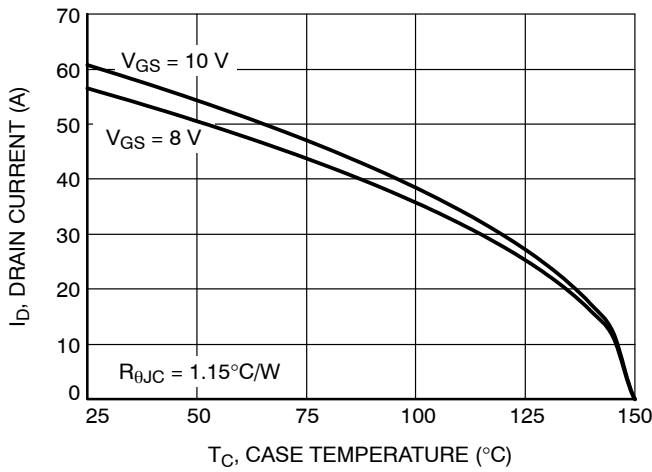


Figure 9. Drain Current vs. Case Temperature

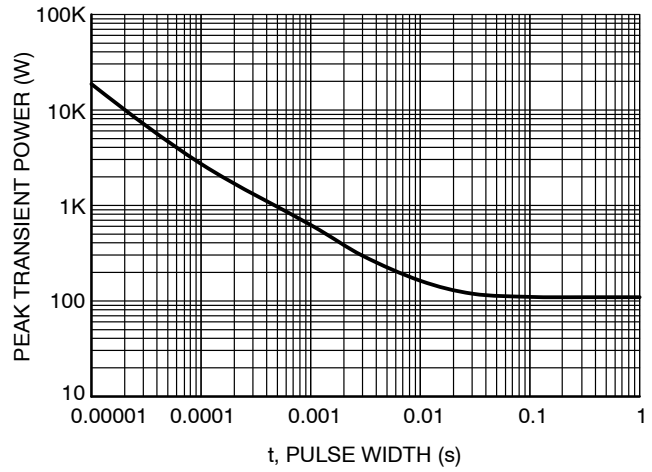


Figure 10. Peak Power

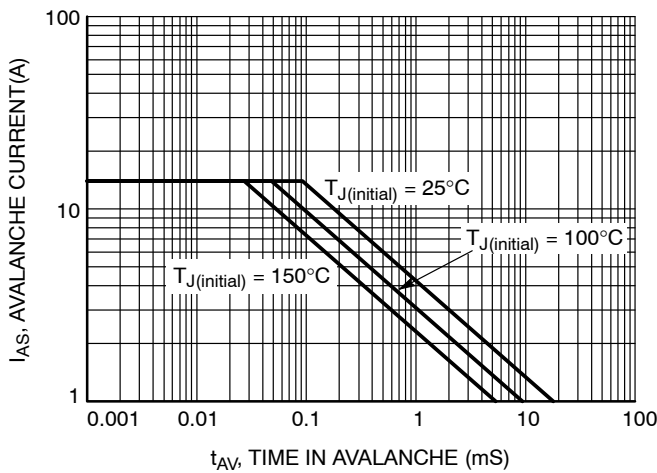


Figure 11. Unclamped Inductive Switching Capability

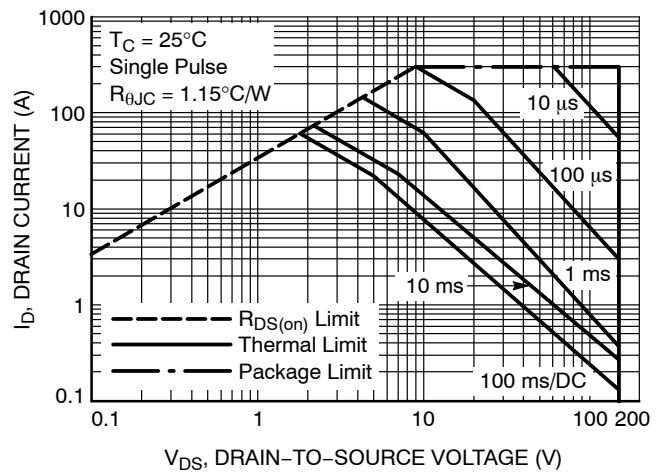


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

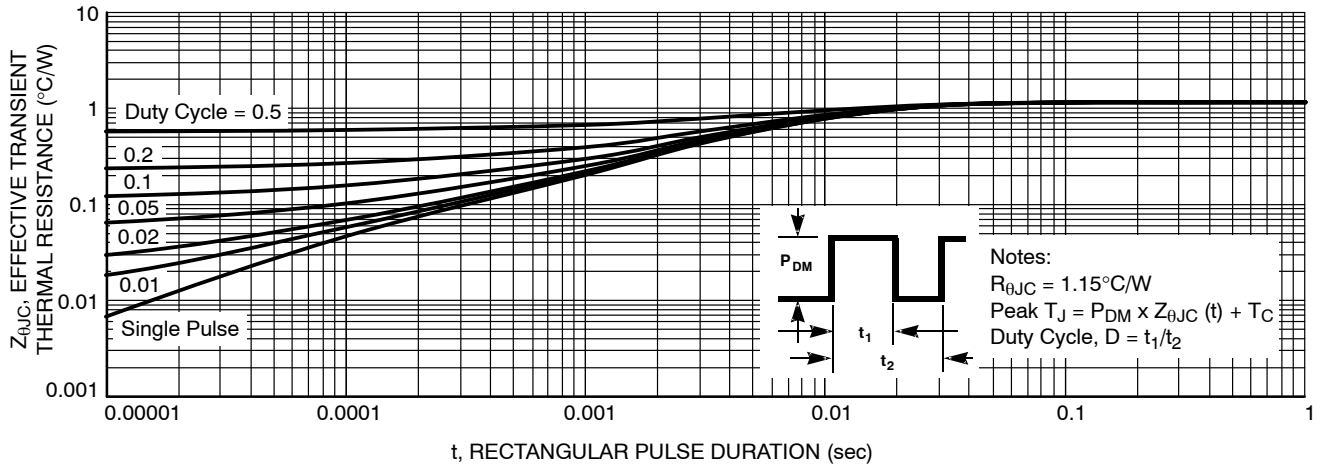
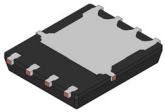


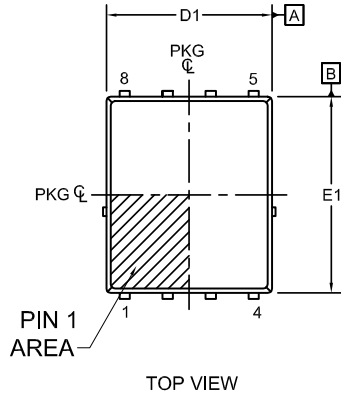
Figure 13. Transient Thermal Impedance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



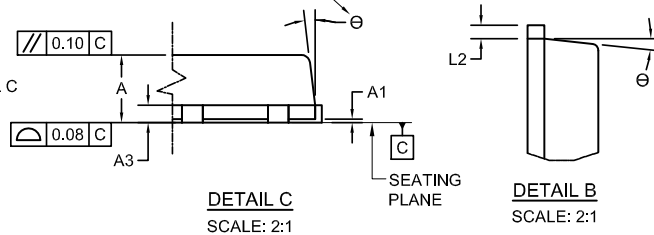
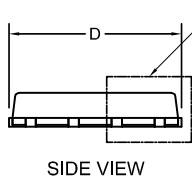
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

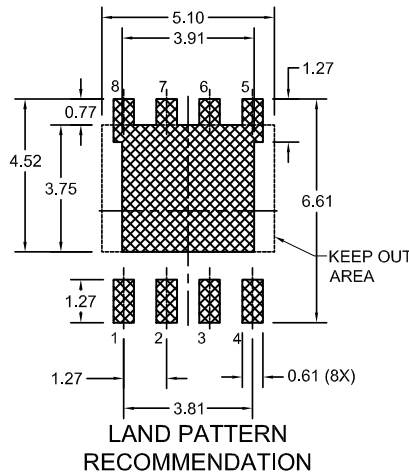
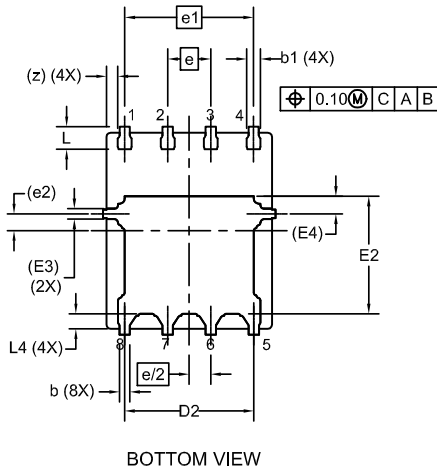


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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