

# **MOSFET** – Power, Single N-Channel, PQFN8 5x6

# 150 V, 11.5 mΩ, 78 A

# NTMFS011N15MC

#### **Features**

- Small Footprint (5 x 6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## **Typical Applications**

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

#### MAXIMUM RATINGS (T<sub>J</sub> = 25 °C, Unless otherwise specified)

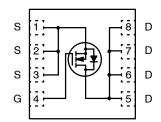
Para	Parameter		Symbol	Value	Unit
Drain-to-Source Break	down Voltage		$V_{(BR)DSS}$	150	٧
Gate-to-Source Voltag	е		$V_{GS}$	±20	V
$\begin{array}{c} \text{Continuous Drain} \\ \text{Current R}_{\theta JC} \\ \text{(Note 2)} \end{array}$	Steady State T <sub>C</sub> = 25 °C		Ι <sub>D</sub>	78	Α
Power Dissipation $R_{\theta JC}$ (Note 2)				147	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 2)	Steady State	, ,,		10.7	Α
Power Dissipation R <sub>0JA</sub> (Note 1, 2)			P <sub>D</sub>	2.7	W
Pulsed Drain Current	$T_A = 25  ^{\circ}C, t_p = 250  \mu s$		I <sub>DM</sub>	259	Α
Operating Junction and	nd Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body	urce Current (Body Diode)		I <sub>S</sub>	133	Α
Single Pulse Drain-to-S Energy (I <sub>AV</sub> = 39 A, L =			E <sub>AS</sub>	76.1	mJ
Lead Temperature Solo Soldering Purposes (1,			TL	300	°C

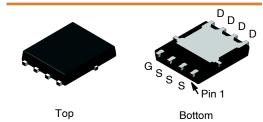
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
150 V	11.5 mΩ @ 10 V	35 A
150 V	13.2 mΩ @ 8 V	18 A

#### **N-Channel MOSFET**





PQFN8 5x6, 1.27P (Power 56) CASE 483AE

#### **MARKING DIAGRAM**



A = Assembly Location Y = Year

W = Work Week ZZ = Lot Traceability

## **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

#### THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{ hetaJC}$	Junction-to-Case – Steady State (Note 5)	0.85	°C/W
$R_{ hetaJA}$	Junction-to-Ambient – Steady State (Note 5)	46	

## **ORDERING INFORMATION**

Device	Device Marking	Package	Shipping (Qty / Packing) <sup>†</sup>
NTMFS011N15MC	NTMFS011N15MC	PQFN8 5x6, 1.27 P (Power 56) (Pb-Free/Halogen Free)	3000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25 \, ^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Тур	Max	Unit
OFF CHARAC	TERISTICS	•				-	
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		150			V
V <sub>(BR)DSS</sub> / T <sub>J</sub>	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , ref to	25 °C		85		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 120 V	T <sub>J</sub> = 25 °C			1	μΑ
			T <sub>J</sub> = 125 °C			100	
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 1	±20 V			±100	nA
ON CHARACT	TERISTICS (Note 3)						
V <sub>GS(TH)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 19$	94 μΑ	2.5	3.35	4.5	V
V <sub>GS(TH)</sub> / T <sub>J</sub>	Negative Threshold Temperature Coefficient	$I_D = 250 \mu A$ , ref to	25 °C		-7.2		mV/°C
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> =	35 A		9.0	11.5	mΩ
		V <sub>GS</sub> = 8 V, I <sub>D</sub> = 1	8 A		9.7	13.2	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> =	18 A		96	116	S
R <sub>G</sub>	Gate-Resistance	T <sub>A</sub> = 25 °C			0.9	1.1	Ω
CHARGES & (	CAPACITANCES					•	
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, f = 1 MHz, \	/ <sub>DS</sub> = 75 V		2478	3592	pF
coss	Output Capacitance	7			728	1092	
C <sub>RSS</sub>	Reverse Transfer Capacitance	7			7.9	15	
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 75 V	I <sub>D</sub> = 35 A		30.6	46	nC
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 75 V	/, I <sub>D</sub> = 35 A		30.7	46	
Q <sub>GS</sub>	Gate-to-Source Charge				12.8		
Q <sub>SW</sub>	Switching Charge	1			9.4		
Q <sub>GD</sub>	Gate-to-Drain Charge	1			4.5		
Q <sub>OSS</sub>	Output Charge	V <sub>GS</sub> = 0 V, V <sub>DD</sub> =	75 V		95		
V <sub>GP</sub>	Plateau Voltage	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 75 V	/, I <sub>D</sub> = 35 A		5.1		V
SWITCHING C	CHARACTERISTICS (Note 3)	•			•	•	
t <sub>d(ON)</sub>	Turn-On Delay Time	$V_{GS} = 10 \text{ V}, V_{DS} = 75 \text{ V}$ $R_G = 6 \Omega$	, I <sub>D</sub> = 35 A,		19.8		ns
t <sub>r</sub>	Rise Time	$R_G = 6 \Omega$			4.7		1
t <sub>d(OFF)</sub>	Turn-Off Delay Time	1			25.5		
t <sub>f</sub>	Fall Time	7			4.0		

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted) (continued)

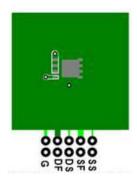
Symbol	Parameter	Test Conditio	Test Conditions		Тур	Max	Unit
DRAIN-SOUR	DRAIN-SOURCE DIODE CHARACTERISTICS						
$V_{SD}$	Forward Diode Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 35 A	T <sub>J</sub> = 25 °C		0.869		V
			T <sub>J</sub> = 125 °C		0.725		
t <sub>RR</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, dl <sub>S</sub> /dt = 3	800 A/μs,		48.8		ns
Q <sub>RR</sub>	Reverse Recovery Charge	I <sub>S</sub> = 35 A	I <sub>S</sub> = 35 A		227		nC
t <sub>RR</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 1$	$V_{GS}$ = 0 V, $dI_S/dt$ = 1000 A/ $\mu$ s, $I_S$ = 35 A		36.4		ns
Q <sub>RR</sub>	Reverse Recovery Charge	I <sub>S</sub> = 35 A			407		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

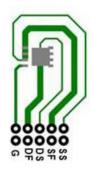
3. Switching characteristics are independent of operating junction temperatures.

#### NOTES:

4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



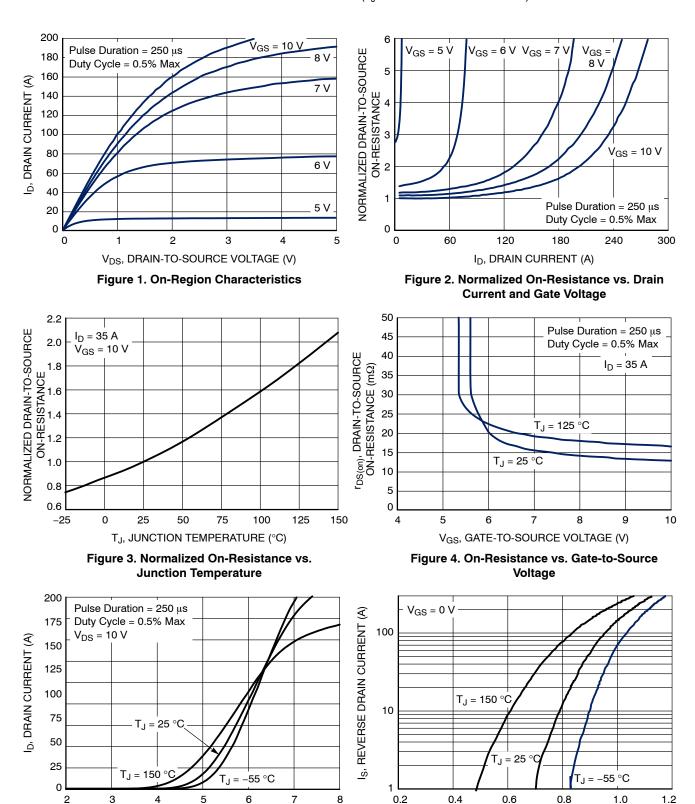
a) 46 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 116 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.</li>
   E<sub>AS</sub> of 196 mJ is based on starting T<sub>J</sub> = 25 °C; L = 3 mH, I<sub>AS</sub> = 12.7 A, V<sub>DD</sub> = 100 V, V<sub>GS</sub> = 15 V. 100% tested at L = 0.1 mH, I<sub>AS</sub> = 41 A.
   Pulsed I<sub>D</sub> please refer to Fig 11 SOA graph for more details.
   Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## TYPICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted)



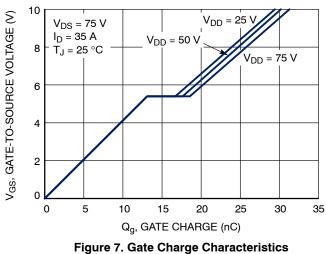
V<sub>SD</sub>, BODY DIODE FORWARD VOLTAGE (V)

Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 5. Transfer Characteristics

## TYPICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted) (continued)



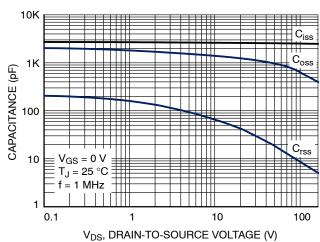


Figure 8. Capacitance vs. Drain-to-Source Voltage

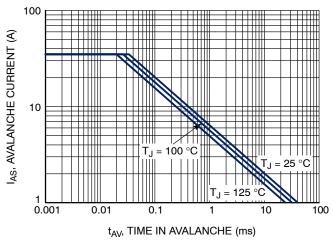


Figure 9. Unclamped Inductive Switching Capability

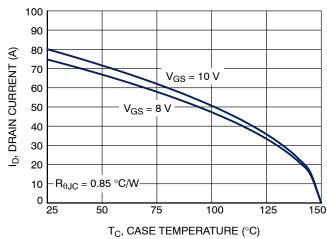


Figure 10. Maximum Continuous Drain **Current vs. Case Temperature** 

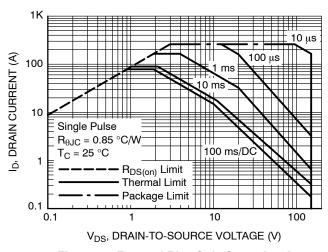


Figure 11. Forward Bias Safe Operating Area

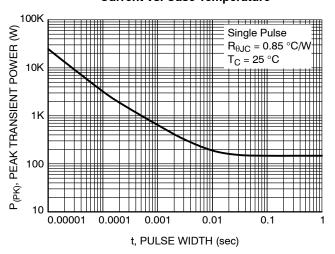


Figure 12. Single Pulse Maximum Power Dissipation

## **TYPICAL CHARACTERISTICS** ( $T_J$ = 25 $^{\circ}$ C unless otherwise noted) (continued)

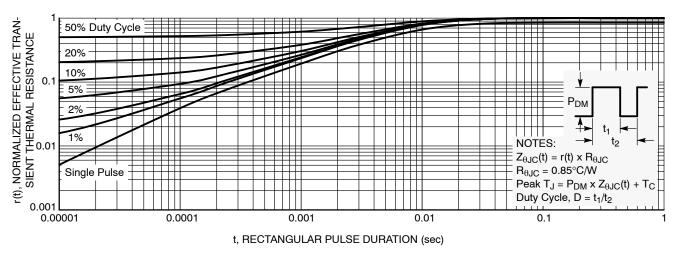


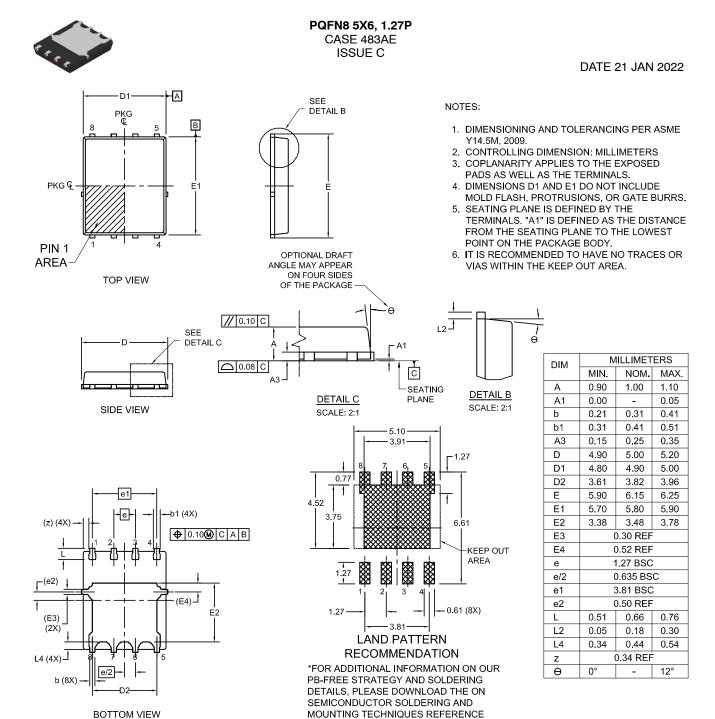
Figure 13. Junction-to-Case Transient Thermal Response Curve

## **REVISION HISTORY**

Revision	Description of Changes	Date
2	Document rebranded to <b>onsemi</b> format.	11/5/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.





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