

MOSFET - Power, Single P-Channel, SO8-FL

-30 V, 1.4 mΩ, -263 A

NTMFS002P03P8Z

Features

- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 5x6mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-30	V
Gate-to-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	-263
		$T_C = 85^\circ\text{C}$		-189
		$T_C = 25^\circ\text{C}$	P_D	138.9
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-40.2
		$T_A = 85^\circ\text{C}$		-29
		$T_A = 25^\circ\text{C}$	P_D	3.3
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	-648	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 65.16 \text{ A}$)		E_{AS}	212.3	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

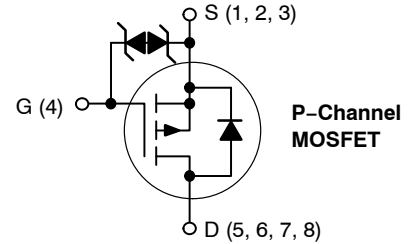
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

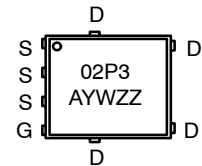
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Drain) (Note 2)	$R_{\theta JC}$	0.9	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38.3	$^\circ\text{C}/\text{W}$

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad. Assuming a 76 mm x 76 mm x 1.6 mm board.

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30 V	1.4 mΩ @ -10 V	-263 A
	2.3 mΩ @ -4.5 V	



MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFS002P03P8ZT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA, ref to 25°C		-3.3		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V, T _J = 25°C			-1.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 25 V			± 10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1.0		-3.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = -250 μA, ref to 25°C		5.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -23 A		0.9	1.4	mΩ
		V _{GS} = -4.5 V, I _D = -20 A		1.5	2.3	
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -20 A		129		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -15 V		14950		pF
Output Capacitance	C _{oss}			5280		
Reverse Transfer Capacitance	C _{rss}			4870		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -23 A		217		nC
Threshold Gate Charge	Q _{G(TH)}			13		
Gate-to-Source Charge	Q _{GS}			35		
Gate-to-Drain Charge	Q _{GD}			145		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -23 A		365		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -23 A, R _G = 6 Ω		68		ns
Rise Time	t _r			375		
Turn-Off Delay Time	t _{d(off)}			160		
Fall Time	t _f			317		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -23 A, R _G = 6 Ω		27		ns
Rise Time	t _r			78		
Turn-Off Delay Time	t _{d(off)}			280		
Fall Time	t _f			295		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -23 A	T _J = 25°C	-0.65	-1.3	V
			T _J = 125°C	-0.48		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -23 A		82		ns
Charge Time	t _a			47		
Discharge Time	t _b			36		
Reverse Recovery Charge	Q _{RR}			180		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

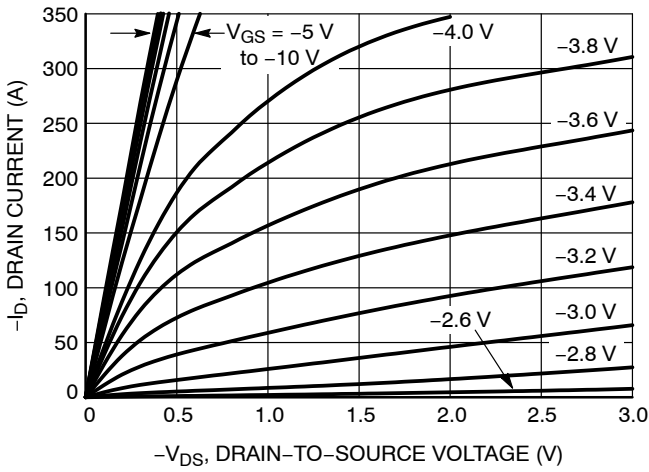


Figure 1. On-Region Characteristics

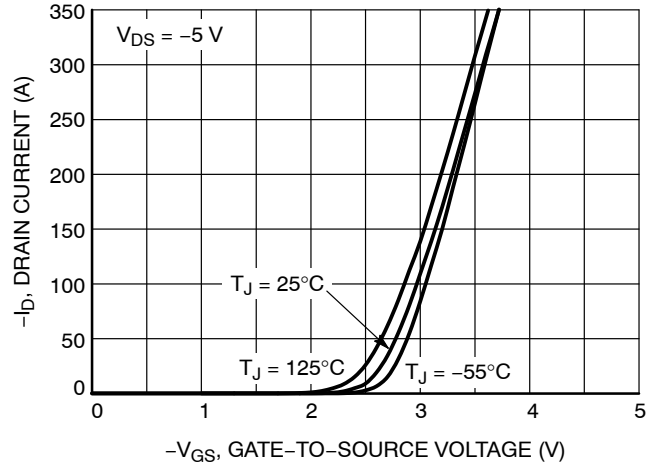


Figure 2. Transfer Characteristics

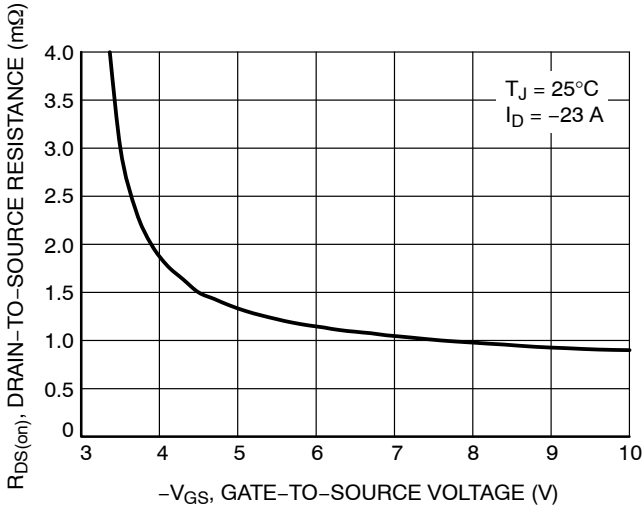


Figure 3. On-Resistance vs. Gate-to-Source Voltage

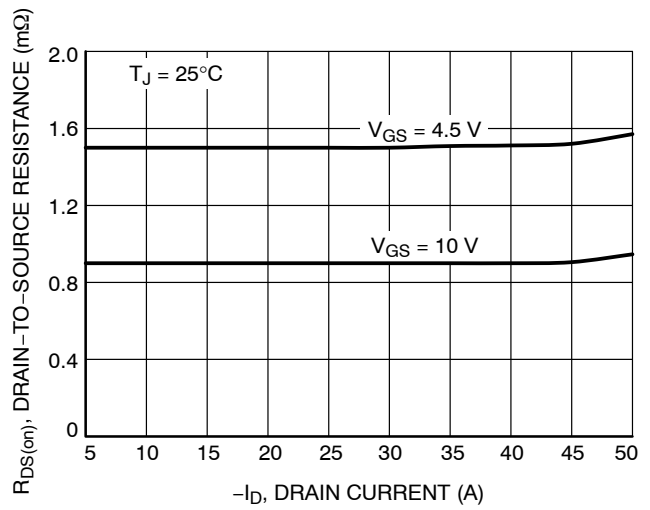


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

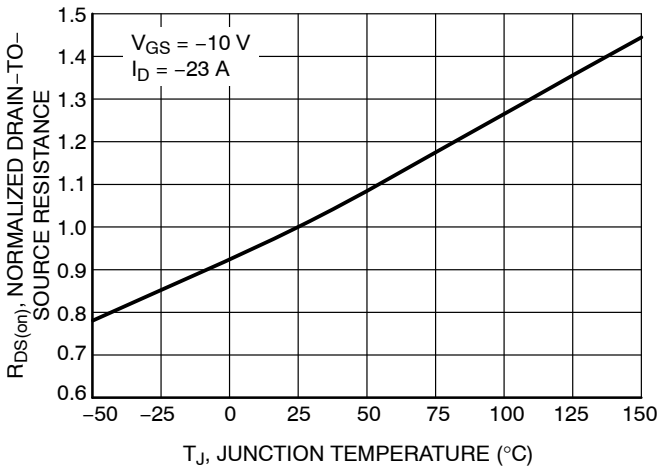


Figure 5. On-Resistance Variation with Temperature

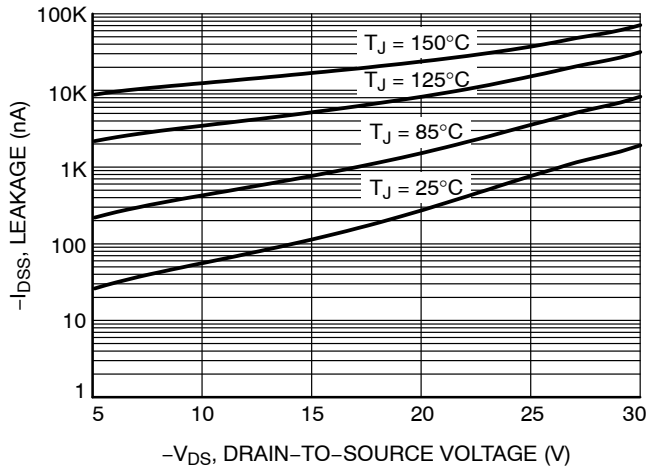


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

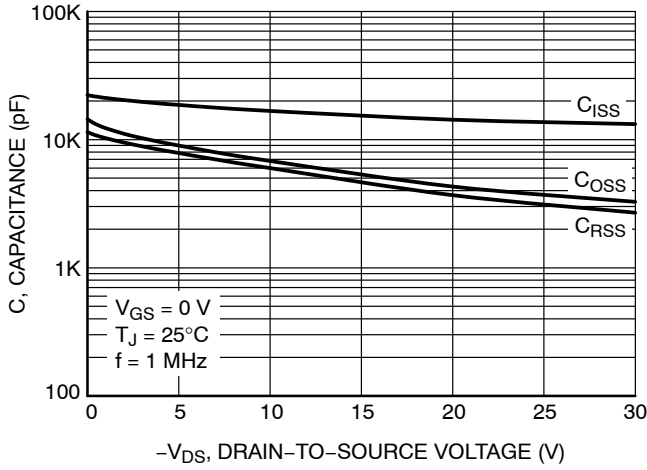


Figure 7. Capacitance Variation

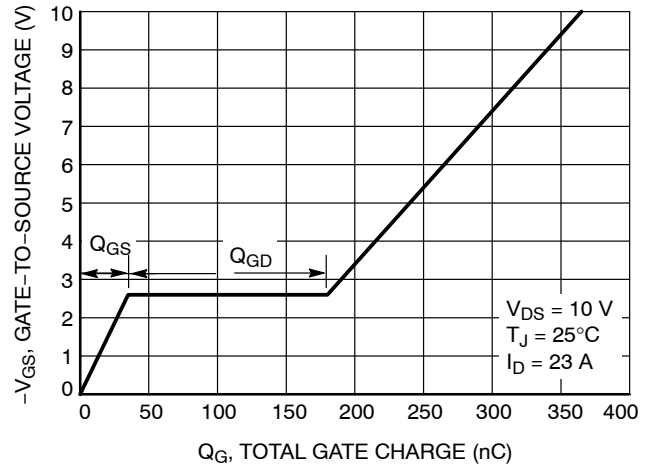


Figure 8. Gate-to-Source Voltage vs. Total Charge

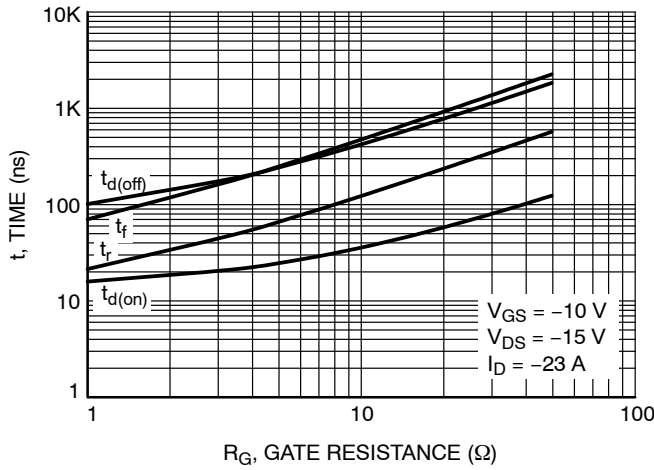


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

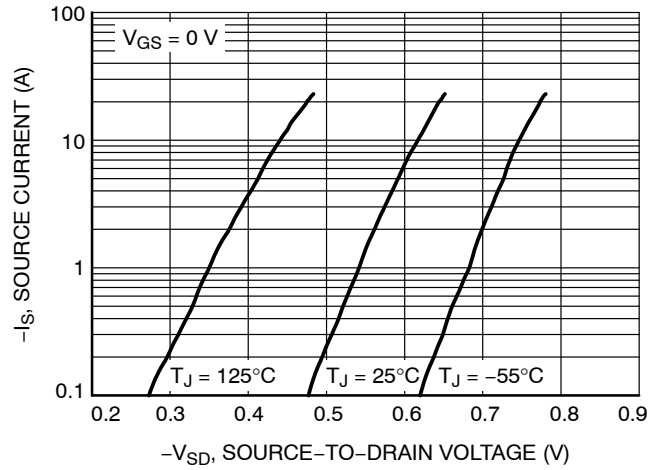


Figure 10. Diode Forward Voltage vs. Current

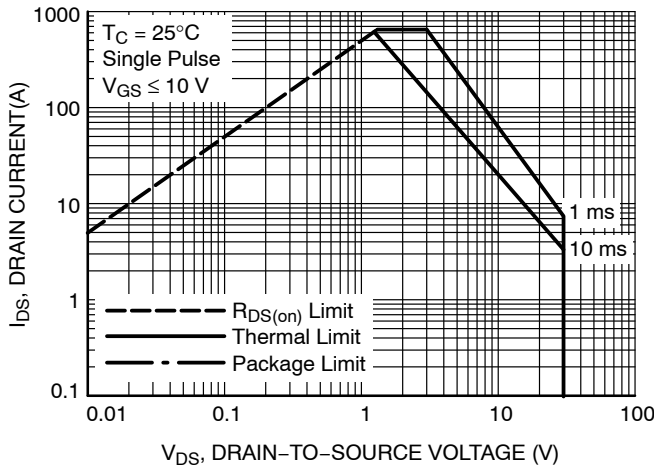


Figure 11. Maximum Rated Forward Biased Safe Operating Area

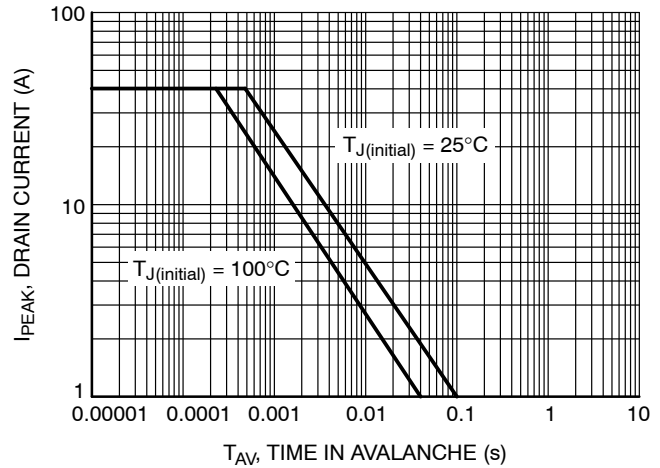


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

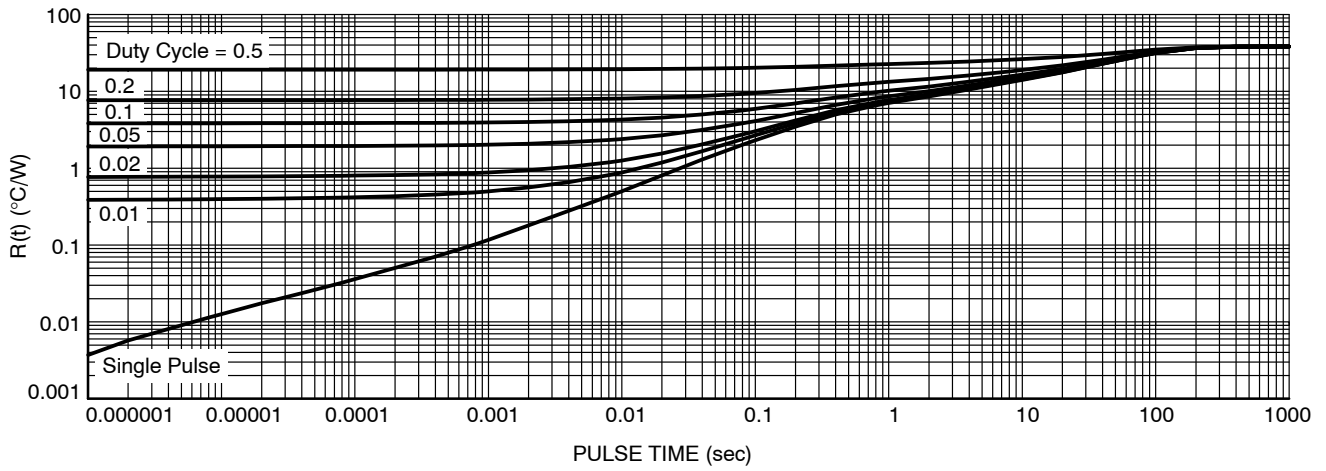
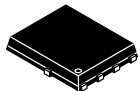


Figure 13. Thermal Characteristics

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

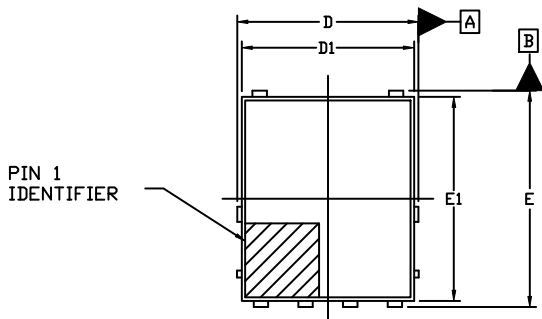
ON Semiconductor®



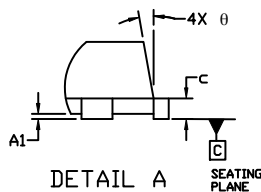
1
SCALE 2:1

DFN5 5x6, 1.27P (SO-8FL)
CASE 506EZ
ISSUE A

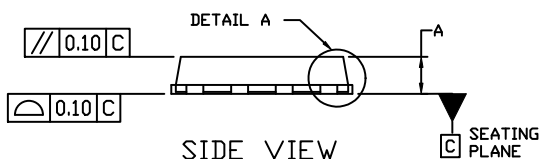
DATE 25 AUG 2021



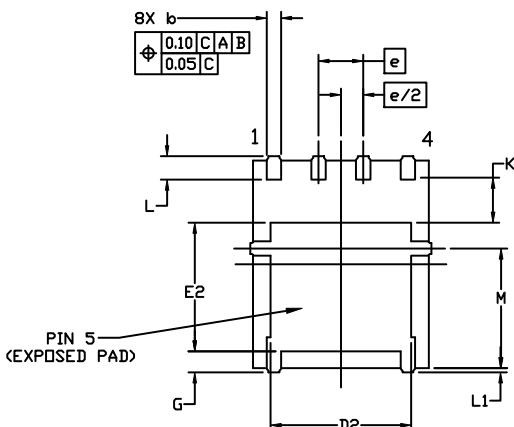
TOP VIEW



DETAIL A



SIDE VIEW



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

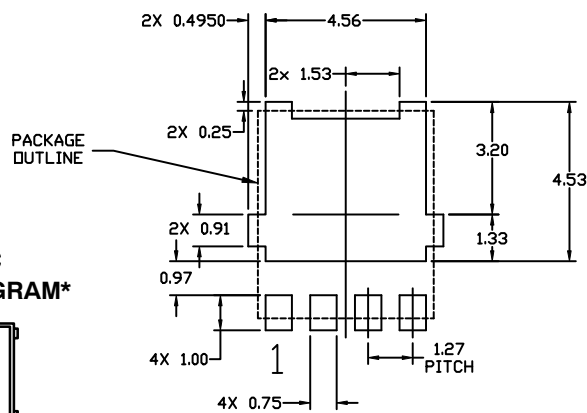


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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