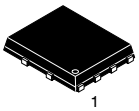
MOSFET – Power, Dual N-Channel, DUAL SO8FL

60 V, 27 A, 20.3 mΩ

NTMFD020N06C

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	20.3 mΩ @ 10 V	27 A



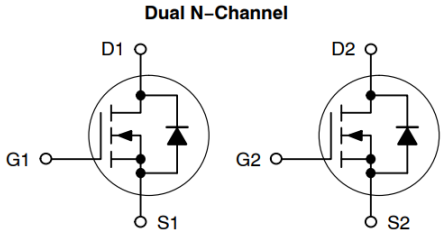
DFN8 5x6
(SO8FL)
CASE 506BT

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation



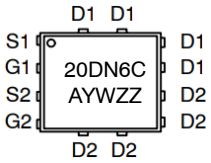
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Symbol	Parameter			Value	Units
V_{DSS}	Drain−to−Source Voltage			60	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	27	A
			T_C = 100°C	19	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	31	W
			T_C = 100°C	15	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	8	A
			T_A = 100°C	6	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	3.1	W
			T_A = 100°C	1.5	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		98	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			25	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (I_L = 5.7 A_{pk})			16	mJ
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



20DN6C = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFD020N06CT1G	SO8FL Dual (Pb-Free)	1,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State (Note 2)	4.8	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	47	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60			V
$V_{(BR)DSS}$ / T_J	Drain−to−Source Breakdown Voltage Temperature Coefficient	I_D = 250 μA, ref to 25°C			29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 20 μA		2.0		4.0	V
$V_{GS(TH)}$ / T_J	Negative Threshold Temperature Coefficient	I_D = 20 μA, ref to 25°C			−7.8		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 4 A			16.9	20.3	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 4 A			12		S
R_G	Gate Resistance	T_A = 25°C			1.0		Ω
CHARGES & CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 30 V			355		pF
C_{OSS}	Output Capacitance				260		
C_{RSS}	Reverse Capacitance				4.9		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 4 A			5.8		nC
$Q_{G(TH)}$	Threshold Gate Charge				1.4		
Q_{GS}	Gate−to−Source Charge				2.3		
Q_{GD}	Gate−to−Drain Charge				0.53		
SWITCHING CHARACTERISTICS (Note 3)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 4 A, R_G = 6 Ω			6.5		ns
t_r	Rise Time				1.4		
$t_{d(OFF)}$	Turn−Off Delay Time				9.7		
t_f	Fall Time				4.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Voltage	V_{GS} = 0 V, I_S = 4 A	T_J = 25°C		0.81	1.2	V
			T_J = 125°C		0.67		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 4 A			24		ns
ta	Charge Time				12		
tb	Discharge Time				12		
Q_{RR}	Reverse Recovery Charge				12		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

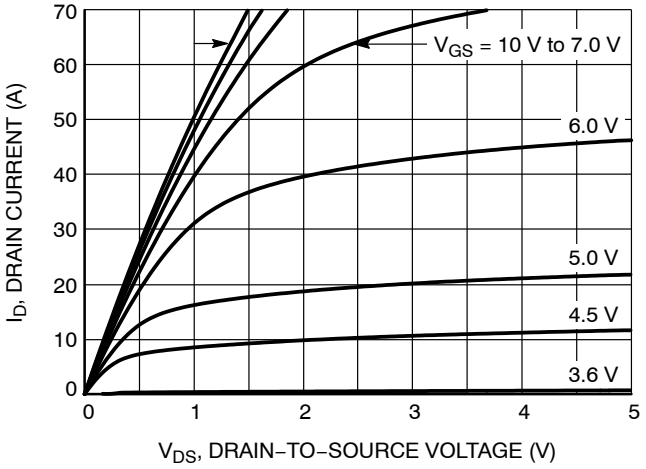


Figure 1. On−Region Characteristics

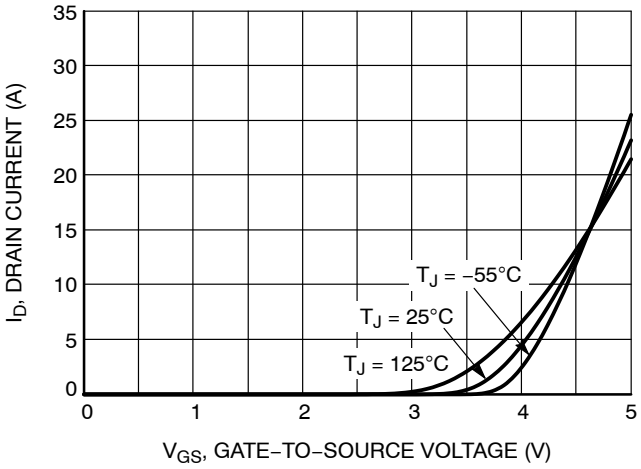


Figure 2. Transfer Characteristics

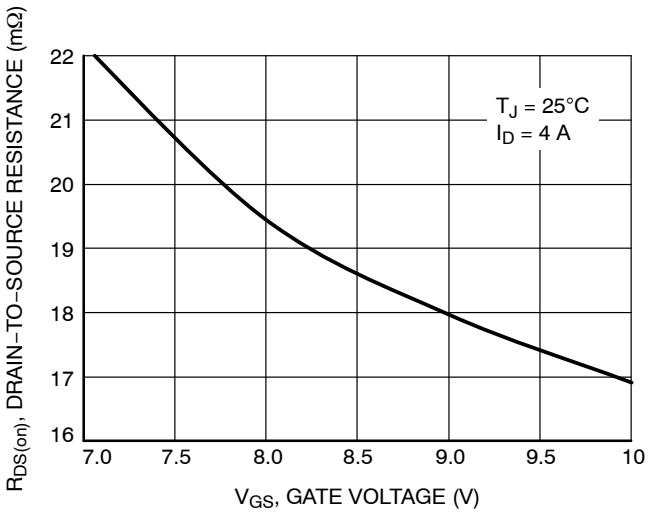


Figure 3. On−Resistance vs. Gate−to−Source Voltage

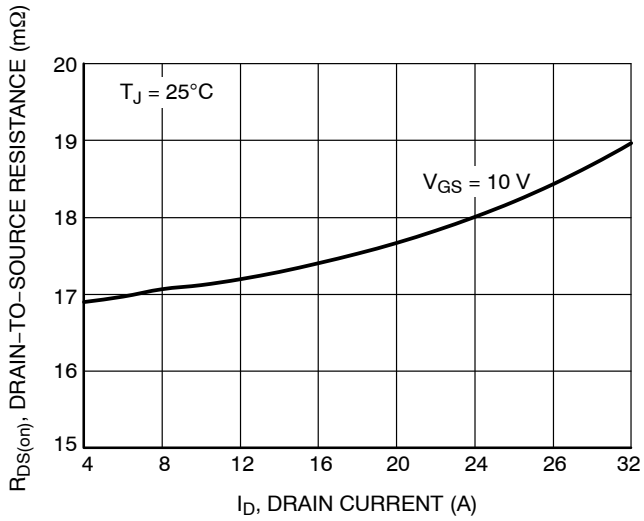


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

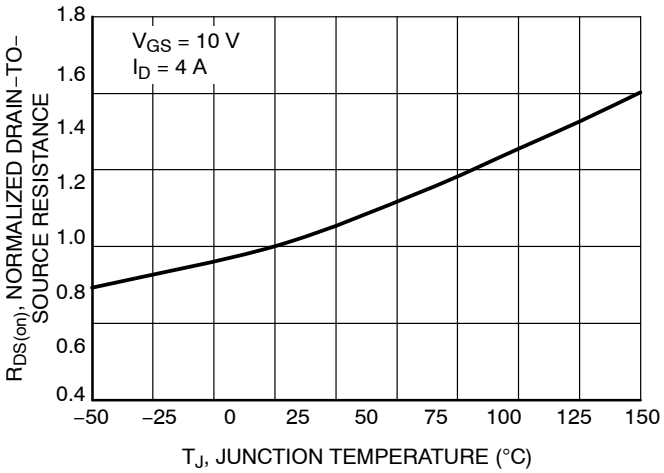


Figure 5. On−Resistance Variation with Temperature

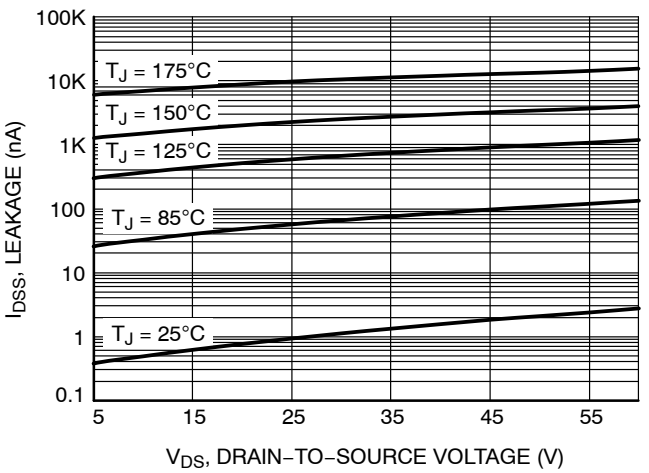


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

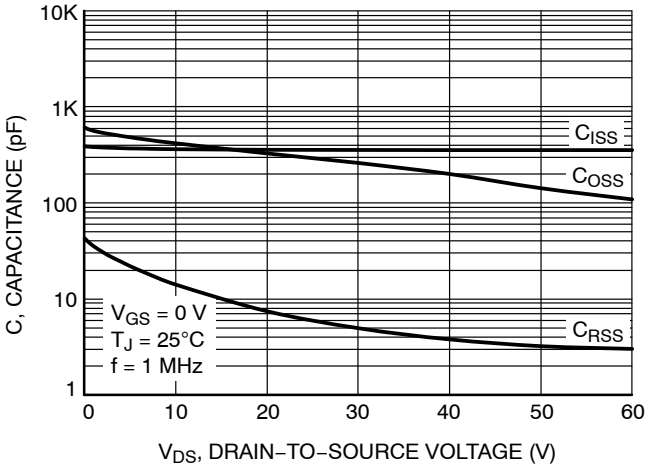


Figure 7. Capacitance Variation

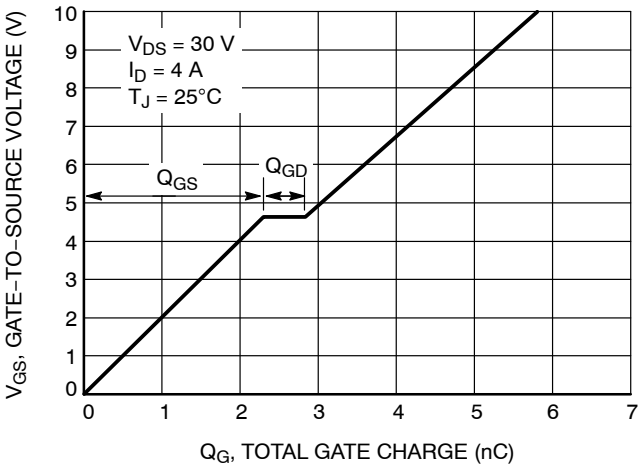


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

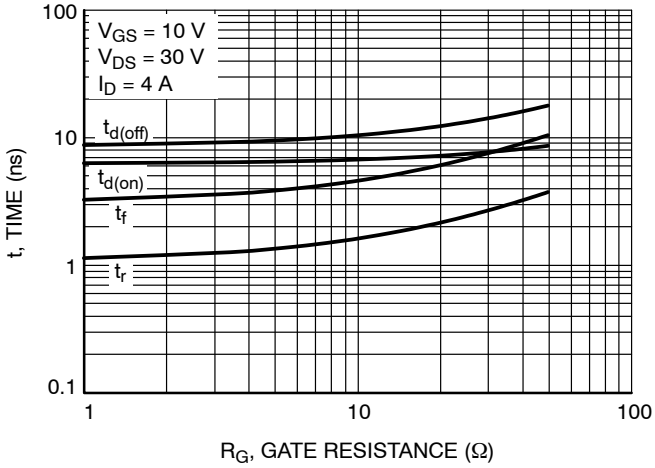


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

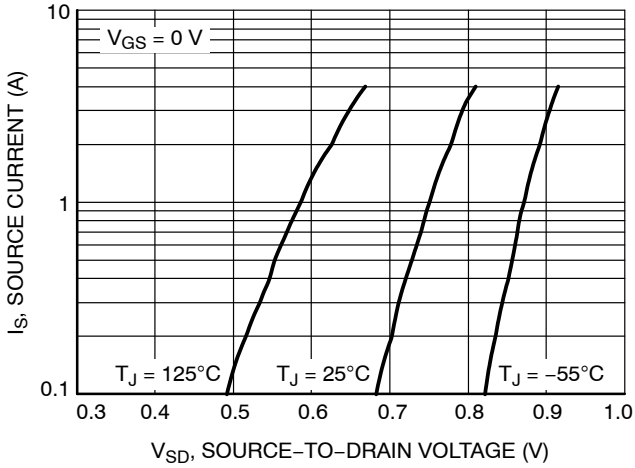


Figure 10. Diode Forward Voltage vs. Current

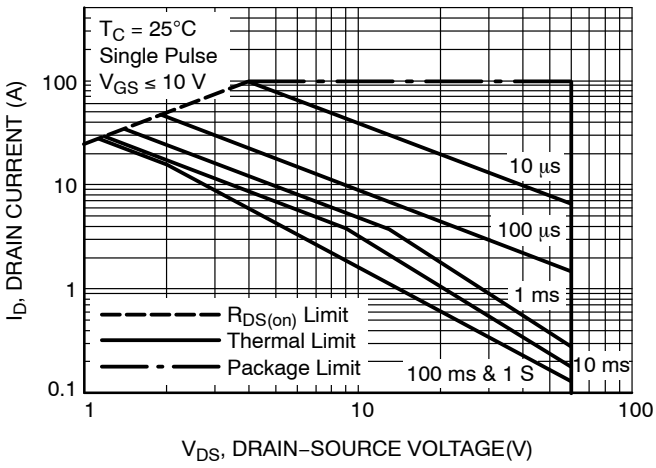


Figure 11. Safe Operating Area

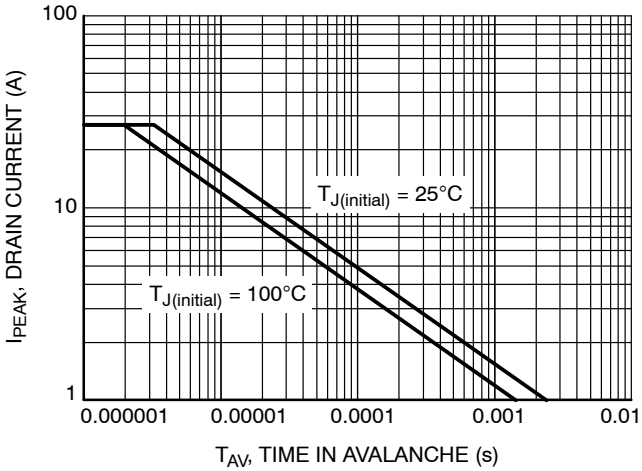


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

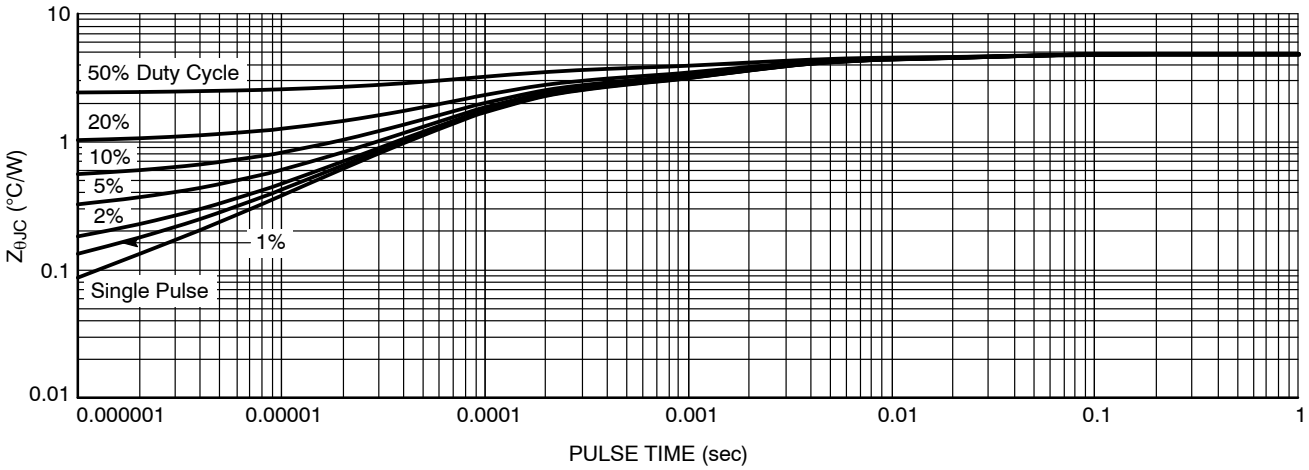
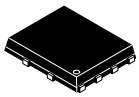


Figure 13. Thermal Response

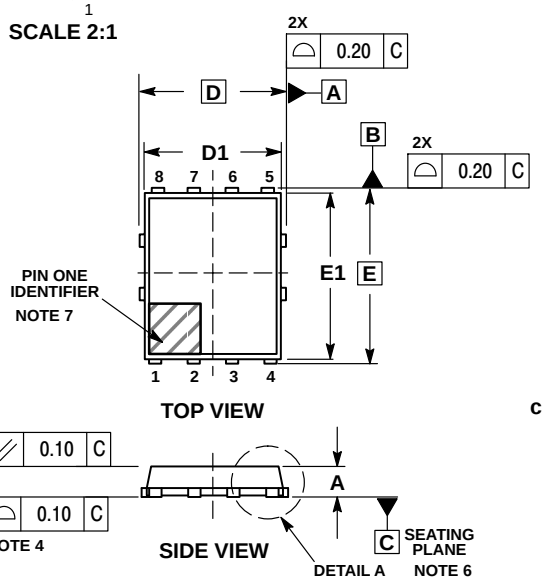
DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual)

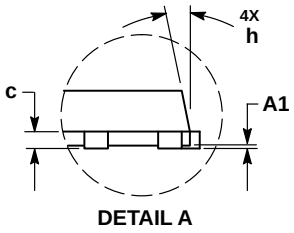
CASE 506BT
ISSUE F

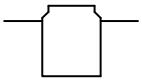
DATE 23 NOV 2021



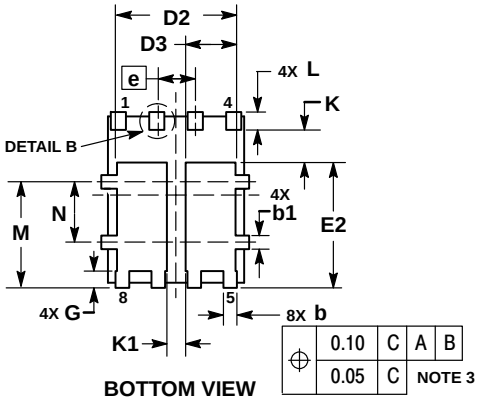
SCALE 2:1







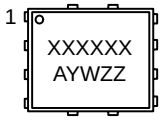
DETAIL B
ALTERNATE CONSTRUCTION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	–––	1.10
A1	–––	–––	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	–––	0.33
D		5.15 BSC	
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E		6.15 BSC	
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e		1.27 BSC	
G	0.45	0.55	0.65
h	–––	–––	12 °
K	0.51	–––	–––
K1	0.56	–––	–––
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

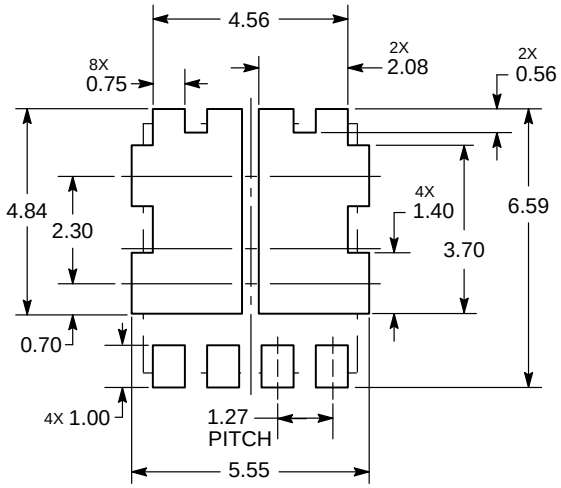
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL)**		**PAGE 1 OF 1**

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