

NTLUS3192PZ

Advance Information

Power MOSFET

–20 V, –4.2 A, μ Cool™ Single P-Channel, ESD, 1.6x1.6x0.55 mm UDFN Package

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6 x 1.6 x 0.55 mm for Board Space Saving
- Lowest RDS(on) in 1.6x1.6 Package
- ESD Protected
- This is a Halide Free Device
- This is a Pb-Free Device

Applications

- High Side Load Switch
- PA Switch and Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			V _{DSS}	–20	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	–3.4	A
		T _A = 85°C		–2.4	
	t ≤ 5 s	T _A = 25°C		–4.2	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.5	W
	t ≤ 5 s	T _A = 25°C		2.3	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	–2.2	A
		T _A = 85°C		–1.6	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.6	W
Pulsed Drain Current		t _p = 10 μs	I _{DM}	–17	A
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	–1.0	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T _L	260	°C
Gate-to-Source ESD Rating (HBM) per JESD22–A114F			ESD	1000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

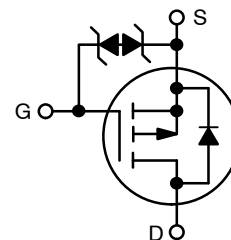


ON Semiconductor®

<http://onsemi.com>

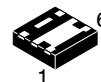
MOSFET

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
–20 V	85 mΩ @ –4.5 V	–3.0 A
	115 mΩ @ –2.5 V	–1.5 A
	160 mΩ @ –1.8 V	–0.5 A
	250 mΩ @ –1.5 V	–0.2 A

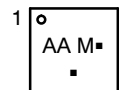


P-Channel MOSFET

MARKING DIAGRAM



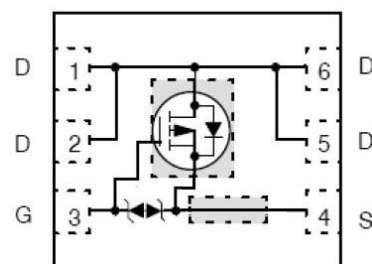
UDFN6
CASE 517AU
 μ COOL™



AA = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTLUS3192PZ

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	85	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	55	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	200	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
-----------	--------	----------------	-----	-----	-----	-------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\text{ }\mu\text{A}$, ref to 25°C		14		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$			-1.0	μA
					-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			10	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			2.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		65	85	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1.5\text{ A}$		90	115	
		$V_{GS} = -1.8\text{ V}, I_D = -0.5\text{ A}$		120	160	
		$V_{GS} = -1.5\text{ V}, I_D = -0.2\text{ A}$		160	250	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}, I_D = -0.2\text{ A}$		2.0		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -10\text{ V}$		450		pF
Output Capacitance	C_{OSS}			85		
Reverse Transfer Capacitance	C_{RSS}			65		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}; I_D = -3.0\text{ A}$		5.5	8.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.8		
Gate-to-Drain Charge	Q_{GD}			1.6		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -3.0\text{ A}, R_G = 1\text{ }\Omega$		26		ns
Rise Time	t_r			69		
Turn-Off Delay Time	$t_{d(OFF)}$			225		
Fall Time	t_f			200		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.72	1.2	V
			$T_J = 85^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$		11		ns	
Charge Time	t_a			8.0			
Discharge Time	t_b			3.0			
Reverse Recovery Charge	Q_{RR}			6.0		nC	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

5. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

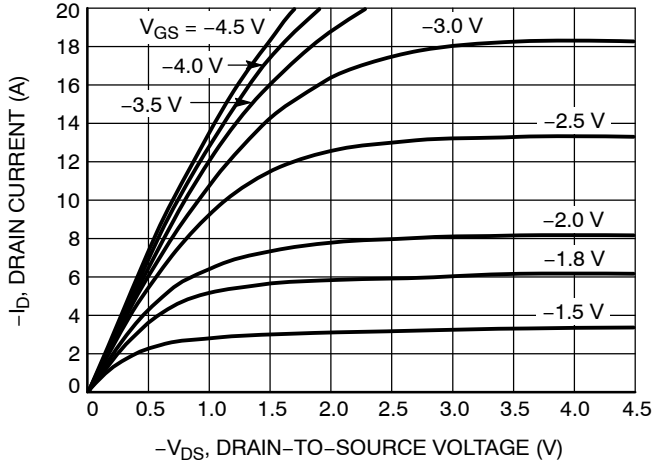


Figure 1. On-Region Characteristics

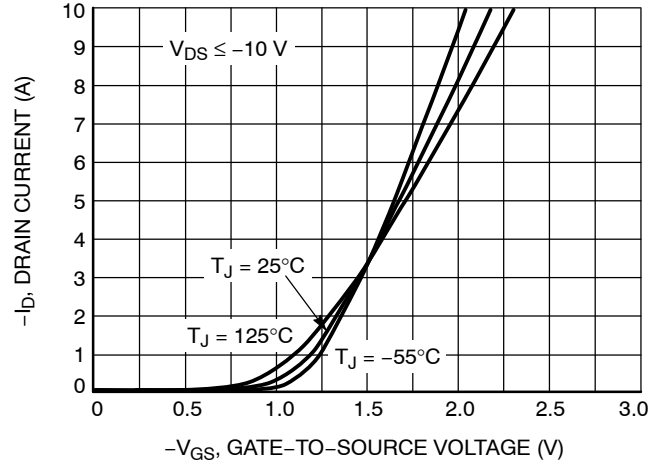


Figure 2. Transfer Characteristics

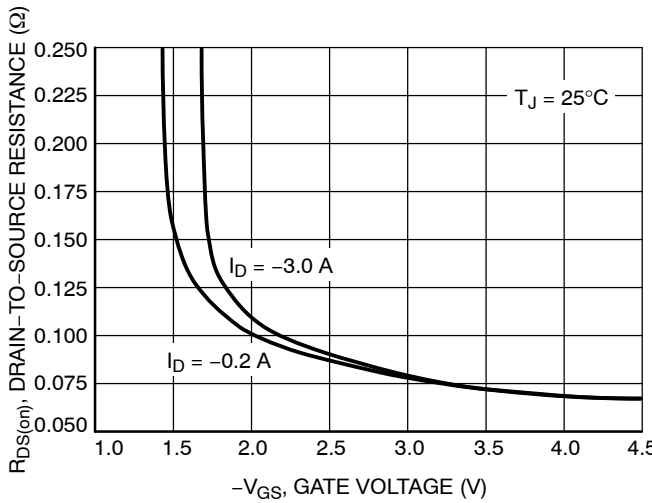


Figure 3. On-Resistance vs. Gate-to-Source Voltage

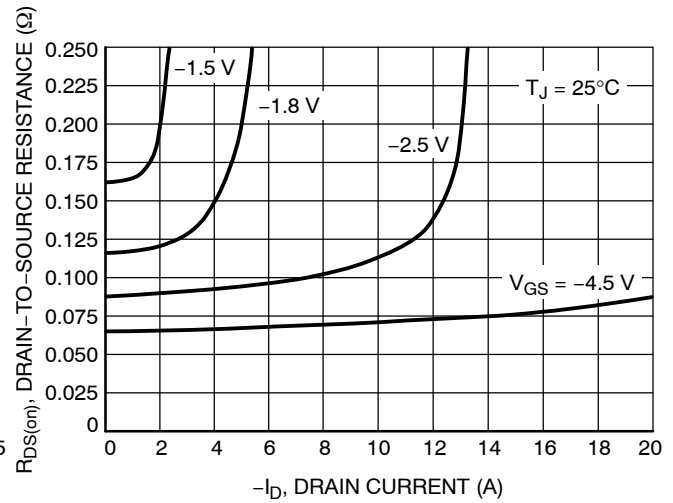


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

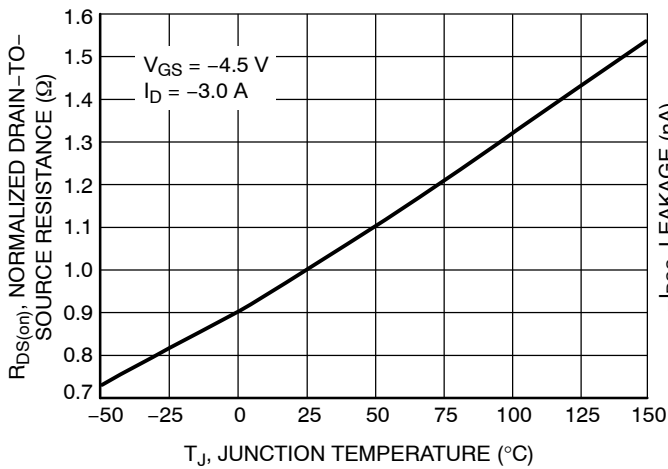


Figure 5. On-Resistance Variation with Temperature

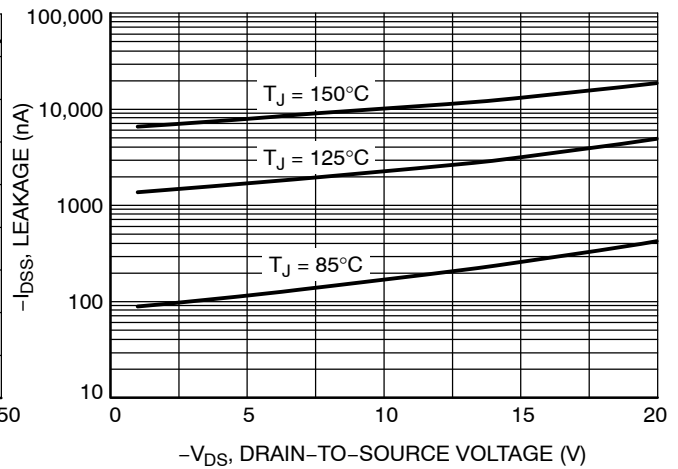


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

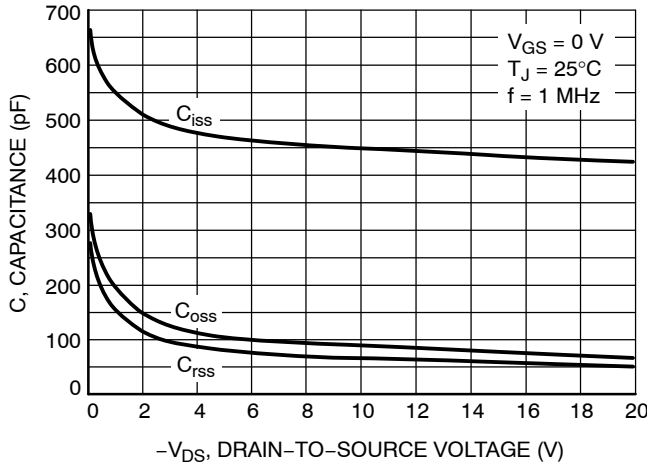


Figure 7. Capacitance Variation

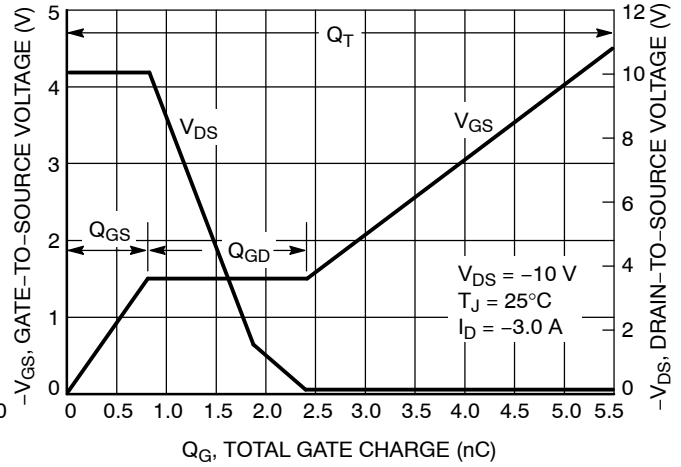


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

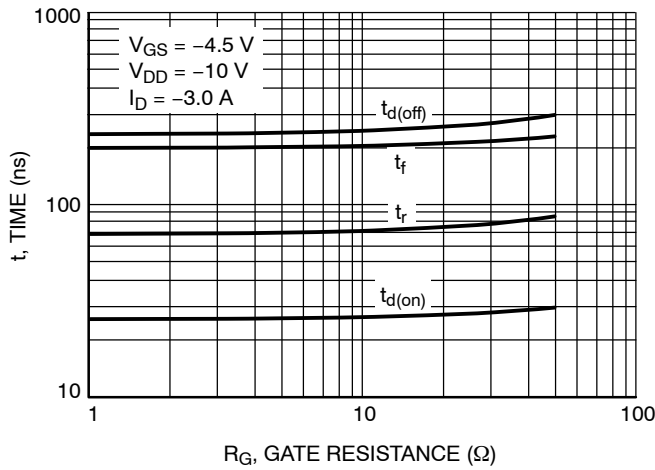


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

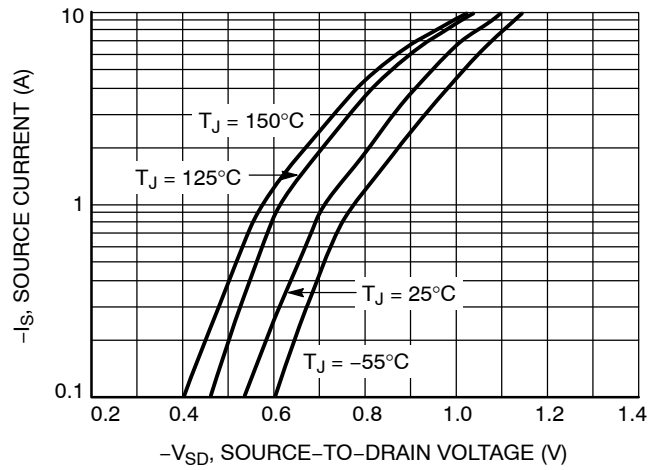


Figure 10. Diode Forward Voltage vs. Current

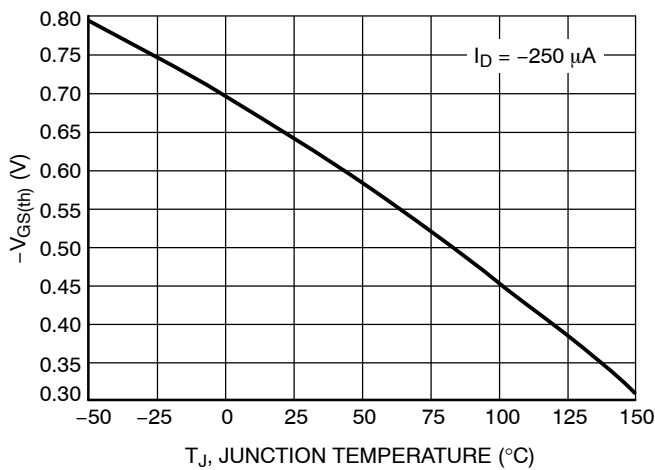


Figure 11. Threshold Voltage

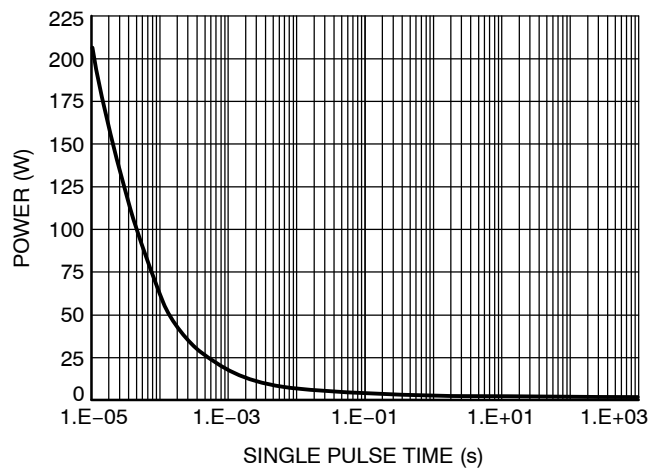


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

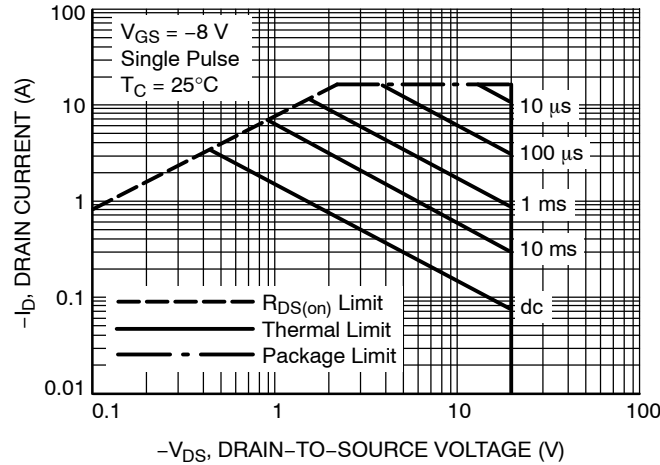


Figure 13. Maximum Rated Forward Biased Safe Operating Area

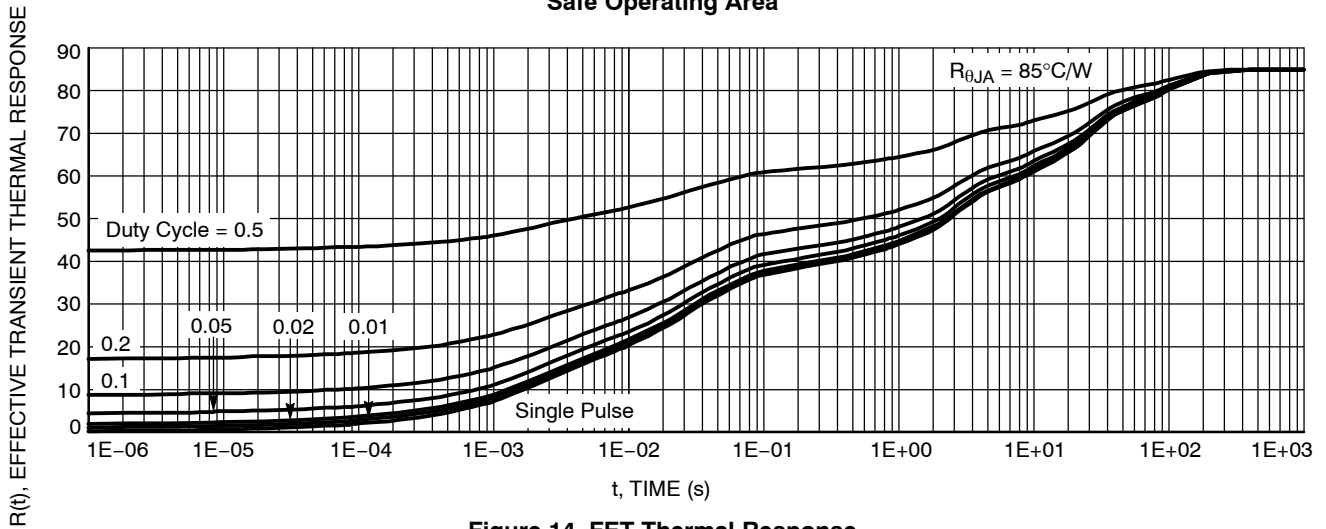


Figure 14. FET Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NTLUS3192PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3192PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

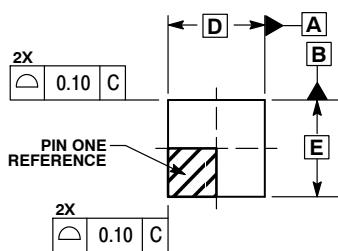
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



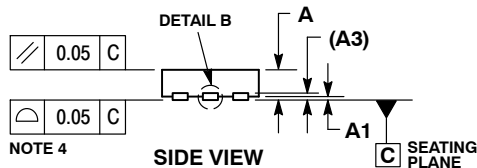
SCALE 4:1

UDFN6 1.6x1.6, 0.5P
CASE 517AU
ISSUE O

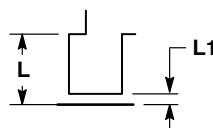
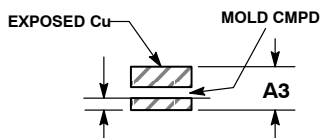
DATE 16 OCT 2008



TOP VIEW



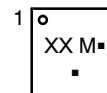
SIDE VIEW


DETAIL A
OPTIONAL
CONSTRUCTION

DETAIL B
OPTIONAL
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55	BSC
G	0.25	BSC
L	0.20	0.30
L1	---	0.15

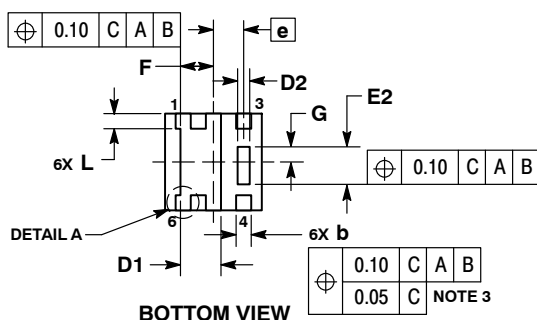
**GENERIC
MARKING DIAGRAM***


XX = Specific Device Code

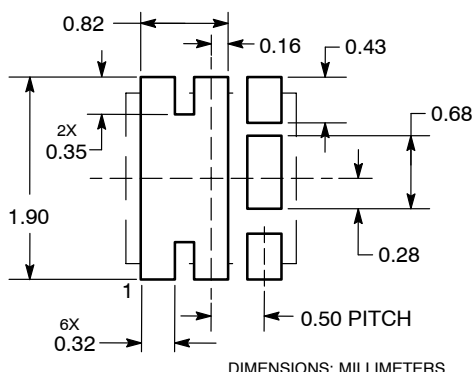
M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either loca-

tion)
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.


BOTTOM VIEW

**SOLDERMASK DEFINED
MOUNTING FOOTPRINT***


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON35147E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UDFN6 1.6x1.6, 0.5P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales