# NTLJD2105L

# Power MOSFET

## 8 V, 4.3 A, High Side Load Switch with Level Shift, 2x2 mm WDFN Package

### Features

- WDFN 2x2 mm Package with Exposed Drain Pads Offers Excellent Thermal Performance
- Low $R_{DS(on)}$ P−Channel Load Switch with N−channel MOSFET for Level Shift
- N Channel Operated at 1.5 V Gate Drive Voltage Level
- P Channel Operated at 1.5 V Supply Voltage
- Same Footprint as SC88
- Low Profile (<0.8 mm) Allows it to Fit Easily into Extremely Thin Environments
- ESD Protection
- These are Pb−Free Devices

### Applications

- High Slide Load Switch with Level Shift
- Optimized for Power Management in Ultra Portable Equipment

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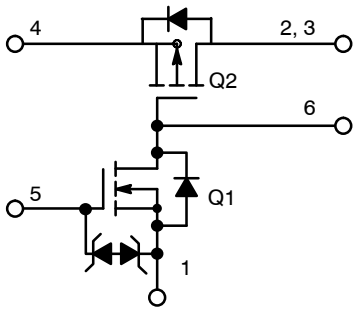
| $V_{INMAX}$ | $R_{DS(on)}$ MAX | $I_L$ MAX |
|---|---|---|
| 20 V | 50 mΩ @ 4.5 V | 4.3 A |
| | 60 mΩ @ 2.5 V | |
| | 80 mΩ @ 1.8 V | |
| | 115 mΩ @ 1.5 V | |



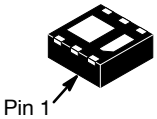

### MOSFET(Q2) MAXIMUM RATINGS

($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Q2 Input Voltage ($V_{DS}$, P−Channel) | | | $V_{IN}$ | 8 | V |
| Q1 On/Off Voltage ($V_{GS}$, N−Channel) | | | $V_{ON/OFF}$ | 6 | V |
| Continuous Load Current (Note 1) | Steady State | $T_A$ = 25°C | $I_L$ | 4.3 | A |
| | | $T_A$ = 85°C | | 3.1 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 1.56 | W |
| Continuous Load Current (Note 2) | Steady State | $T_A$ = 25°C | $I_L$ | 2.5 | A |
| | | $T_A$ = 85°C | | 1.8 | |
| Power Dissipation (Note 2) | | $T_A$ = 25°C | $P_D$ | 0.52 | W |
| Pulsed Load Current | $t_p$ = 10 μs | | $I_{LM}$ | 20 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) (Note 2) | | | $I_S$ | −2.7 | A |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size.

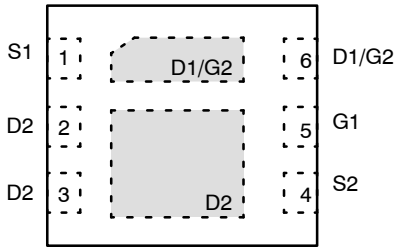



**WDFN6**
**CASE 506AZ**

**MARKING DIAGRAM**


JN = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

## THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 3) | $R_{\theta JA}$ | 80 | °C/W |
| Junction−to−Ambient − t ≤ 5 s (Note 3) | $R_{\theta JA}$ | 38 | °C/W |
| Junction−to−Ambient − Steady State Min Pad (Note 4) | $R_{\theta JA}$ | 180 | °C/W |

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface−mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Q2 Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | −8.0 | | | V |
| Q2 Forward Leakage Current | $I_{FL}$ | $V_{ON/OFF}$ = 0 V, $V_{IN}$ = 8.0 V | $T_J$ = 25°C | | | 0.1 | μA |
| | | | $T_J$ = 85°C | | | 1 | |
| Q1 Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS1}$ = ±6 V | | | | ±100 | nA |
| Q1 Diode Forward On−Voltage | $V_{SD}$ | $I_S$ = −1.0 A, $V_{GS1}$ = 0 V | | | −0.8 | −1.1 | V |
| **ON CHARACTERISTICS** | | | | | | | |
| Q1 ON/OFF Voltage | $V_{ON/OFF}$ | | | 1.5 | | 8.0 | |
| Q1 Gate Threshold Voltage | $V_{GS1(TH)}$ | $V_{GS1}$ = $V_{DS1}$, $I_D$ = 250 μA | | 0.40 | | 1.0 | V |
| Q2 Input Voltage | $V_{IN}$ | | | 1.8 | | 8.0 | V |
| Q2 Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{IN}$ = 4.5 V, $I_L$ = 4.0 A | | | 33 | 50 | mΩ |
| | | $V_{IN}$ = 2.5 V, $I_L$ = 3.0 A | | | 40 | 60 | |
| | | $V_{IN}$ = 1.8 V, $I_L$ = 1.7 A | | | 60 | 80 | |
| | | $V_{IN}$ = 1.5 V, $I_L$ = 1.2 A | | | 75 | 115 | |
| Q2 Load Current | $I_L$ | $V_{DROP}$ ≤ 0.2 V, $V_{IN}$ = 2.5 V, $V_{ON/OFF}$ = 1.5 V | | 1.0 | | | A |
| | | $V_{DROP}$ ≤ 0.3 V, $V_{IN}$ = 1.8 V, $V_{ON/OFF}$ = 1.5 V | | 1.0 | | | |

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

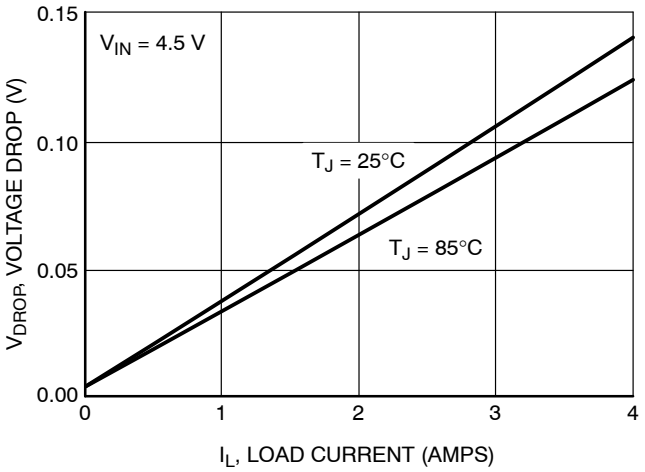



**Figure 1. Voltage Drop versus Load Current @ $V_{IN}$ = 4.5 V**

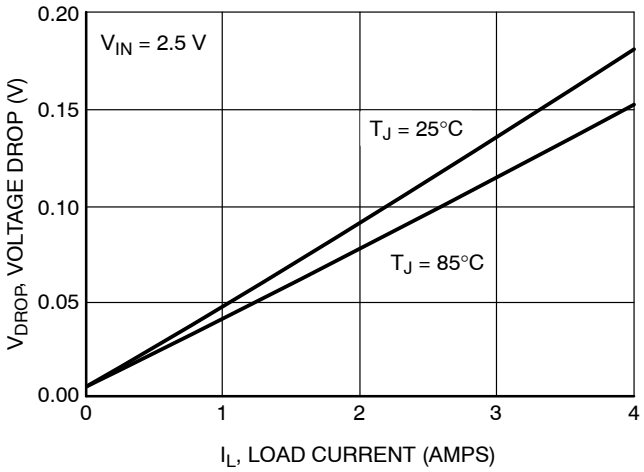



**Figure 2. Voltage Drop versus Load Current @ $V_{IN}$ = 2.5 V**

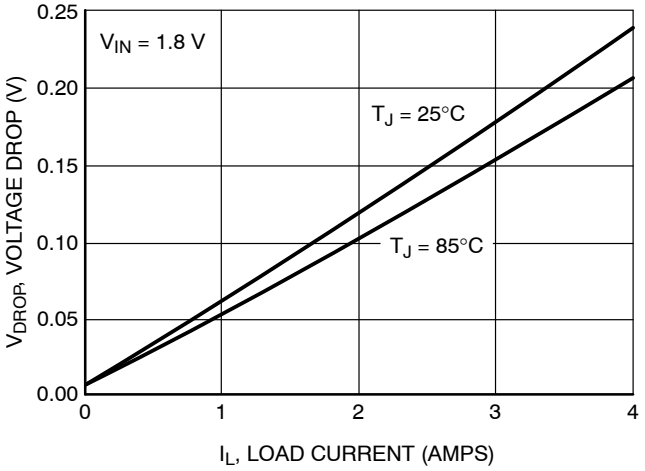



**Figure 3. Voltage Drop versus Load Current @ $V_{IN}$ = 1.8 V**

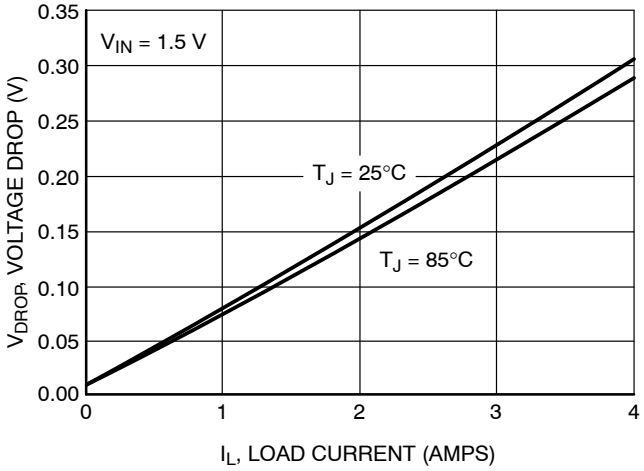



**Figure 4. Voltage Drop versus Load Current @ $V_{IN}$ = 1.5 V**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

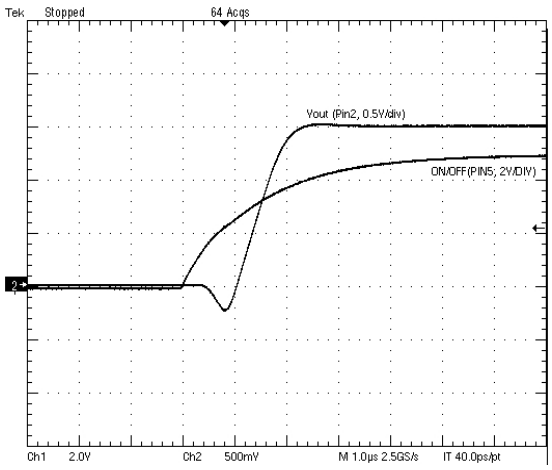



**Figure 5. Turn−on**
**($V_{in}$ = 1.5 V, $R_L$ = 3 Ω, R1 = 1 kΩ, R2 = 0, C1 = 47 nF)**

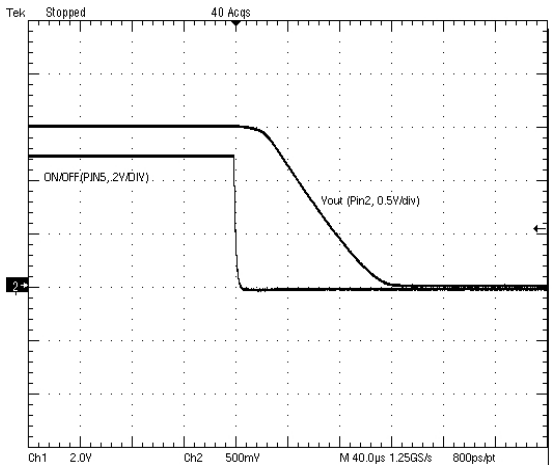



**Figure 6. Turn−off**
**($V_{in}$ = 1.5 V, $R_L$ = 3 Ω, R1 = 1 kΩ, R2 = 0, C1 = 47 nF)**

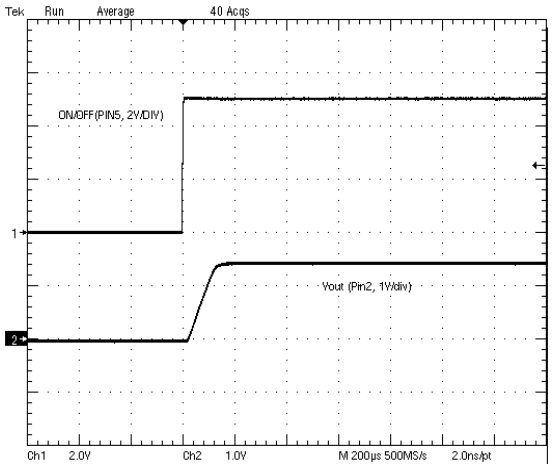



**Figure 7. Turn−on**
**($V_{in}$ = 1.5 V, $R_L$ = 3 Ω, R1 = 10 kΩ, R2 = 1 kΩ, C1 = 47 nF)**

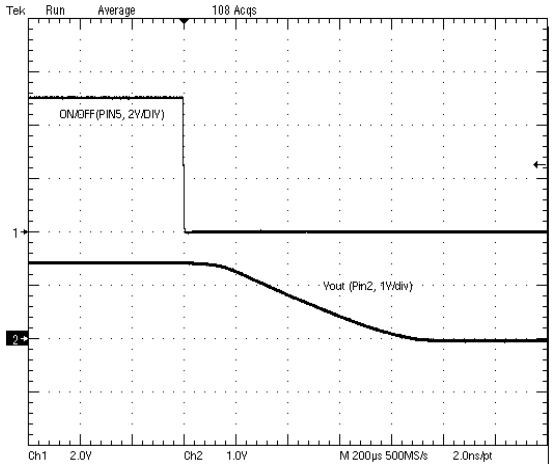



**Figure 8. Turn−off**
**($V_{in}$ = 1.5 V, $R_L$ = 3 Ω, R1 = 10 kΩ, R2 = 1 kΩ, C1 = 47 nF)**

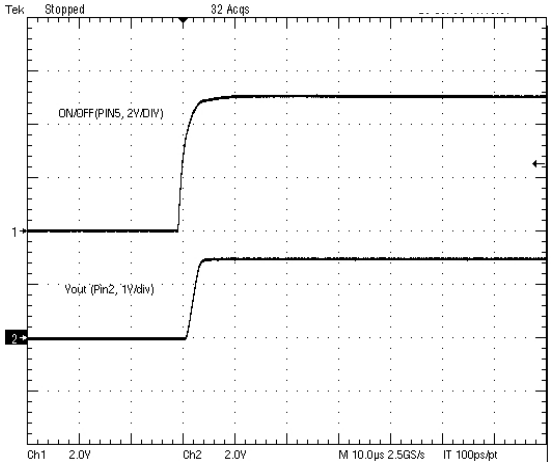



**Figure 9. Turn−on**
**($V_{in}$ = 3 V, $R_L$ = 3 Ω, R1 = 10 kΩ, R2 = 1 kΩ, C1 = 47 nF)**

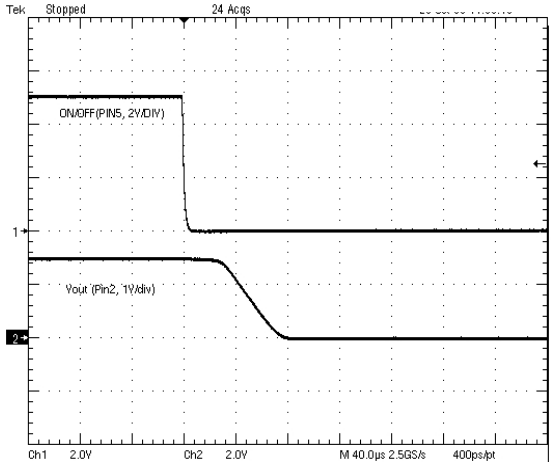



**Figure 10. Turn−off**
**($V_{in}$ = 3 V, $R_L$ = 3 Ω, R1 = 10 kΩ, R2 = 1 kΩ, C1 = 47 nF)**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

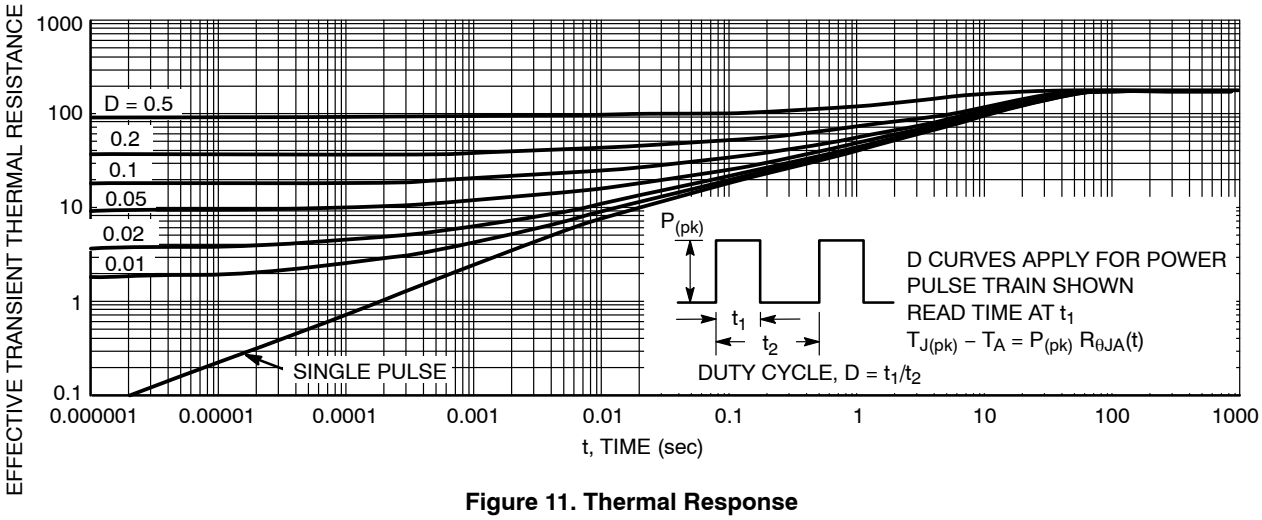



**Figure 11. Thermal Response**

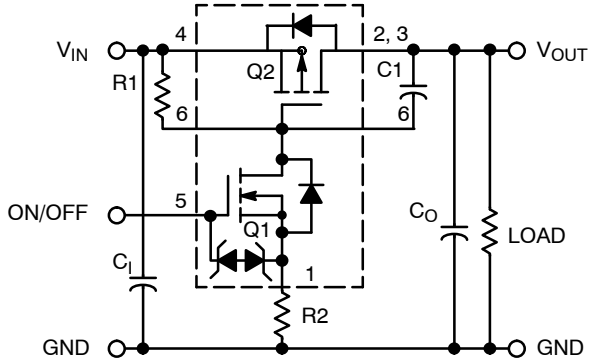



**Figure 12. Load Switch Application**

| Components | Description | Value |
|---|---|---|
| R1 | Pull−up Resistor | Typical 10 kΩ to 1.0 MΩ* |
| R2 | Optional Slew−Rate Control | Typical 0 kΩ to 100 kΩ* |
| $C_O$, $C_I$ | Output Capacitance | Usually < 1.0 μF |
| C1 | Optional In−Rush Current Control | Typical ≤ 1000 pF |

*Minimum R1 value should be at least 10 x R2 to ensure Q1 turn−on.

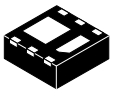
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTLJD2105LTBG | WDFN6<br>(Pb−Free) | 3000 / Tape & Reel |

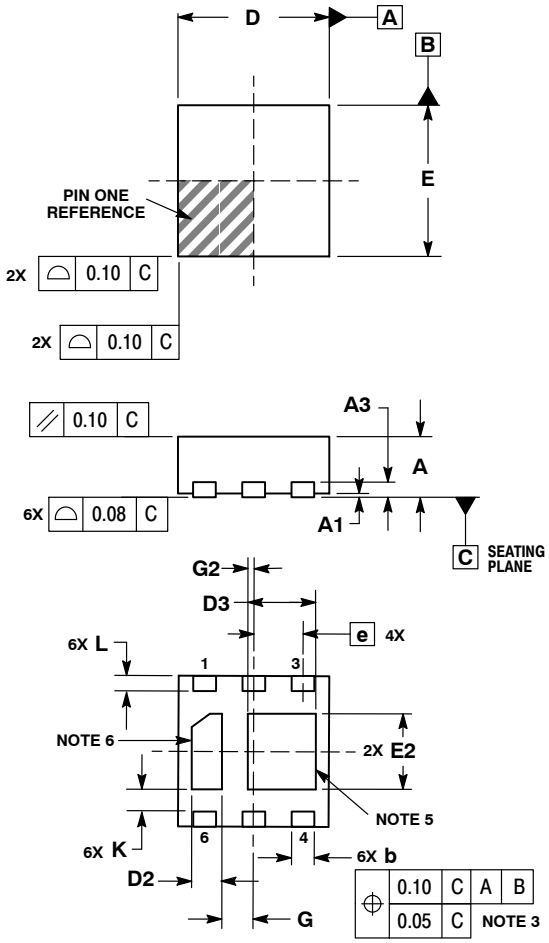
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**WDFN6, 2x2**
CASE 506AZ
ISSUE A

DATE 25 APR 2006



**SCALE 4:1**




**BOTTOM VIEW**

STYLE 1:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. PINS 2 & 3 CONNECTED TO LARGE FLAG.
2. PIN 6 CONNECTED TO SMALL FLAG.

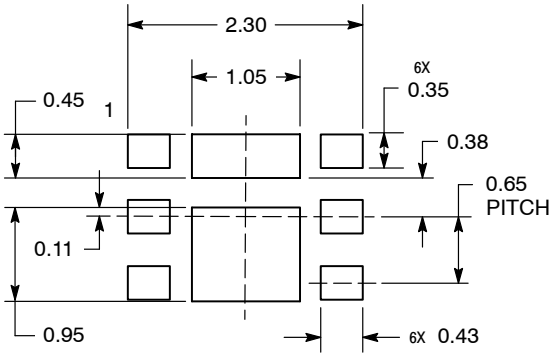
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 2.00 BSC | |
| D2 | 0.30 | 0.50 |
| D3 | 0.80 | 1.00 |
| E | 2.00 BSC | |
| E2 | 0.90 | 1.10 |
| e | 0.65 BSC | |
| G | 0.41 REF | |
| G2 | 0.085 REF | |
| K | 0.25 REF | |
| L | 0.20 | 0.30 |

## GENERIC MARKING DIAGRAM*


XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

## SOLDERMASK DEFINED MOUNTING FOOTPRINT




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON22362D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **6 PIN WDFN 2X2, 0.65P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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