

# NTK3142P

## Small Signal MOSFET

–20 V, –280 mA, P–Channel with ESD Protection, SOT–723

### Features

- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC–89 and 38% Thinner than SC–89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, 1.8 V  $R_{DS(on)}$  Rating
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology.
- This is a Pb–Free Device

### Applications

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDA's

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		$V_{DSS}$	–20	V
Gate–to–Source Voltage		$V_{GS}$	$\pm 8.0$	V
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	–260
			$T_A = 85^\circ\text{C}$	–185
			$T_A = 25^\circ\text{C}$	–280
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	400
			$t \leq 5 \text{ s}$	500
Continuous Drain Current (Note 2)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	–215
			$T_A = 85^\circ\text{C}$	–155
Power Dissipation (Note 2)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	280
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	–310	mA
Operating Junction and Storage Temperature		$T_J, T_{STG}$	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode) (Note 2)		$I_S$	–240	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface–mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface–mounted on FR4 board using the minimum recommended pad size.

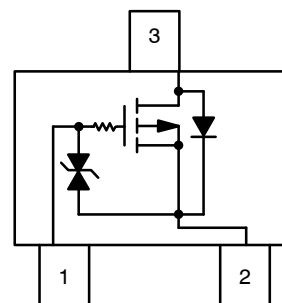


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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ Max
–20 V	2.7 $\Omega$ @ –4.5 V	–280 mA
	4.1 $\Omega$ @ –2.5 V	
	6.1 $\Omega$ @ –1.8 V	

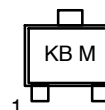
### SOT–723 (3–LEAD)



Top View  
1 – Gate  
2 – Source  
3 – Drain

### MARKING DIAGRAM

  
CASE 631AA  
SOT–723



KB = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTK3142PT1G	SOT–723 (Pb–Free)	4000/Tape & Reel 4 mm Pitch
NTK3142PT5G	SOT–723 (Pb–Free)	8000/Tape & Reel 2 mm Pitch

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	315	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	250	
Junction-to-Ambient – Steady State Minimum Pad (Note 4)	$R_{\theta JA}$	440	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)  
 4. Surface-mounted on FR4 board using the minimum recommended pad size.

**MOSFET ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -100\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -100\text{ }\mu\text{A}$ , Reference to $25^\circ\text{C}$		14		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	$\mu\text{A}$
					-2.0	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			$\pm 1$	$\mu\text{A}$

**ON CHARACTERISTICS** (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1.3	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-2.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -260\text{ mA}$		2.9	4.0	$\Omega$
Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -10\text{ mA}$		2.7	3.4	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ mA}$		4.1	5.3	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ mA}$		6.1	10	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5\text{ V}, I_D = -10\text{ mA}$		73		mS

**CAPACITANCES**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -10\text{ V}$		15.3		pF
Output Capacitance	$C_{OSS}$			4.3		
Reverse Transfer Capacitance	$C_{RSS}$			2.3		

**SWITCHING CHARACTERISTICS,  $V_{GS} = 4.5\text{ V}$**  (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -5\text{ V}, I_D = -100\text{ mA}, R_G = 6\text{ }\Omega$		8.4	16	ns
Rise Time	$t_r$			15.3	28	
Turn-Off Delay Time	$t_{d(OFF)}$			37.5	80	
Fall Time	$t_f$			22.7	43	

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = -10\text{ mA}$	$T_J = 25^\circ\text{C}$	0.69	-1.2	V
			$T_J = 125^\circ\text{C}$	0.56		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, V_{DD} = -20\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$		37	80	ns
Charge Time	$t_a$			15.9	30	
Discharge Time	$t_b$			21.1	50	
Reverse Recovery Charge	$Q_{RR}$			20	70	nC

5. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

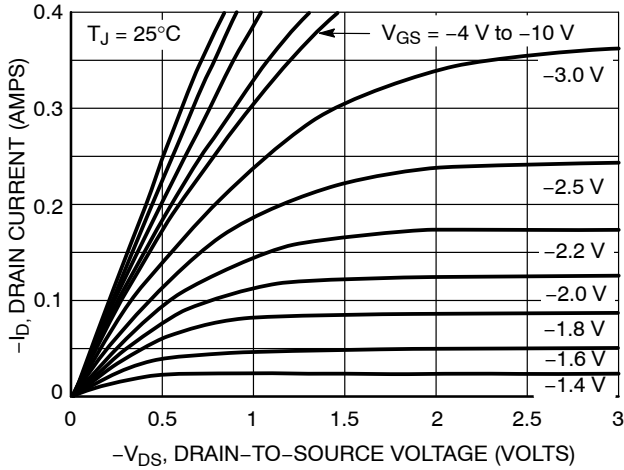


Figure 1. On-Region Characteristics

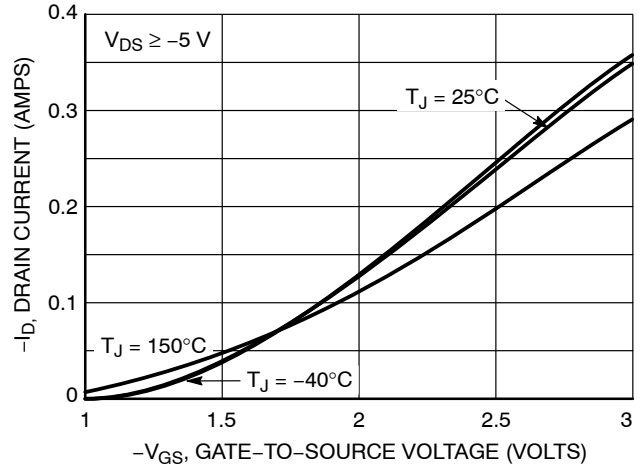


Figure 2. Transfer Characteristics

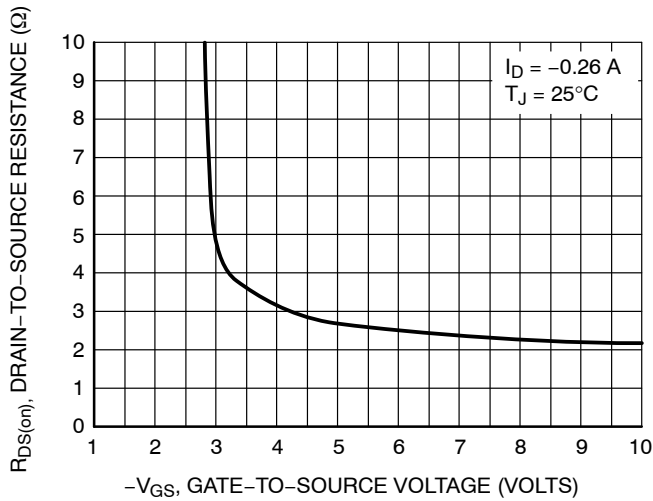


Figure 3. On-Resistance vs. Gate-to-Source Voltage

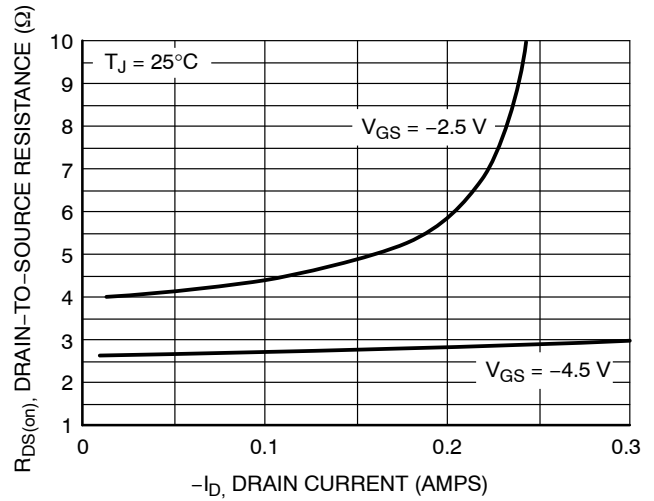


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

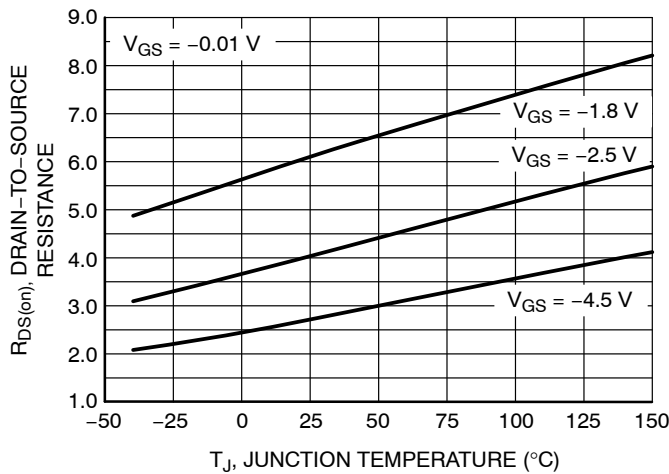


Figure 5. On-Resistance Variation with Temperature

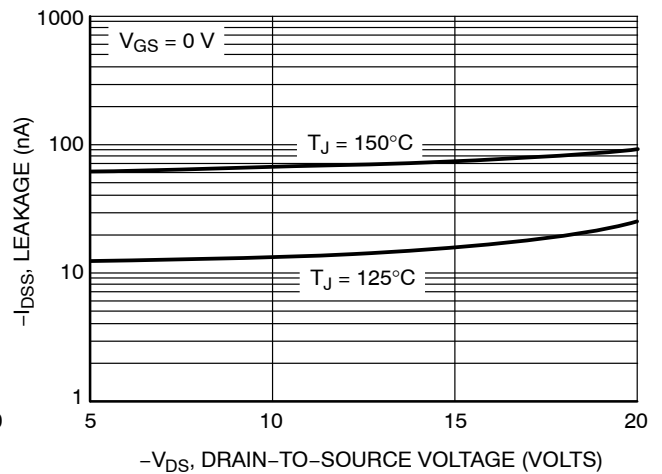


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

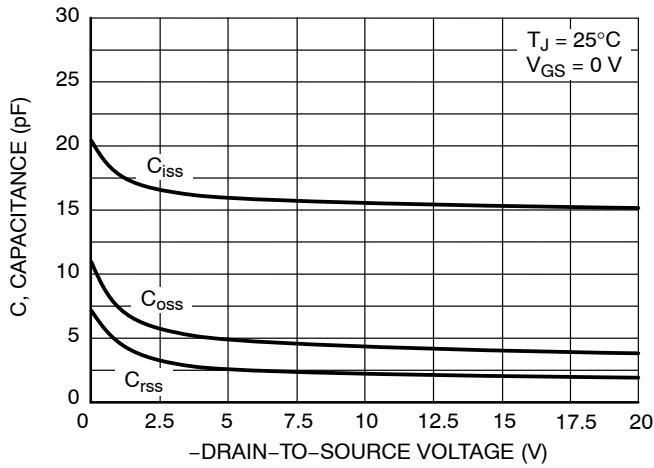


Figure 7. Capacitance Variation

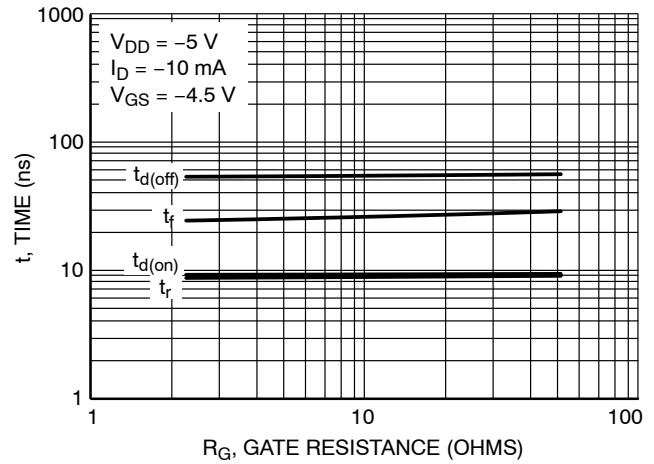


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

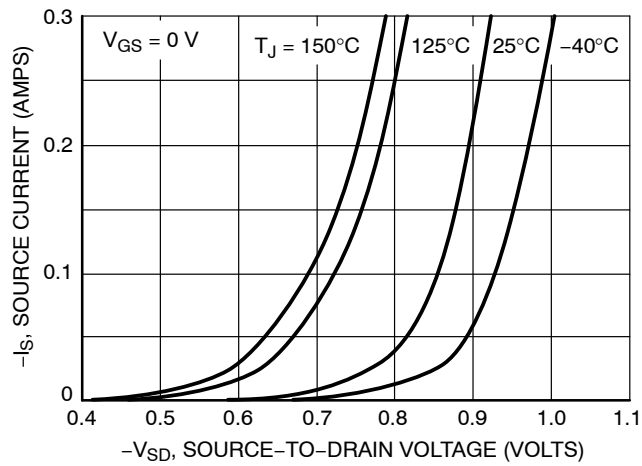


Figure 9. Diode Forward Voltage vs. Current



**SOT-723 1.20x0.80x0.50, 0.40P**  
**CASE 631AA**  
**ISSUE E**

DATE 24 JAN 2024

NOTES:

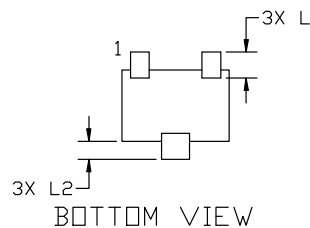
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



TOP VIEW



SIDE VIEW



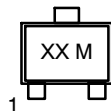
BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
c	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25



RECOMMENDED MOUNTING  
FOOTPRINT

**GENERIC  
MARKING DIAGRAM\***



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLE 1: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 2: PIN 1. ANODE 2. N/C 3. CATHODE	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. GATE 2. SOURCE 3. DRAIN
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