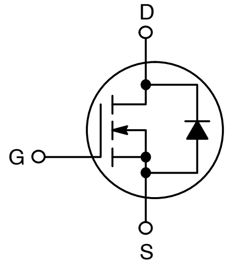
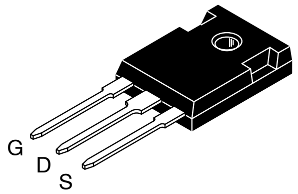
Silicon Carbide (SiC) MOSFET – 32 mohm, 650 V, M2, TO-247-3L

NTHL045N065SC1

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
650 V	50 mΩ @ 18 V	66 A

N−CHANNEL MOSFET





TO−247−3LD
CASE 340CX

Features

- Typ. $R_{DS(on)}$ = 32 mΩ @ V_{GS} = 18 V
  Typ. $R_{DS(on)}$ = 42 mΩ @ V_{GS} = 15 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 105 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 162 pF)
- 100% Avalanche Tested
- T_J < 175°C
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

- SMPS (Switching Mode Power Supplies)
- Solar Inverters
- UPS (Uninterruptable Power Supplies)
- Energy Storages

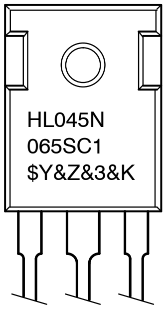
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	650	V
Gate−to−Source Voltage			V_{GS}	−8/+22	V
Recommended Operation Values of Gate−to−Source Voltage		T_C < 175°C	V_{GSop}	−5/+18	V
Continuous Drain Current (Note 1)	Steady State	T_C = 25°C	I_D	66	A
Power Dissipation (Note 1)			P_D	291	W
Continuous Drain Current (Note 1)	Steady State	T_C = 100°C	I_D	46	A
Power Dissipation (Note 1)			P_D	145	W
Pulsed Drain Current (Note 2)	T_C = 25°C		I_{DM}	191	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	75	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 12 A, L = 1 mH) (Note 3)			E_{AS}	72	mJ
Maximum Lead Temperature for Soldering (1/8″ from case for 5 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Repetitive rating, limited by max junction temperature.
3. EAS of 72 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 12 A, V_{DD} = 50 V, V_{GS} = 18 V.

MARKING DIAGRAM



HL045N065SC1 = Specific Device Code
$Y = **onsemi** Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot

ORDERING INFORMATION

Device	Package	Shipping
NTHL045N065SC1	TO−247 Long Lead	30 Units / Tube

December, 2023 − Rev. 5

Publication Order Number:
NTHL045N065SC1/D

Table 1. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	0.52	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	40	

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	650	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 20 mA, referenced to 25°C	–	0.15	–	V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V; T_J = 25°C	–	–	10	μA
		T_J = 175°C	–	–	1	mA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +22/−8 V, V_{DS} = 0 V	–	–	250	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 8 mA	1.8	2.8	4.3	V
Recommended Gate Voltage	V_{GOP}		−5	–	+18	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 15 V, I_D = 25 A, T_J = 25°C	–	42	–	mΩ
		V_{GS} = 18 V, I_D = 25 A, T_J = 25°C	–	32	50	
		V_{GS} = 18 V, I_D = 25 A, T_J = 175°C	–	42	–	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 25 A	–	14	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 325 V	–	1870	–	pF
Output Capacitance	C_{OSS}		–	162	–	
Reverse Transfer Capacitance	C_{RSS}		–	14	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/18 V, V_{DS} = 520 V, I_D = 25 A	–	105	–	nC
Gate−to−Source Charge	Q_{GS}		–	27	–	
Gate−to−Drain Charge	Q_{GD}		–	30	–	
Gate−Resistance	R_G	f = 1 MHz	–	3.1	–	Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5/18 V, V_{DS} = 400 V, I_D = 25 A, R_G = 2.2 Ω Inductive load	–	14	–	ns
Rise Time	t_r		–	30	–	
Turn−Off Delay Time	$t_{d(OFF)}$		–	26	–	
Fall Time	t_f		–	7	–	
Turn−On Switching Loss	E_{ON}		–	198	–	μJ
Turn−Off Switching Loss	E_{OFF}		–	28	–	
Total Switching Loss	E_{tot}		–	226	–	
DRAIN−SOURCE DIODE CHARACTERISTICS						
Continuous Drain−Source Diode Forward Current	I_{SD}	V_{GS} = −5 V, T_J = 25°C	–	–	75	A
Pulsed Drain−Source Diode Forward Current (Note 2)	I_{SDM}		–	–	191	
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 25 A, T_J = 25°C	–	4.4	–	V

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = −5/18 V, I_{SD} = 25 A, dI_S/dt = 1000 A/μs	–	19	–	ns
Reverse Recovery Charge	Q_{RR}		–	99	–	nC
Reverse Recovery Energy	E_{REC}		–	3.5	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	10	–	A
Charge Time	Ta		–	11	–	ns
Discharge Time	Tb		–	8.4	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

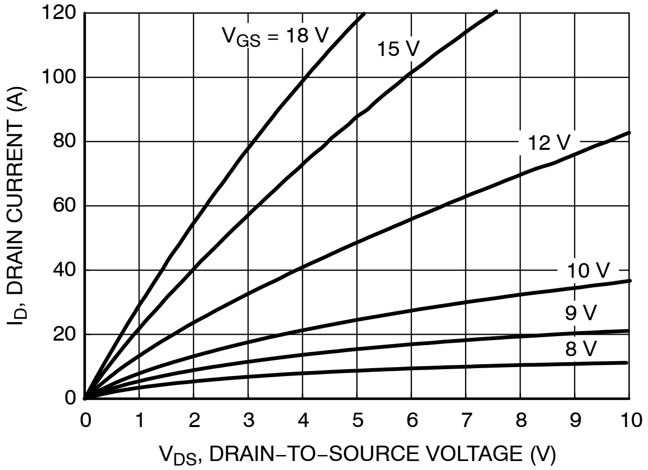


Figure 1. On−Region Characteristics

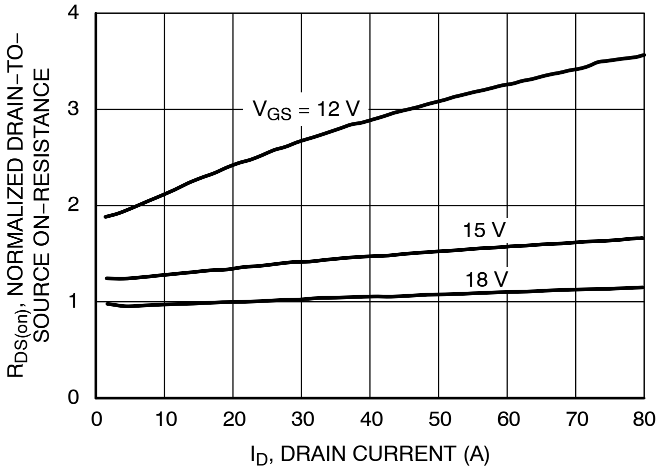


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

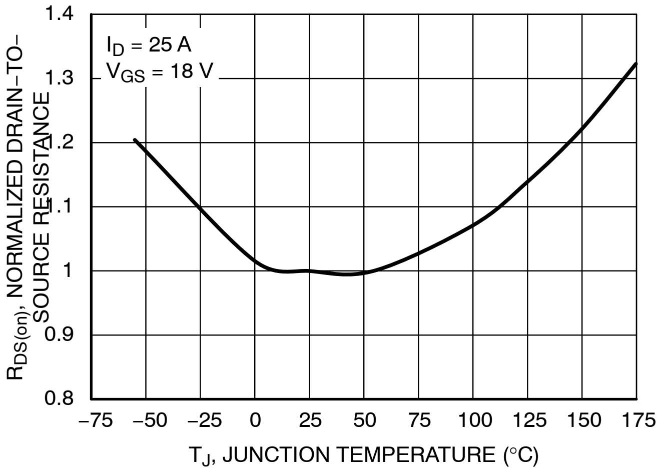


Figure 3. On−Resistance Variation with Temperature

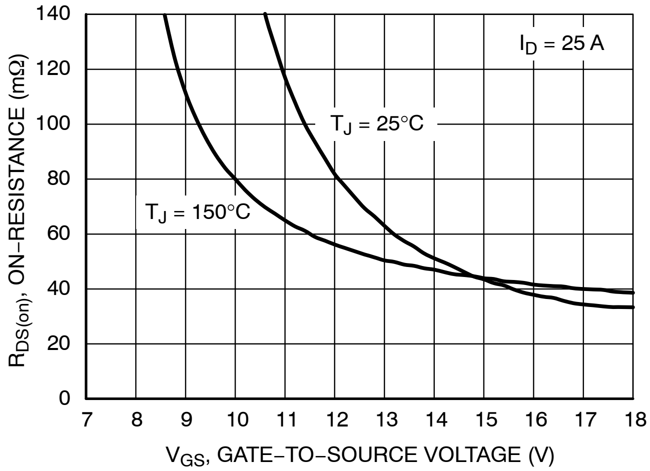


Figure 4. On−Resistance vs. Gate−to−Source Voltage

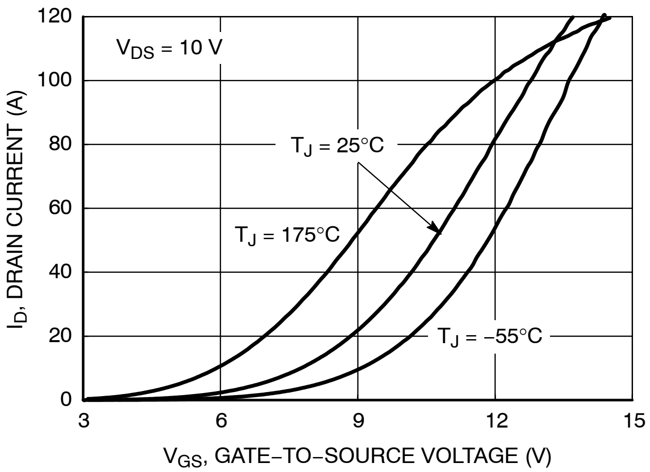


Figure 5. Transfer Characteristics

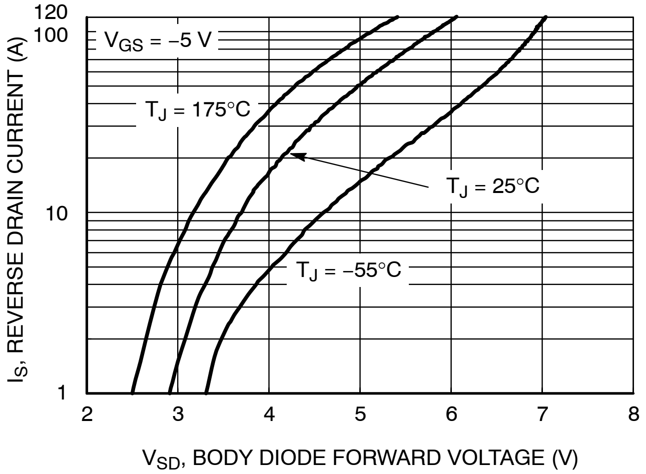


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

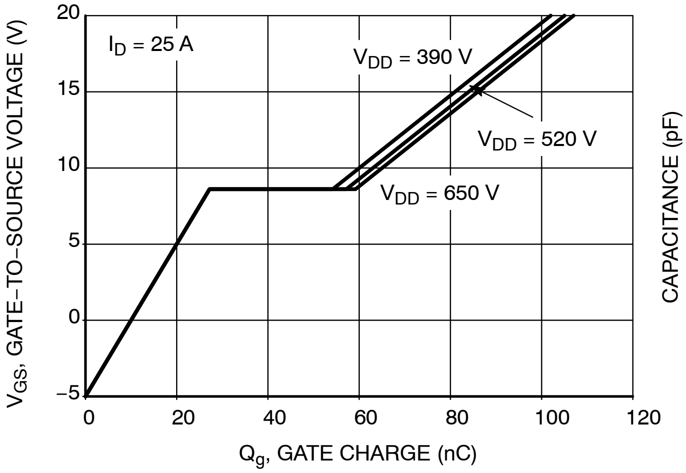


Figure 7. Gate−to−Source Voltage vs. Total Charge

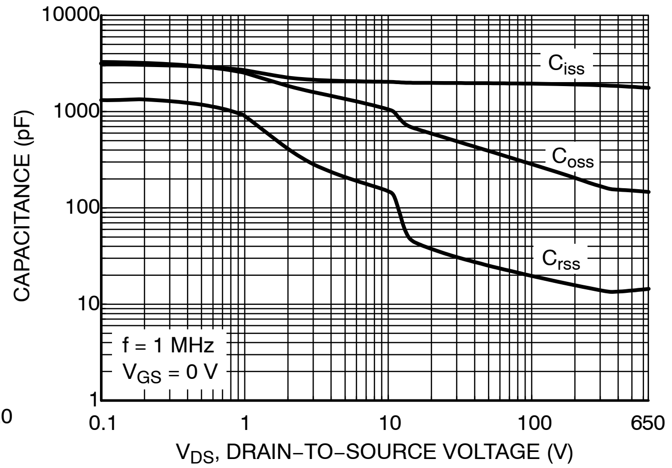


Figure 8. Capacitance vs. Drain−to−Source Voltage

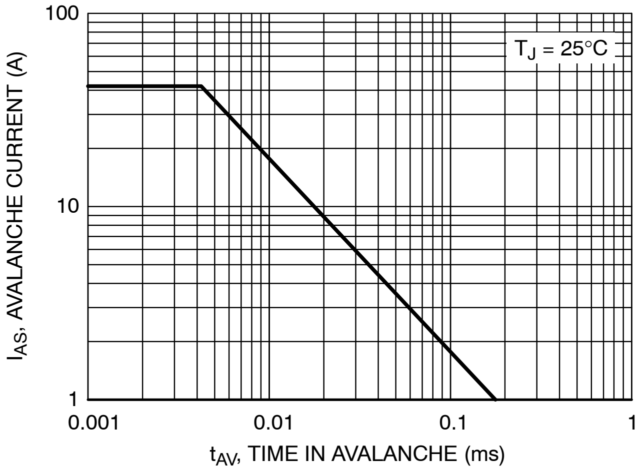


Figure 9. Unclamped Inductive Switching Capability

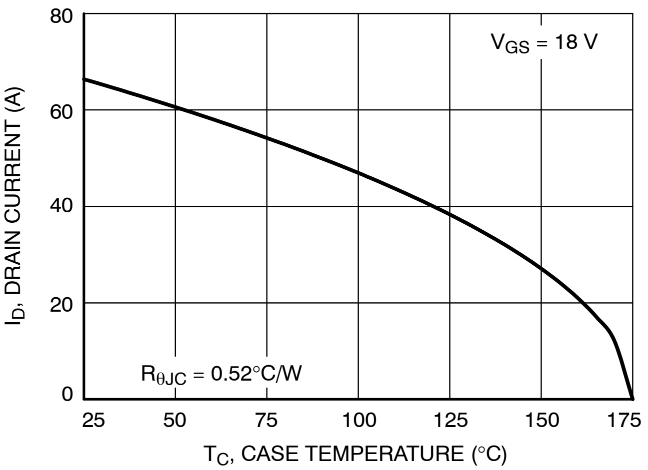


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

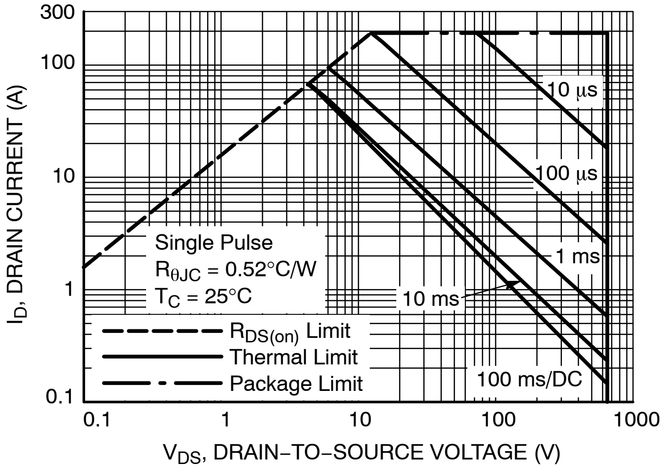


Figure 11. Safe Operating Area

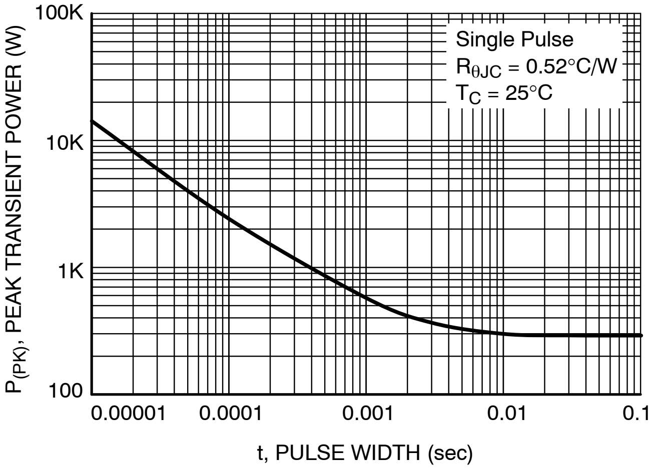


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

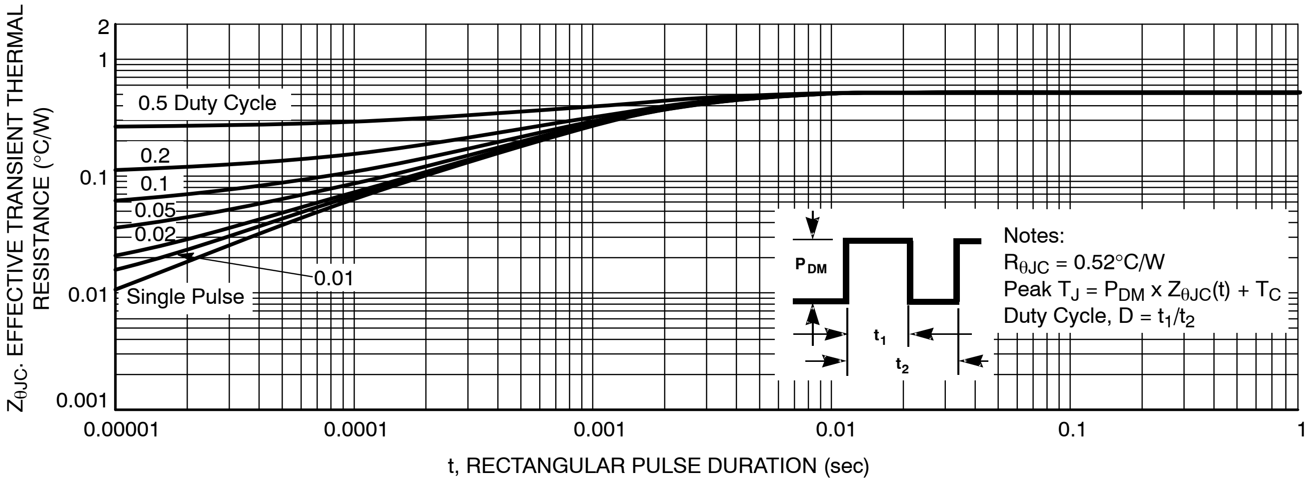
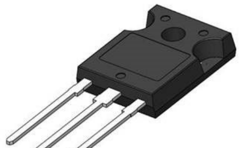


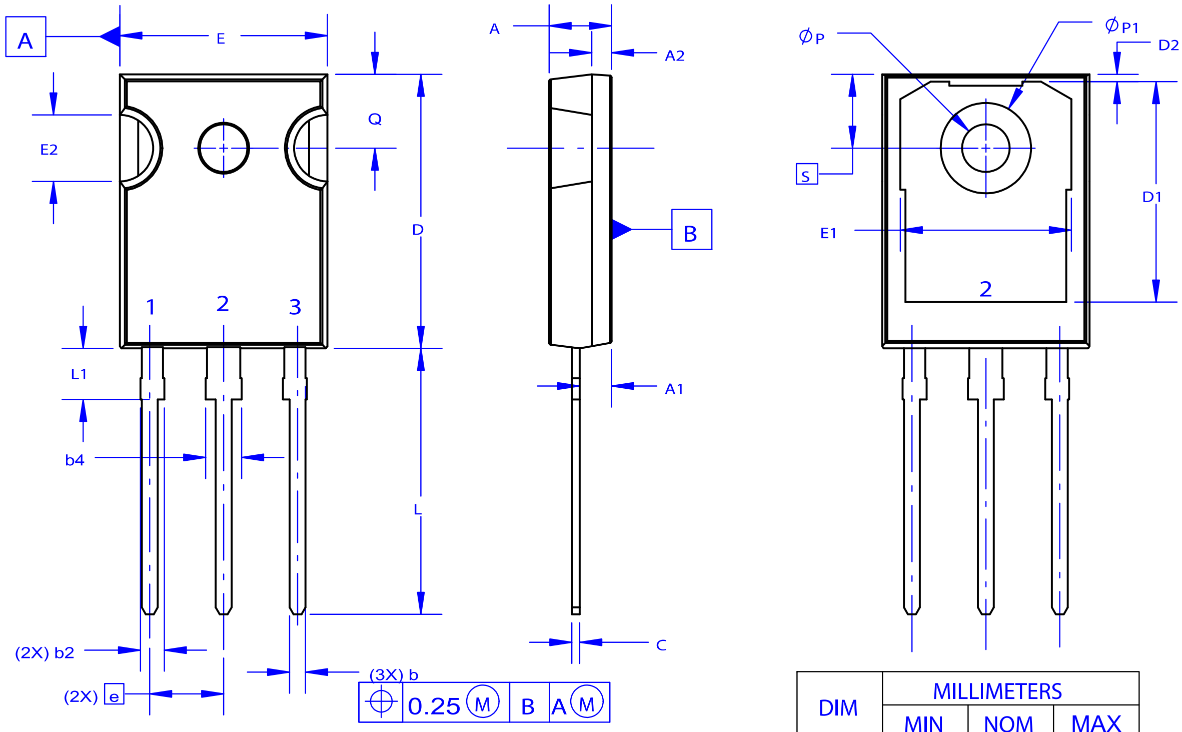
Figure 13. Junction−to−Case Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO−247−3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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