NTHD2110T

Power MOSFET
−12 V, −6.4 A, Single P−Channel +TVS, ChipFET™ Package

Features

- Low $R_{DS(on)}$ MOSFET and TVS Diode ChipFET Package
- Integrated Drain Side TVS for 15 kV Contact Discharge ESD Protection
- 1.8 V Gate Rating
- This is a Pb−Free Device

Applications

- Battery Switch and Load Management Applications in Portable Equipment

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−12	V
Gate−to−Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−4.5	A
		T_A = 85°C		−3.2	
	t ≤ 5 s	T_A = 25°C		−6.4	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.1	W
	t ≤ 5 s			2.3	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Storage Temperature Range			TJ	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)			T_L	260	°C

TVS MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 ms Double Exponential Waveform (Note 2)	PPK	150	W
Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Specification (Contact)	ESD	16 400 30	kV V kV

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	110	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	55	
Junction−to−Ambient − Steady State Min Pad (Note 3)	$R_{\theta JA}$	225	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Nonrepetitive Current Pulse per Figure 11.
3. Surface Mounted on FR4 board using 1 in sq size (Cu area = 1.127 in sq [1 oz] included traces).

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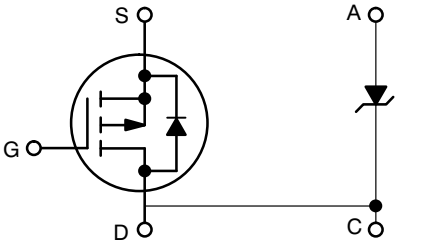
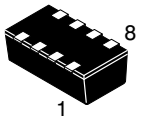
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−12 V	40 mΩ @ −4.5 V	−6.4 A
	53 mΩ @ −2.5 V	
	80 mΩ @ −1.8 V	

TVS

V_{RWM}	V_C @ MAX I_{PP}	$I_{PP\ MAX}$
12	21.5	6.2 A

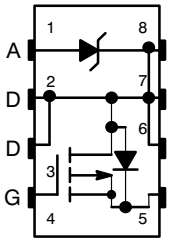


P−Channel MOSFET TVS Diode

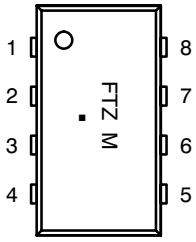


ChipFET
CASE 1206A
STYLE 6

PIN CONNECTIONS



MARKING DIAGRAM



FTZ = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD2110TT1G	ChipFET (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(Br)DSS}$	V_{GS} = 0 V_{dc}, I_D = −250 μA		−12			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −12 V, V_{GS} = 0 V	T_J = 25°C			−1.0	μA
			T_J = 85°C			−5.0	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V				±0.1	μA
ON CHARACTERISTICS (Note 6)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA		−0.40		−0.85	V
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −6.4 A			33	40	mΩ
		V_{GS} = −2.5 V, I_D = −2.0 A			42	53	
		V_{GS} = −1.8 V, I_D = −1.7 A			57	80	
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −6.4 A			13.7		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{DS} = −6.0 V, V_{GS} = 0 V f = 1.0 MHz			1072		pF
Output Capacitance	C_{oss}				260		
Reverse Transfer Capacitance	C_{rss}				134		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −6.0 V, I_D = −6.4 A			10.5	14	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.6		
Gate−to−Source Charge	Q_{GS}				1.3		
Gate−to−Drain Charge	Q_{GD}				2.8		
SWITCHING CHARACTERISTICS (Note 7)							
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = −6.0 V, V_{GS} = −4.5 V, I_D = −1.0 A, R_G = 6.0 Ω			7.5		ns
Rise Time	t_r				8.6		
Turn−Off Delay Time	$t_{d(off)}$				99.7		
Fall Time	t_f				49.8		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Diode Forward Voltage	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V	T_J = 25°C		−0.7	−1.0	V
			T_J = 125°C		−0.6		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S / dt = 100 A/μs, I_S = −1.7 A			41.7		ns
Reverse Recovery Charge	Q_{RR}	V_{GS} = 0 V, dI_S / dt = 100 A/μs, I_S = −1.7 A			22		nC

4. Surface Mounted on FR4 board using 1 in sq size (Cu area = 1.127 in sq [1 oz] included traces).
5. Surface mounted on FR4 board using the minimum recommended pad size.
6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
TVS DIODE						
Reverse Working Voltage (Note 8)	V_{RWM}		12			V
Breakdown Voltage (Note 9)	V_{BR}	I_T = 1 mA	14.5		15.7	V
Reverse Leakage Current	I_R	V_{RWM} = 12 V		0.6	10	nA
Clamping Voltage (Note 10)	V_C	I_{PP} = 1 A (8 x 20 μs Waveform)			15.7	V
Clamping Voltage (Note 10)	V_C	I_{PP} = 5 A (8 x 20 μs Waveform)			19.1	V
Maximum Peak Pulse Current (Note 10)	I_{PP}	8 x 20 μs Waveform			6.2	A
Capacitance	CJ	V_R = 0 V, f = 1 MHz (Anode−to−GND)			60	pF

8. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
9. V_{BR} is measured at pulse test current I_T.
10. Pulse waveform per Figure 11.

TYPICAL MOSFET PERFORMANCE CURVES

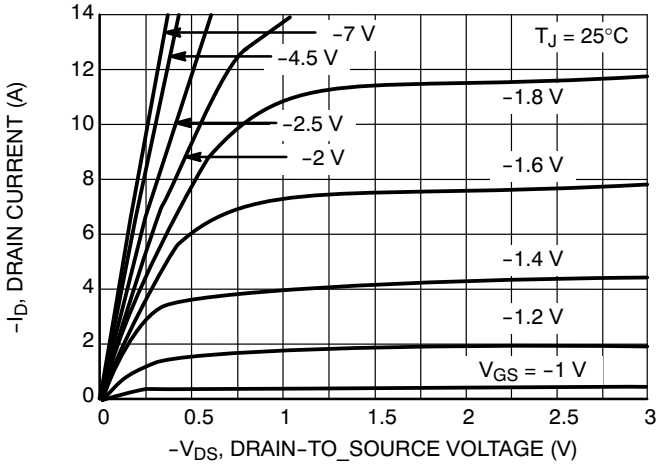


Figure 1. On−Region Characteristics

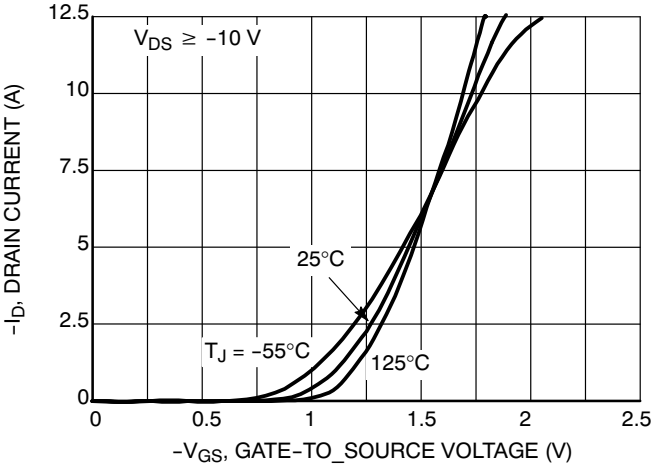


Figure 2. Transfer Characteristics

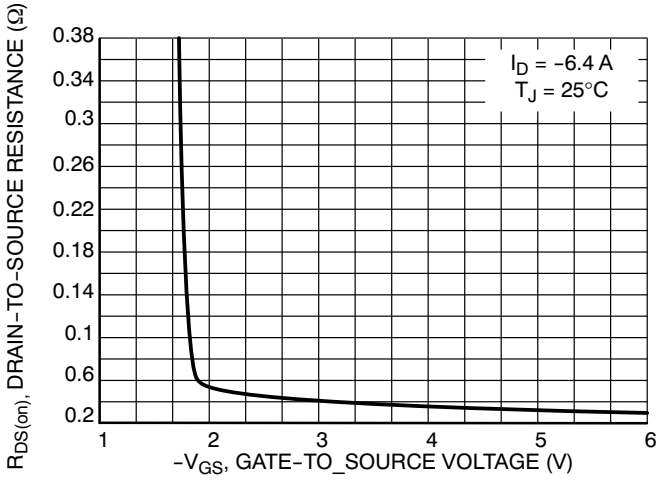


Figure 3. On−Resistance vs. Gate Voltage

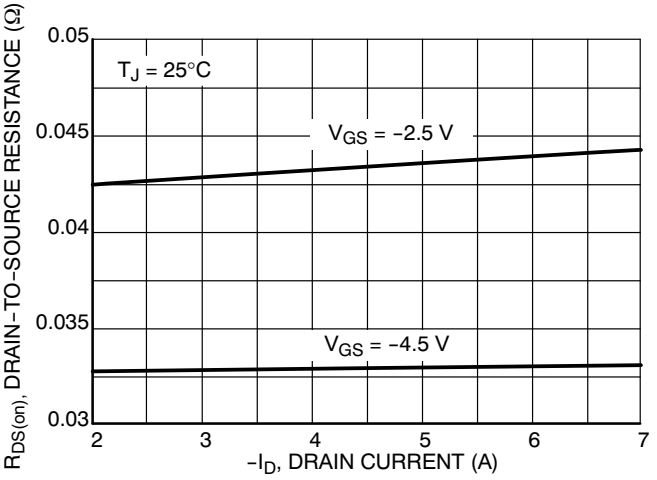


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

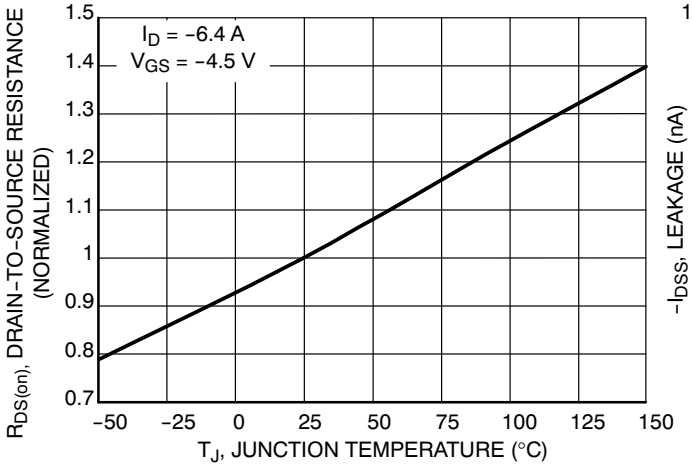


Figure 5. On−Resistance Variation with Temperature

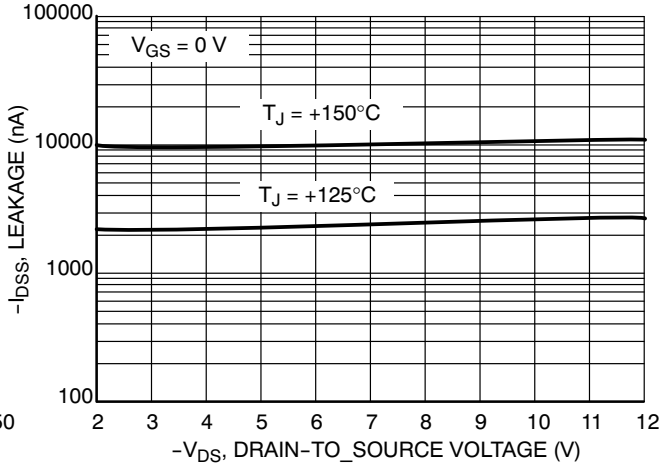


Figure 6. Drain−to−Source Leakage Current

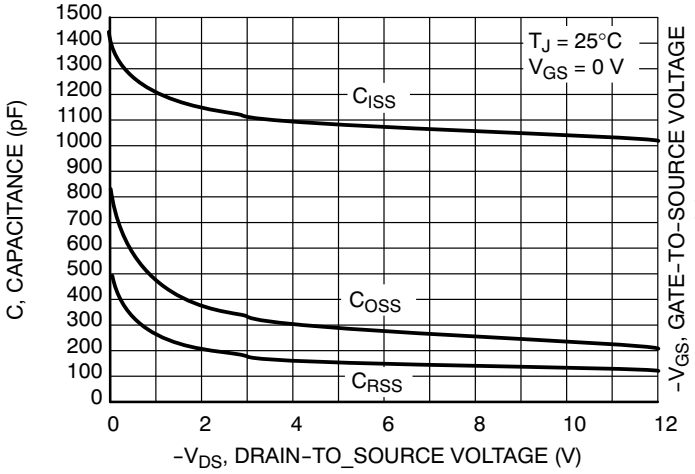


Figure 7. Capacitance Variation

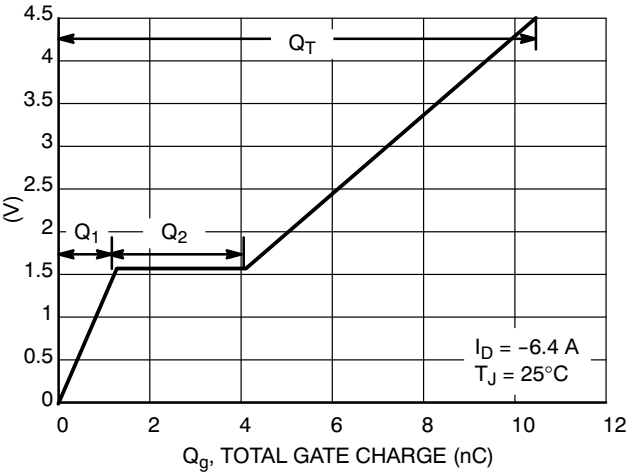


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

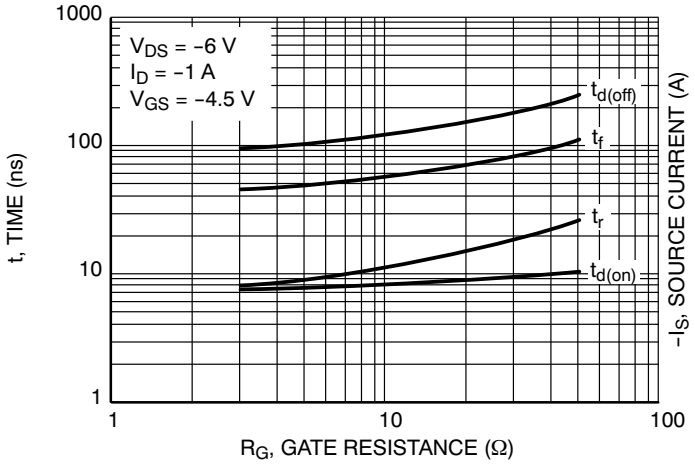


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

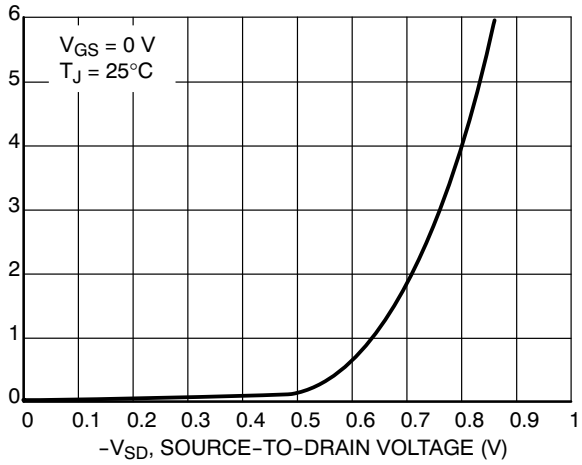


Figure 10. Diode Forward Voltage vs. Current

TYPICAL TVS PERFORMANCE CURVES

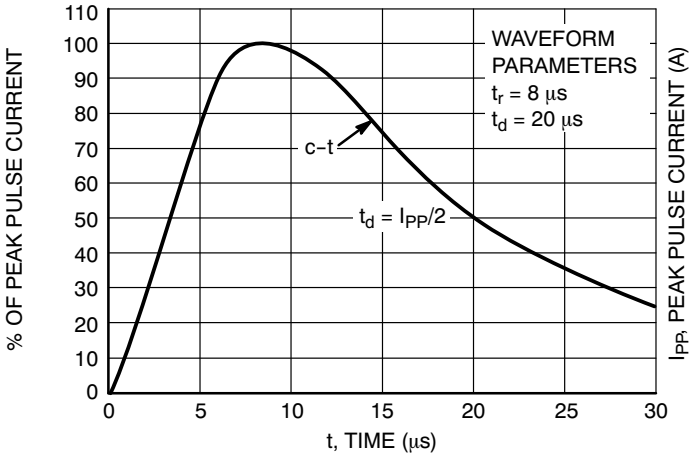


Figure 11. Pulse Waveform, 8 × 20 μs

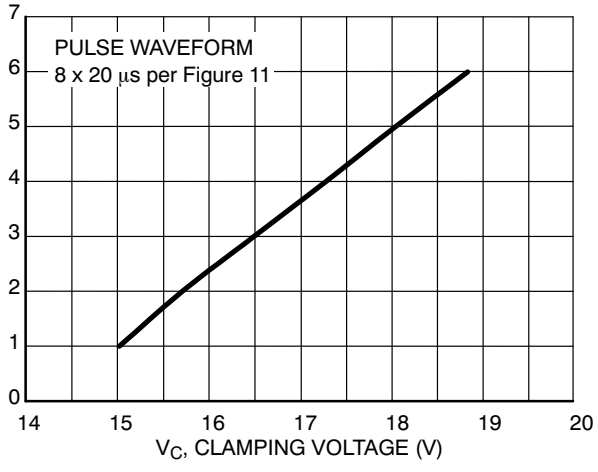


Figure 12. Clamping Voltage vs Peak Pulse Current

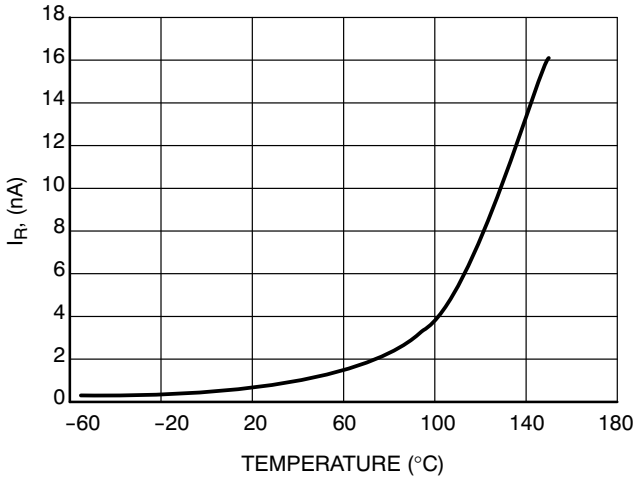


Figure 13. Typical Leakage vs. Temperature

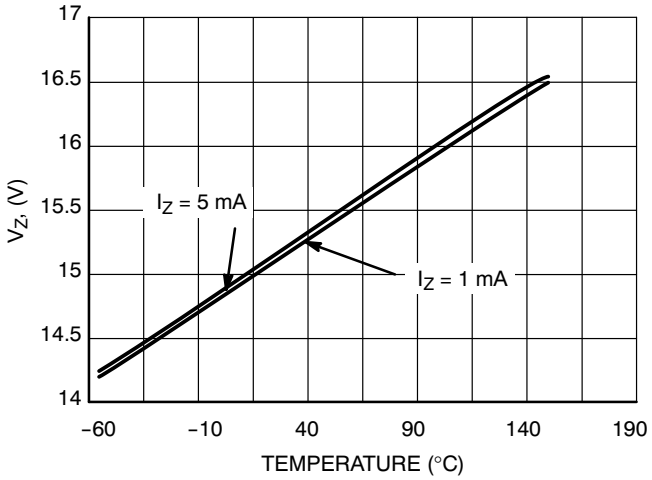


Figure 14. Typical V_Z @ 1 mA vs. Temperature

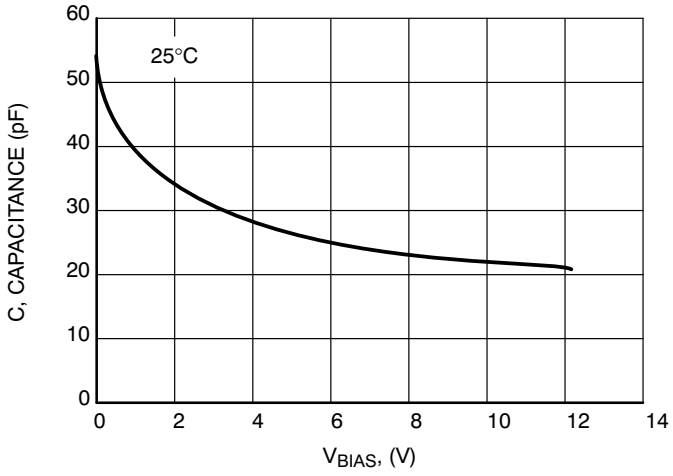


Figure 15. Capacitance vs. V_{BIAS}

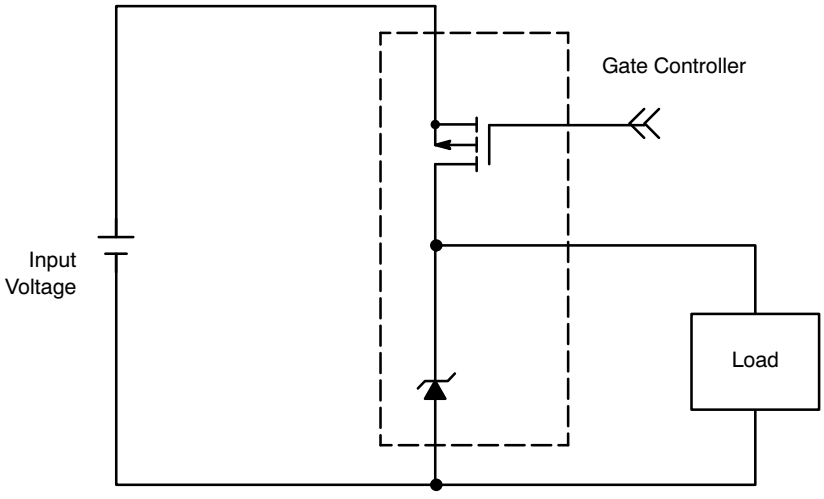


Figure 16. Typical Application Circuit

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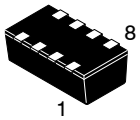
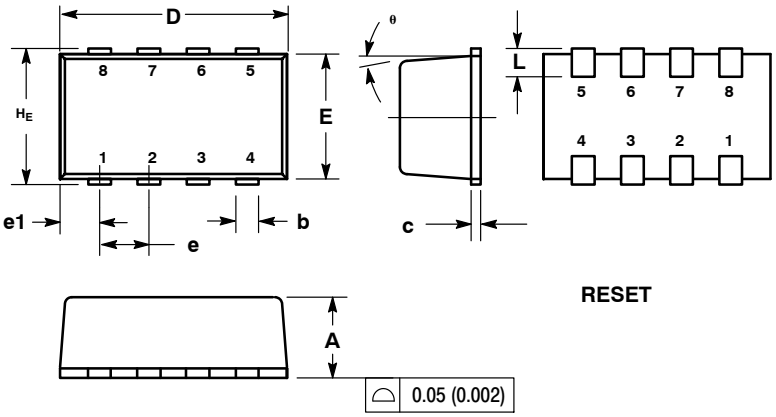
ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e		0.65 BSC			0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ		5° NOM			5° NOM	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

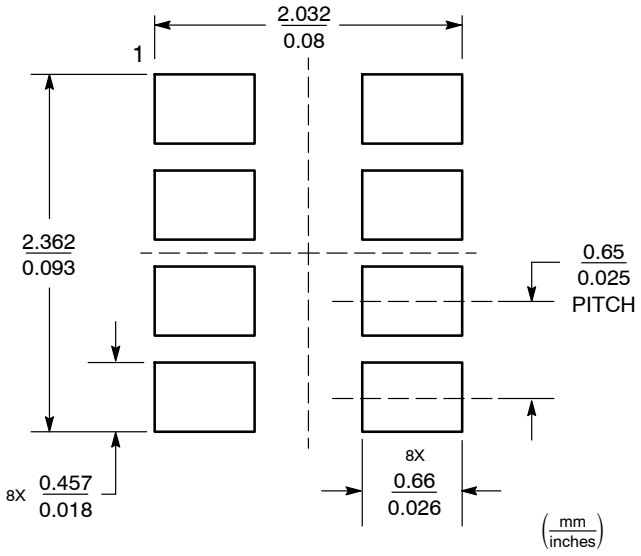
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

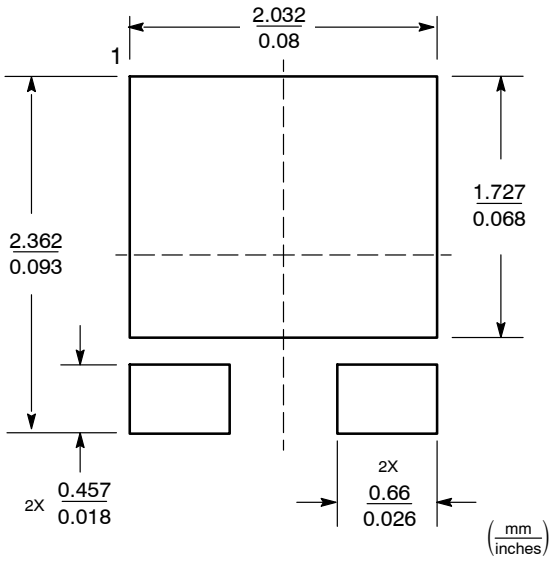
OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

DOCUMENT NUMBER:	**98AON03078D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**ChipFET**		**PAGE 1 OF 2**

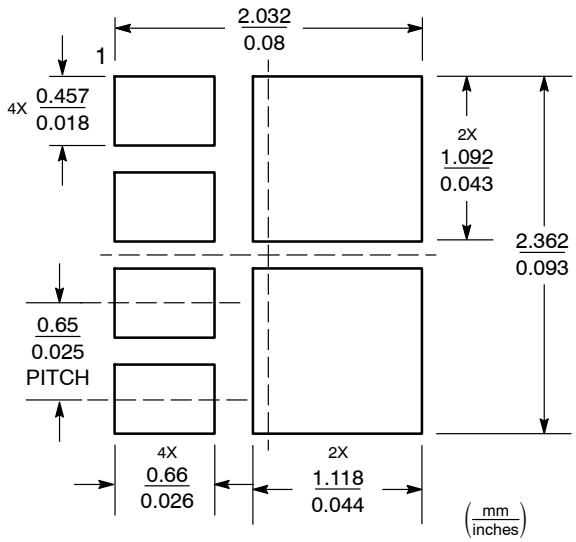
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

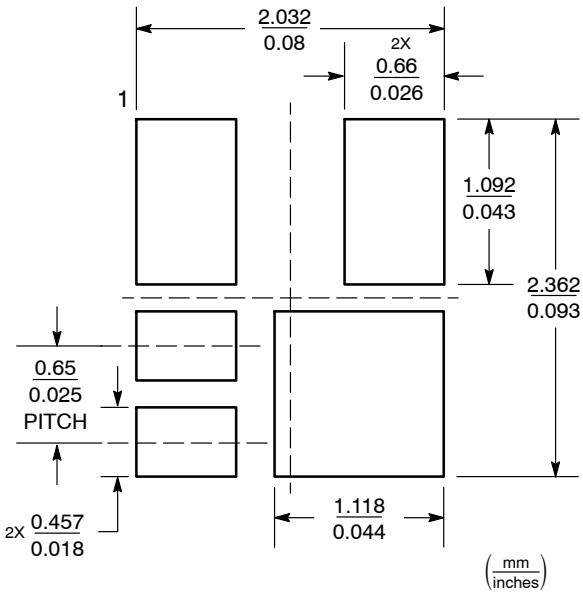
ADDITIONAL SOLDERING FOOTPRINTS*



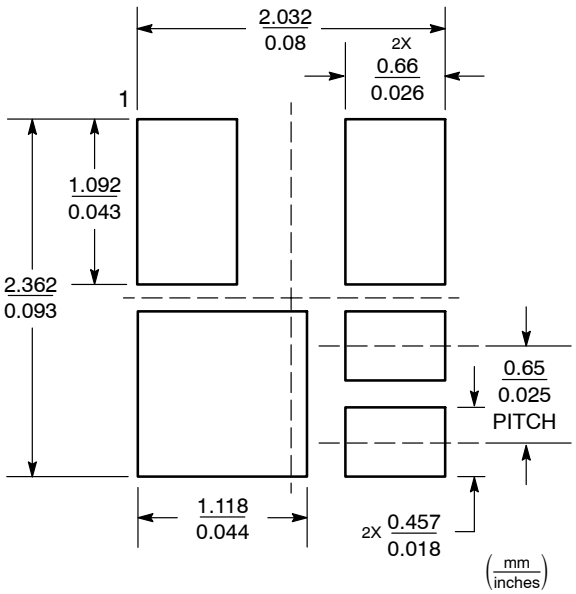
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON03078D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**ChipFET**	**PAGE 2 OF 2**

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