

MOSFET - N-Channel Shielded Gate PowerTrench® 150 V, 15 mΩ, 50 A

NTDS015N15MC

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 15 mΩ at $V_{GS} = 10$ V, $I_D = 29$ A
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Primary Side for 48 V Isolated Bus
- SR for MV Secondary Applications

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	150	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	50	A
Power Dissipation $R_{\theta JC}$ (Note 2)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	11	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	I_{DM}	246	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 10$ A _{pk} , $L = 3$ mH)	E_{AS}	150	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

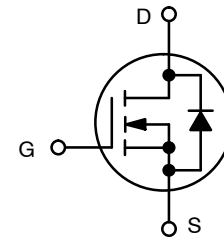
1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	15 mΩ @ 10 V	50 A

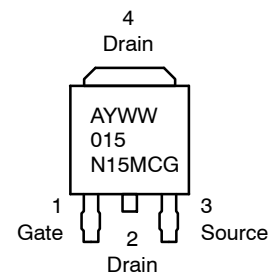


N-CHANNEL MOSFET



DPAK
CASE 369C

MARKING DIAGRAM



015N15MCG = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTDS015N15MCT4G	DPAK (Pb-Free)	2500 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTDS015N15MC

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	1.8	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		83		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 162\ \mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 162\ \mu\text{A}$, ref to 25°C		-8.2		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		11.8	15	m Ω
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 8\text{ V}, I_D = 15\text{ A}$		12.6	16.8	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 29\text{ A}$		58		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2120		pF
Output Capacitance	C_{OSS}			595		
Reverse Transfer Capacitance	C_{RSS}			10.5		
Gate-Resistance	R_G			0.6	1.2	Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 29\text{ A}$		27		nC
Threshold Gate Charge	$Q_{G(TH)}$			7		
Gate-to-Source Charge	Q_{GS}			11		
Gate-to-Drain Charge	Q_{GD}			4		
Plateau Voltage	V_{GP}			5.5		V
Output Charge	Q_{OSS}	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		66		nC

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 29\text{ A}, R_G = 6\ \Omega$		16		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$	$T_J = 25^\circ\text{C}$		0.89	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			49		ns
Reverse Recovery Charge	Q_{RR}					197	
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			34		ns
Reverse Recovery Charge	Q_{RR}					345	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

NTDS015N15MC

TYPICAL CHARACTERISTICS

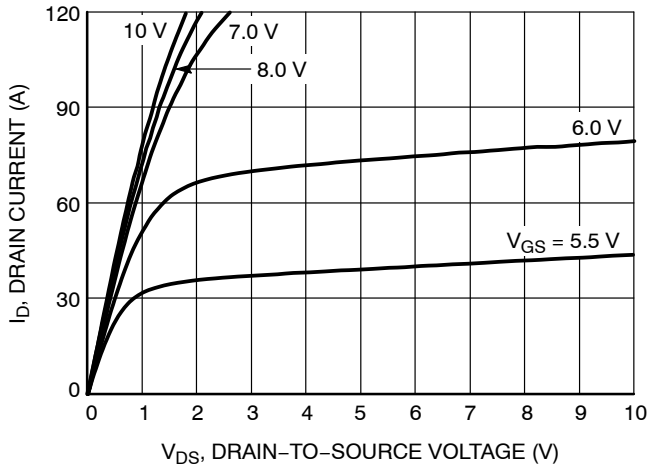


Figure 1. On-Region Characteristics

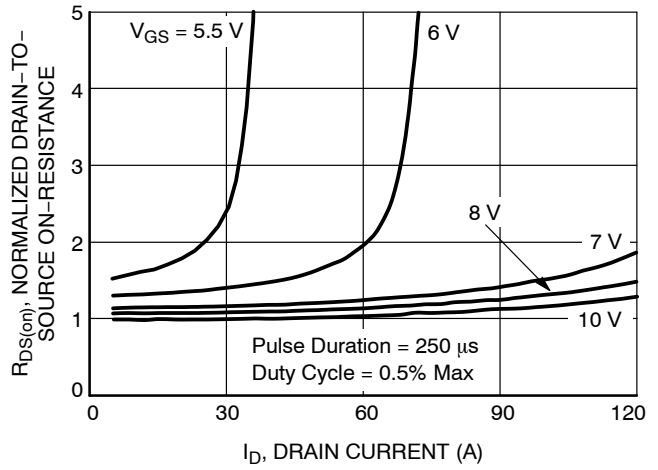


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

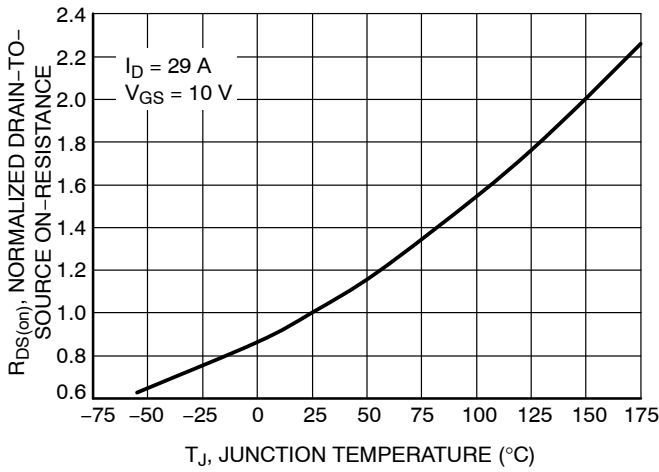


Figure 3. Normalized On-Resistance vs. Junction Temperature

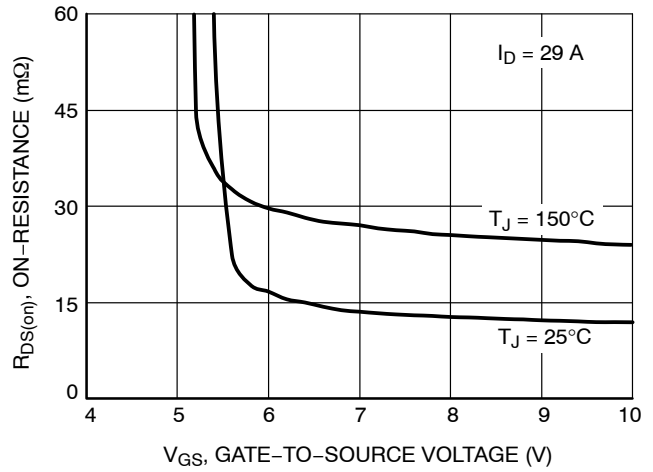


Figure 4. On-Resistance vs. Gate-to-Source Voltage

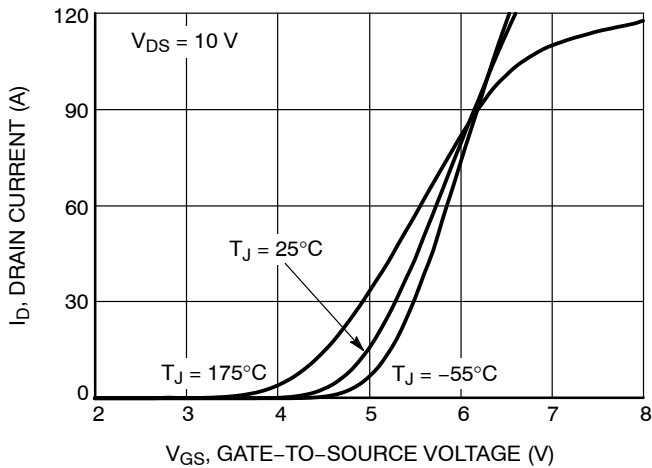


Figure 5. Transfer Characteristics

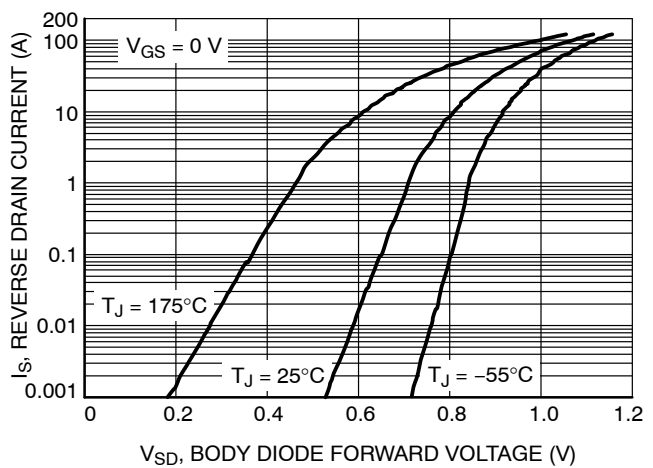


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

NTDS015N15MC

TYPICAL CHARACTERISTICS

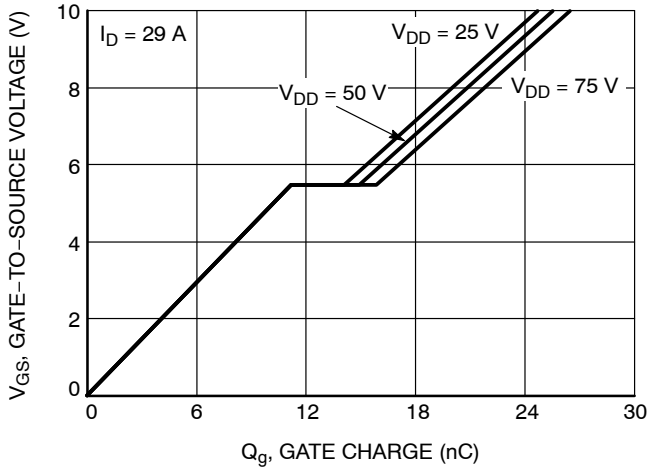


Figure 7. Gate Charge Characteristics

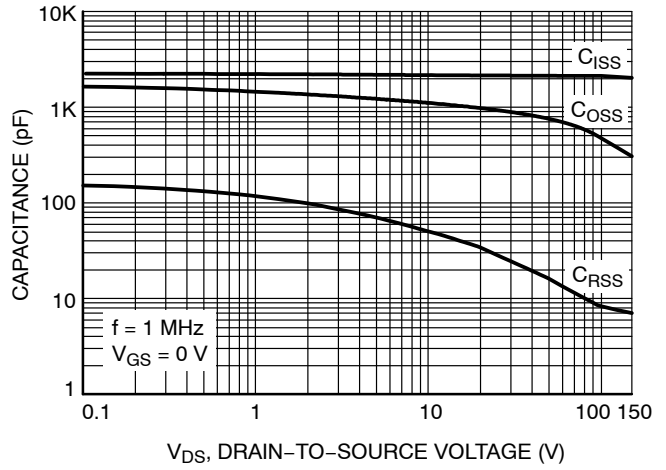


Figure 8. Capacitance vs. Drain-to-Source Voltage

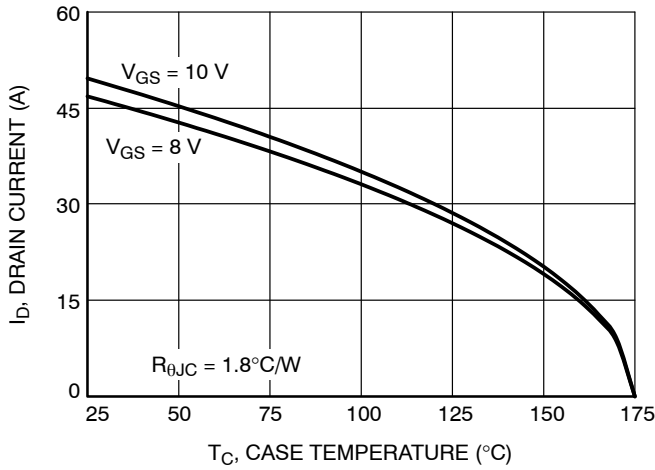


Figure 9. Drain Current vs. Case Temperature

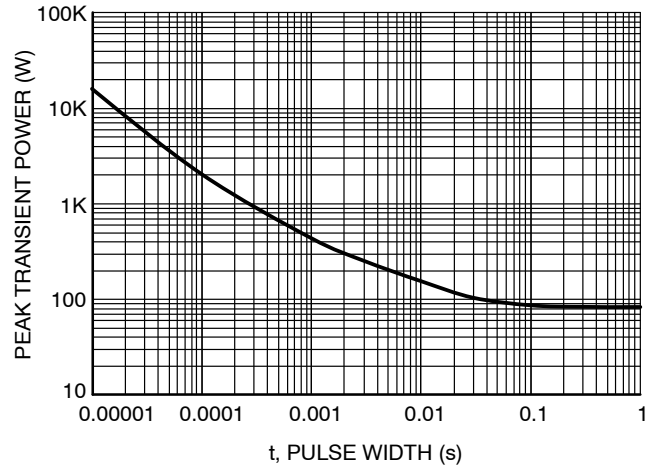


Figure 10. Peak Power

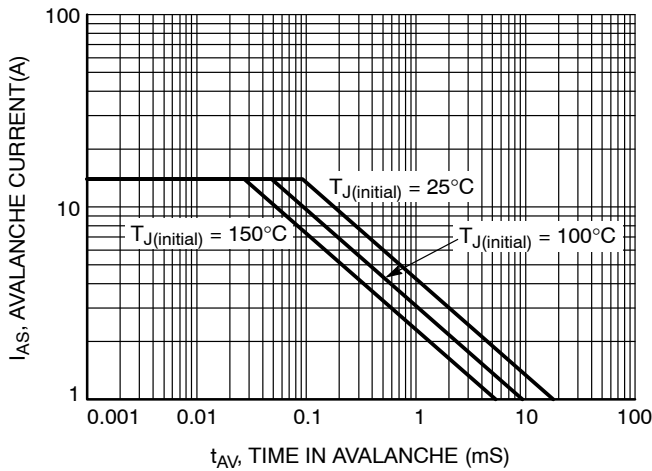


Figure 11. Unclamped Inductive Switching Capability

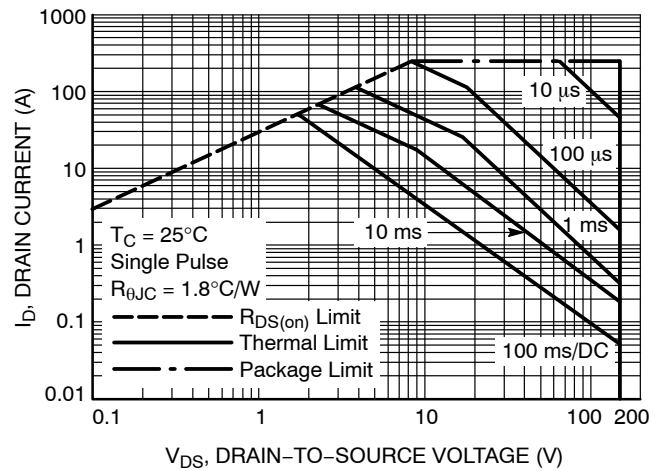


Figure 12. Forward Bias Safe Operating Area

NTDS015N15MC

TYPICAL CHARACTERISTICS

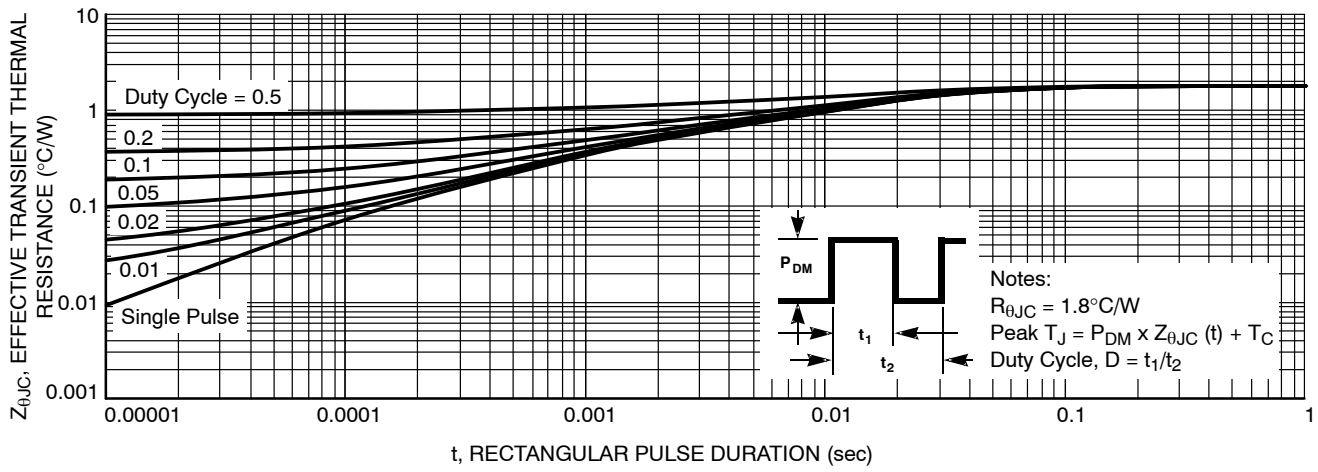
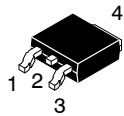


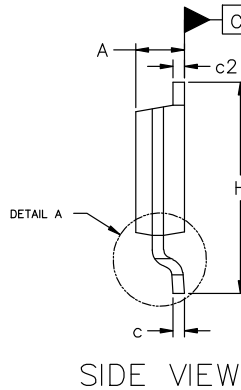
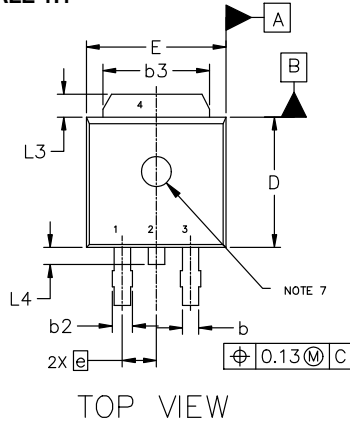
Figure 13. Transient Thermal Impedance



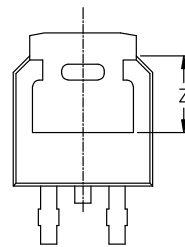
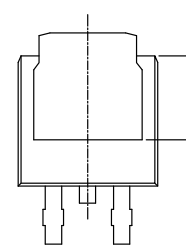
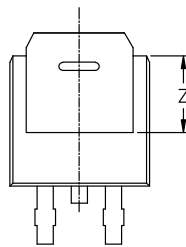
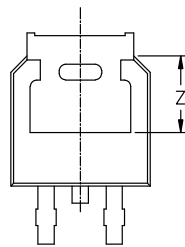
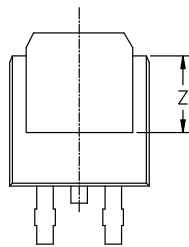
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



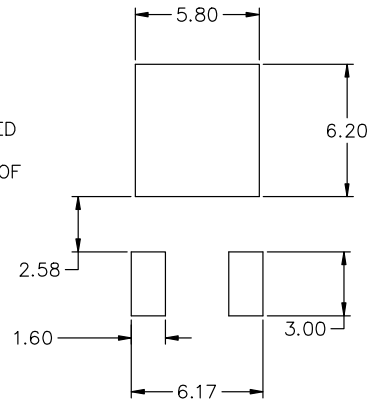
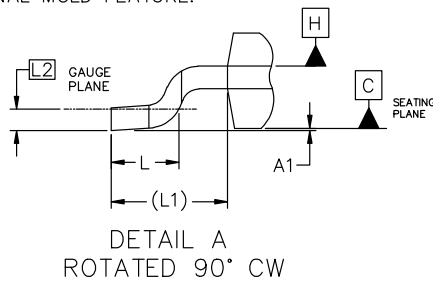
MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

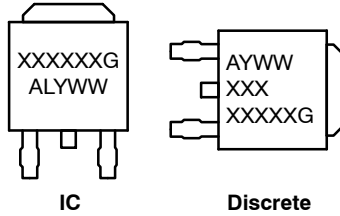
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN</p> | <p>STYLE 3:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 4:
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE</p> | <p>STYLE 5:
 PIN 1. GATE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |
| <p>STYLE 6:
 PIN 1. MT1
 2. MT2
 3. GATE
 4. MT2</p> | <p>STYLE 7:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 8:
 PIN 1. N/C
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. RESISTOR ADJUST
 4. CATHODE</p> | <p>STYLE 10:
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 2 OF 2

onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales