NTD5413N

Power MOSFET

30 Amps, 60 Volts Single N−Channel DPAK

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These are Pb−Free Devices

Applications

- LED Lighting and LED Backlight Drivers
- DC−DC Converters
- DC Motor Drivers
- Switch Mode Power Supplies
- Power Supplies Secondary Side Synchronous Rectification

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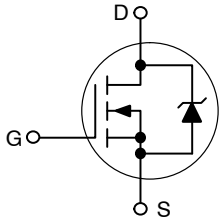
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX (Note 1)
60 V	26 mΩ @ 10 V	30 A

N−Channel



MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Gate−to−Source Voltage − Nonrepetitive (T_P < 10 μs)			V_{GS}	±30	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	30	A
		T_C = 100°C		23	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	P_D	68	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	84	A
Operating and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	30	A
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 V_{dc}, V_{GS} = 10 V, $I_{L(pk)}$ = 30 A, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	135	mJ
Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds			T_L	260	°C

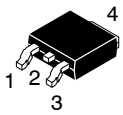
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	2.2	°C/W
	$R_{\theta JA}$	58.5	

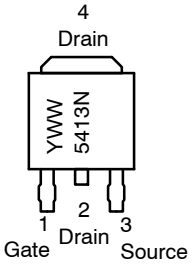
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

MARKING DIAGRAM



DPAK
CASE 369AA
STYLE 2



5413N = Device Code
Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{DS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				67.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
			T_J = 150°C			50	
Gate−Body Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0	3.4	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				7.9		mV/°C
Drain−to−Source On−Voltage	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			0.37	0.52	V
		V_{GS} = 10 V, I_D = 20 A, 150°C			0.86		
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			18.5	26	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 20 A			36		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz			1160	1725	pF
Output Capacitance	C_{oss}				240		
Transfer Capacitance	C_{rss}				100		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 20 A			35	46	nC
Threshold Gate Charge	$Q_{G(TH)}$				1.4		
Gate−to−Source Charge	Q_{GS}				6.5		
Gate−to−Drain Charge	Q_{GD}				16.1		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 48 V, I_D = 20 A, R_G = 2.5 Ω			11		ns
Rise Time	t_r				20		
Turn−Off Delay Time	$t_{d(off)}$				28		
Fall Time	t_f				8.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage (Note 2)	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.87	1.2	V
			T_J = 125°C		0.8		
Reverse Recovery Time	t_{rr}	I_S = 20 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs			52		ns
Charge Time	t_a				37		
Discharge Time	t_b				15		
Reverse Recovery Stored Charge	Q_{RR}				105.7		nC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTD5413NT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL PERFORMANCE CURVES

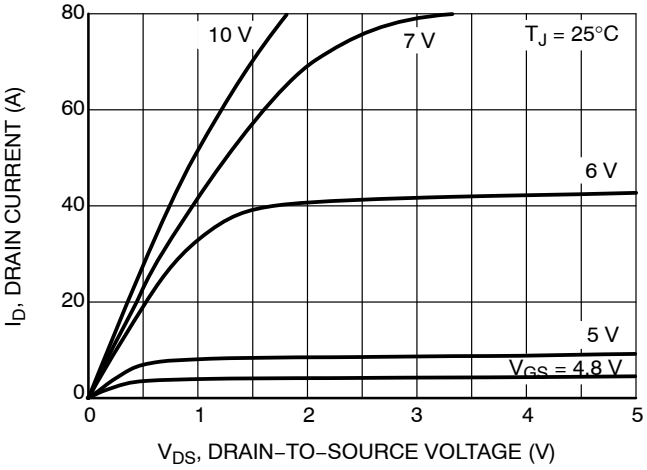


Figure 1. On−Region Characteristics

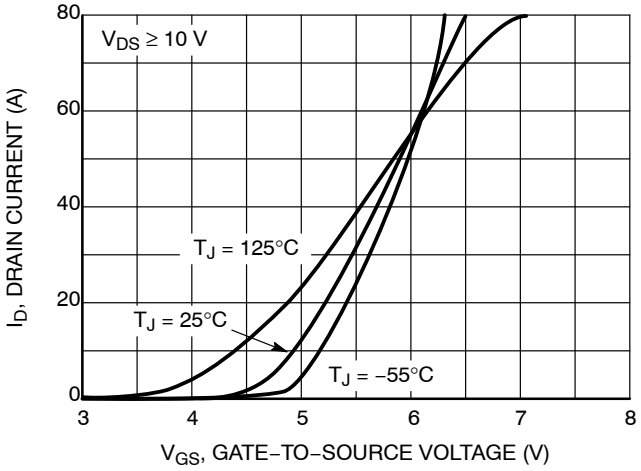


Figure 2. Transfer Characteristics

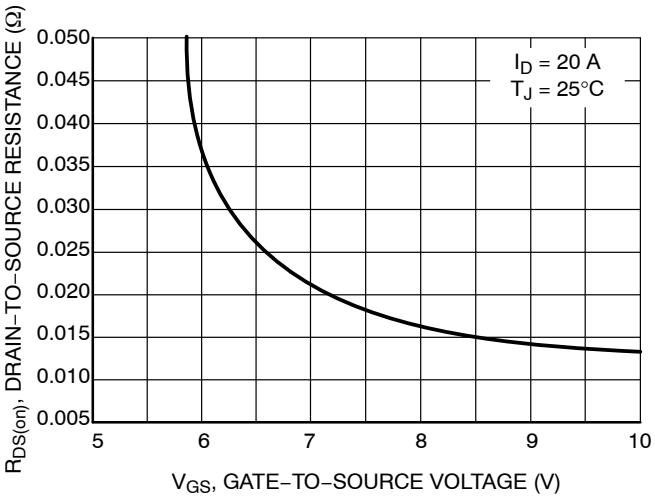


Figure 3. On−Resistance vs. Gate−to−Source Voltage

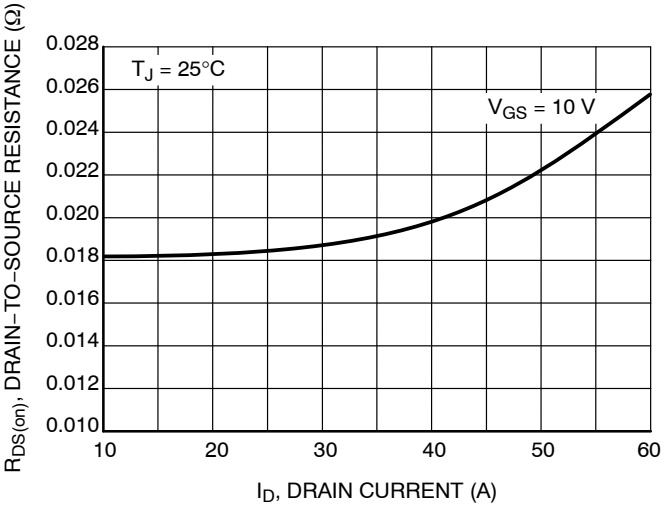


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

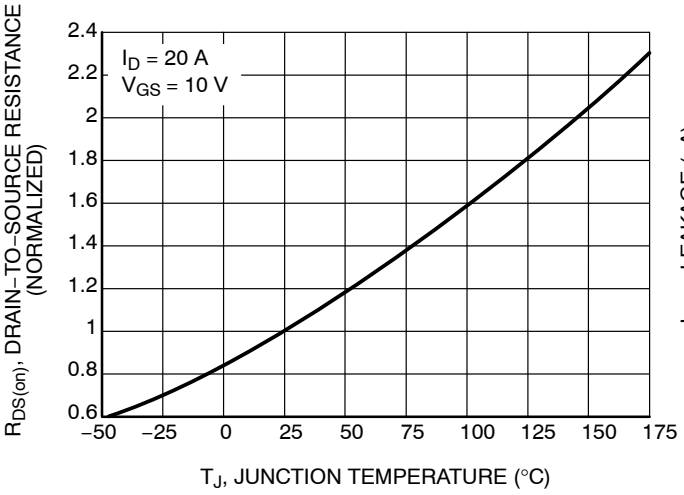


Figure 5. On−Resistance Variation with Temperature

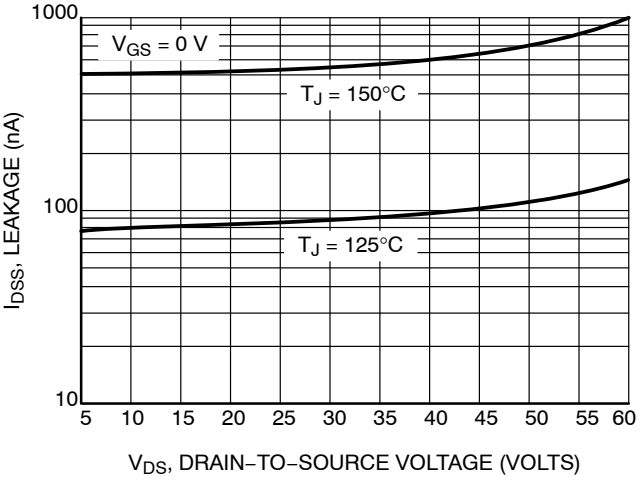


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

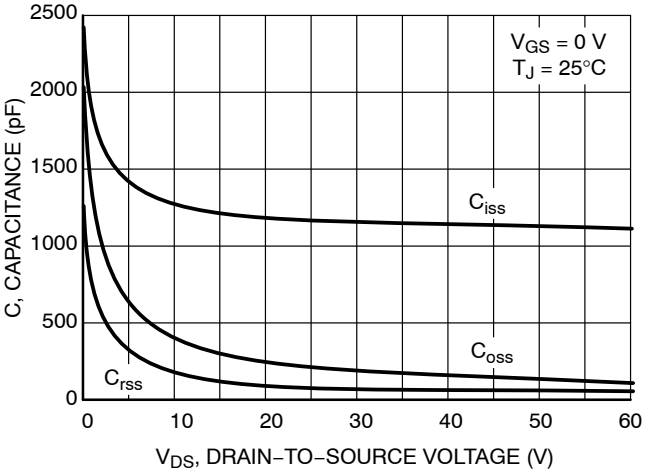


Figure 7. Capacitance Variation

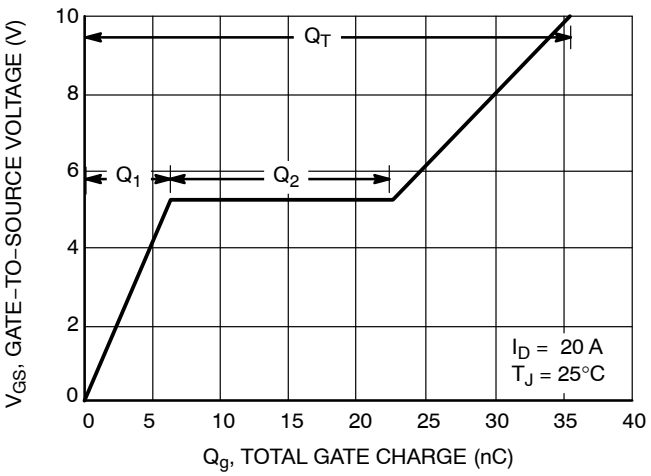


Figure 8. Gate−to−Source Voltage vs. Total Charge

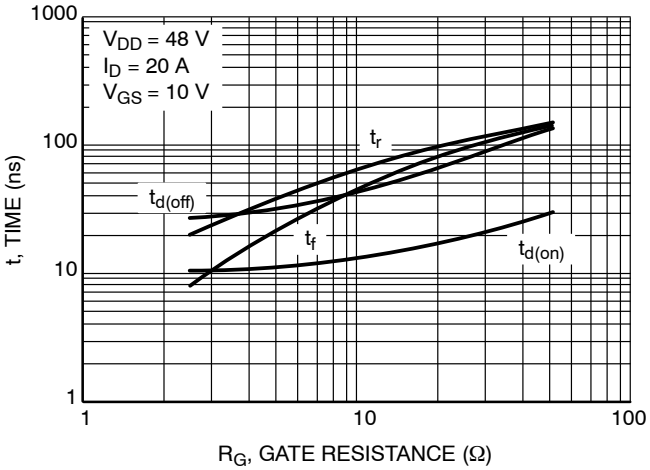


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

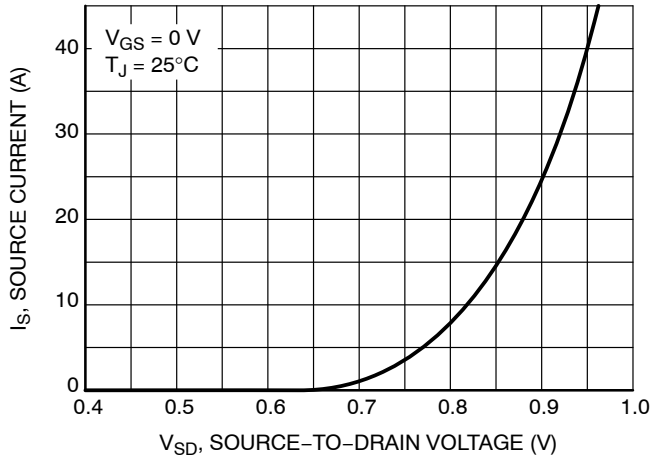


Figure 10. Diode Forward Voltage vs. Current

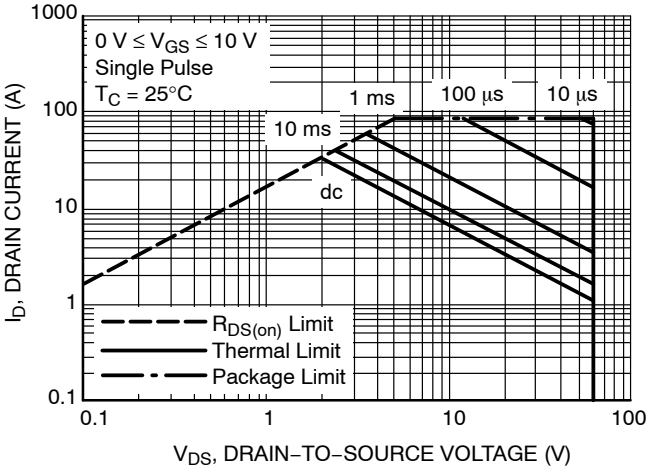


Figure 11. Maximum Rated Forward Biased Safe Operating Area

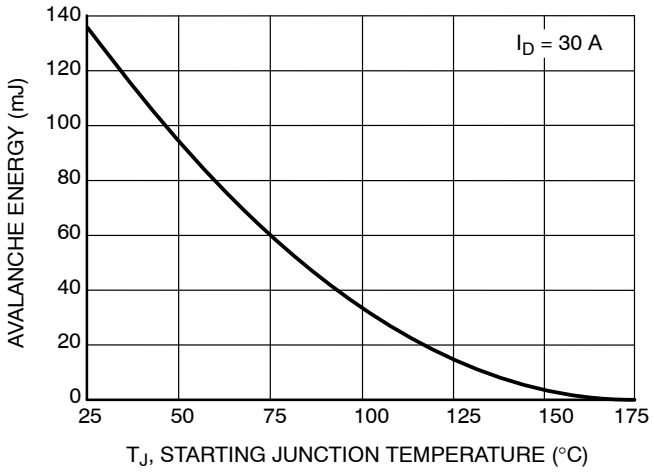


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

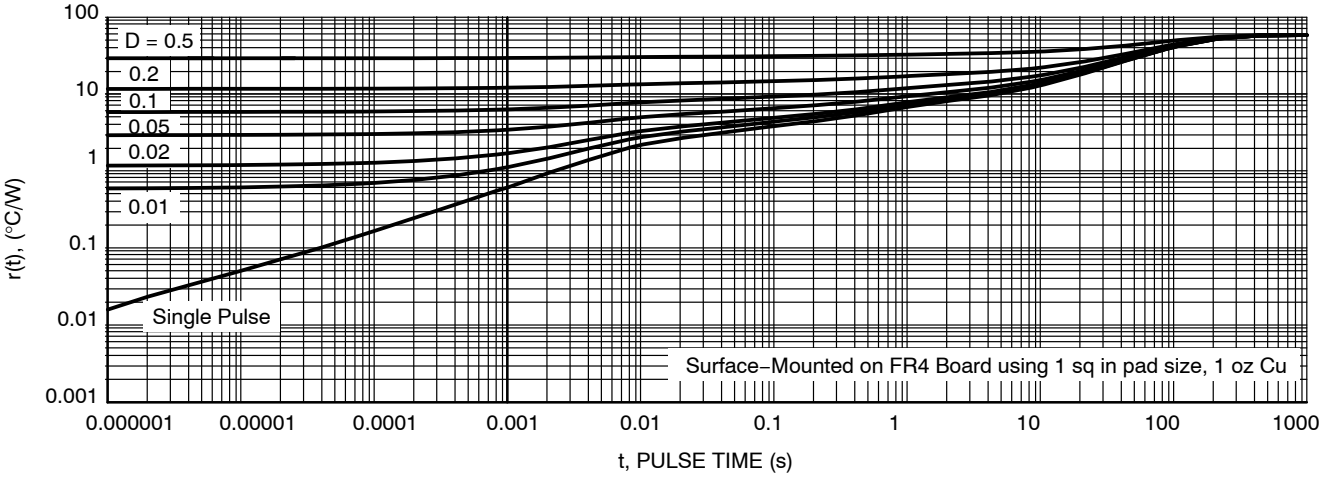
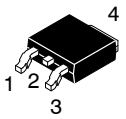


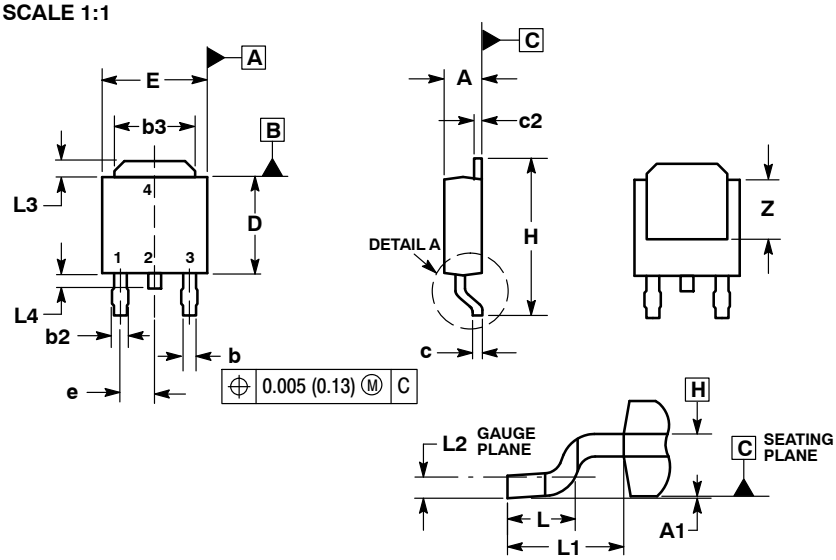
Figure 13. Thermal Response



SCALE 1:1

DPAK (SINGLE GUAGE)
CASE 369AA
ISSUE B

DATE 03 JUN 2010



DETAIL A
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

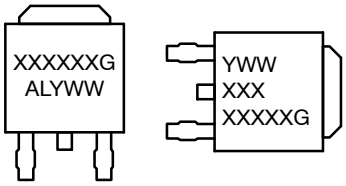
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*

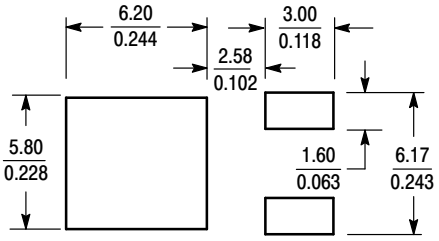


IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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