Power MOSFET

45 A, 25 V, N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low R_{DS(on)} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- These are Pb-Free Devices

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage - Continuous	V _{GS}	±20	Vdc
Thermal Resistance – Junction-to-Case Total Power Dissipation @ T _C = 25°C Drain Current	R _{θJC} P _D	3.0 50	°C/W W
– Continuous @ T _C = 25°C, Chip – Continuous @ T _A = 25°C, Limited by Wires – Single Pulse (tp ≤ 10 μs)	I _D I _D I _D	45 32 100	A A A
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W
- Total Power Dissipation @ T _A = 25°C - Drain Current - Continuous @ T _A = 25°C	P _D I _D	2.1 9.2	W A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	°C/W
- Total Power Dissipation @ T _A = 25°C - Drain Current - Continuous @ T _A = 25°C	P _D I _D	1.5 7.8	W A
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 175	°C
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
- 2. When surface mounted to an FR4 board using minimum recommended pad size.

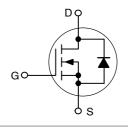


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45 AMPERES, 25 VOLTS $R_{DS(on)} = 12.6 \text{ m}\Omega \text{ (Typ)}$

N-CHANNEL



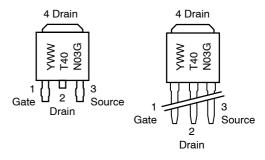




CASE 369AA DPAK (Surface Mount) STYLE 2

CASE 369D DPAK (Straight Lead) STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



= Year WW = Work Week T40N03 = Device Code = Pb-Free Package

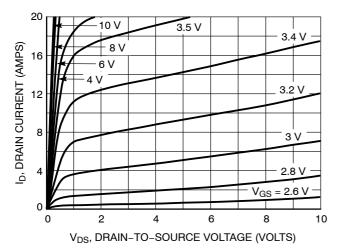
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristics			Min	Тур	Max	Unit
OFF CHARACTERISTICS					_	•
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μμ Temperature Coefficient (Positive)	V(br) _{DSS}	25 -	28 -	- -	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 V (V _{DS} = 20 Vdc, V _{GS} = 0 V		I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0	Vdc)	I _{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 250 \mu \text{Adc})$ Threshold Temperature Coefficient (Negative)			1.0 -	1.7	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resista ($V_{GS} = 4.5 \text{ Vdc}$, $I_D = 10 \text{ A}$ ($V_{GS} = 10 \text{ Vdc}$, $I_D = 10 \text{ A}$	R _{DS(on)}	- -	18.6 12.6	23 16.5	mΩ	
Forward Transconductance (Note 3 (V _{DS} = 10 Vdc, I _D = 10 A	9FS	-	20	_	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	_	584	_	pF
Output Capacitance	$(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz})$	C _{oss}	_	254	_	
Transfer Capacitance		C _{rss}	_	99	_	
SWITCHING CHARACTERISTICS	(Note 4)					
Turn-On Delay Time		t _{d(on)}	_	4.5	_	ns
Rise Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc,	t _r	_	19.5	_	
Turn-Off Delay Time	$I_D = 10 \text{ Adc}, R_G = 3 \Omega$	t _{d(off)}	_	16.7	_	
Fall Time		t _f	_	3.5	_	
Gate Charge		Q_{T}	_	5.78	_	nC
	$(V_{GS} = 4.5 \text{ Vdc}, I_D = 10 \text{ Adc}, V_{DS} = 10 \text{ Vdc}) \text{ (Note 3)}$	Q ₁	_	2.1	_	
	20 , , , ,	Q_2	-	2.5	_	
SOURCE-DRAIN DIODE CHARAC	CTERISTICS					
Forward On-Voltage	$(I_S = 10 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 10 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V_{SD}	- -	0.85 0.71	1.2 -	V _{dc}
Reverse Recovery Time		t _{rr}	-	20.4	-	ns
	(I _S = 10 Adc, V _{GS} = 0 Vdc,	t _a	-	8.25	-	
	$dI_S/dt = 100 A/\mu s$) (Note 3)	t _b	-	12.1	-	
Reverse Recovery Stored Charge]	Q _{RR}	-	0.007	-	μC

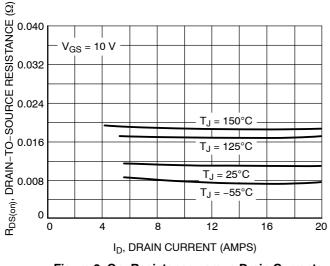
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.



 $(S_{0})^{2}$ $(S_{0})^{2}$

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



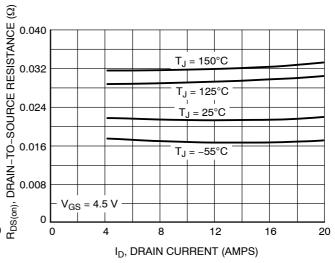
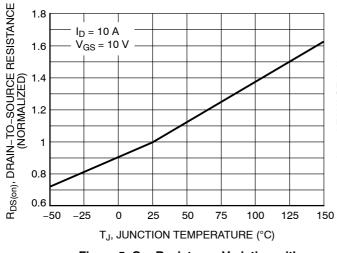


Figure 3. On-Resistance versus Drain Current and Temperature

Figure 4. On-Resistance versus Drain Current and Temperature



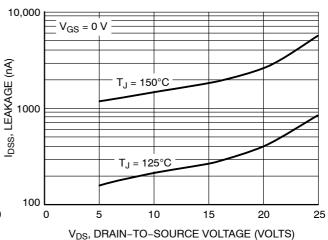


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current versus Voltage

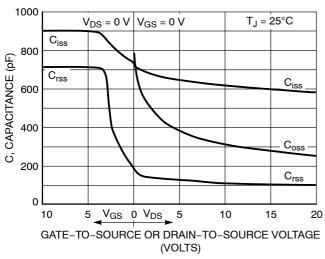


Figure 7. Capacitance Variation

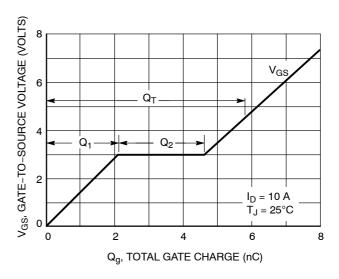


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

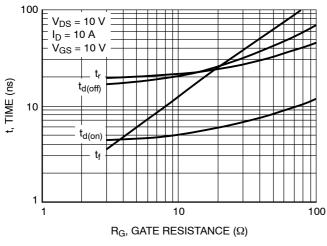


Figure 9. Resistive Switching Time Variation versus Gate Resistance

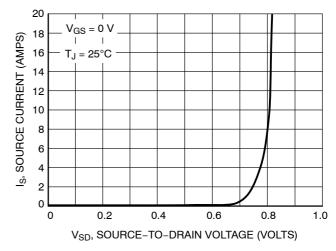


Figure 10. Diode Forward Voltage versus
Current

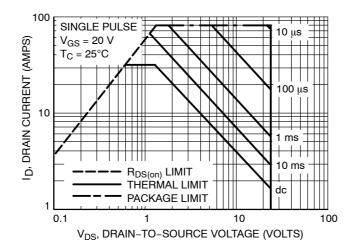


Figure 11. Maximum Rated Forward Biased Safe Operating Area

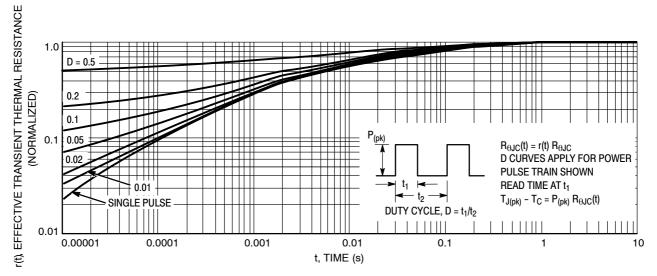


Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD40N03R-1G	DPAK (Straight Lead) (Pb-Free)	75 Units/Rail
NTD40N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

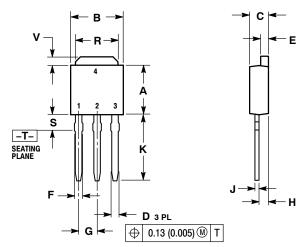


DPAK INSERTION MOUNT

CASE 369 ISSUE O

DATE 02 JAN 2000





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090	BSC	2.29	BSC
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
٧	0.030	0.050	0.77	1.27

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:		STYLE 5:		STYLE 6:	
PIN 1.	BASE	PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	GATE	PIN 1.	MT1
2.	COLLECTOR	2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE	2.	MT2
3.	EMITTER	3.	SOURCE	3.	ANODE	3.	GATE	3.	CATHODE	3.	GATE
4.	COLLECTOR	4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE	4.	MT2

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DESCRIPTION:	DPAK INSERTION MOUNT		PAGE 1 OF 1	

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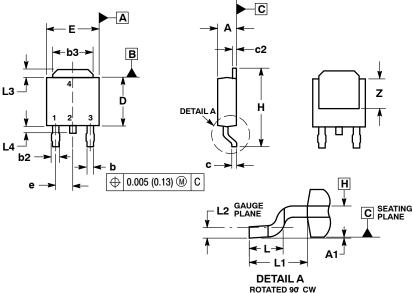
DPAK (SINGLE GUAGE) CASE 369AA **ISSUE B** SCALE 1:1 C

DATE 03 JUN 2010

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCHES.
 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-
- MENSIONS b3, L3 and Z.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020 BSC		0.51	BSC
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	



STYLE 1: PIN 1. BASE

PIN 1. GATE 2. ANODE 3. CATHODE

4. ANODE

STYLE 5:

2. COLLECTOR 3. EMITTER 4. COLLECTOR

STYLE 2: PIN 1. GATE

2. DRAIN 3. SOURCE 4. DRAIN

STYLE 3:

PIN 1. ANODE 2. CATHODE 3. ANODE CATHODE

STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE

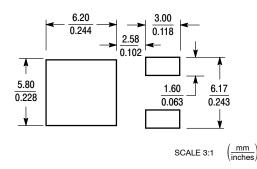
STYLE 7:

STYLE 6: PIN 1. MT1 2. MT2

3. GATE

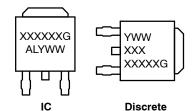
PIN 1. GATE 2. COLLECTOR 3. EMITTER COLLECTOR

SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code Α = Assembly Location L = Wafer Lot ٧ = Year = Work Week WW = Pb-Free Package

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^{*}This information is generic. Please refer to device data sheet for actual part

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