

MOSFET – Power, N-Channel, Logic Level, DPAK/IPAK

12 A, 60 V

NTD3055L104, NTDV3055L104

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Lower R_{DS(on)}
- Lower V_{DS(on)}
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- NTDV and STDV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

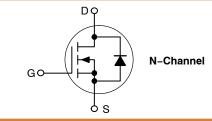
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 10 M Ω)	V_{DGR}	60	Vdc
Gate-to-Source Voltage, Continuous - Non-Repetitive (t _p ≤10 ms)	V_{GS}	±15 ±20	Vdc
$ \begin{array}{ll} \mbox{Drain Current} & -\mbox{ Continuous @ T_A} = 25^{\circ}\mbox{C} \\ -\mbox{ Continuous @ T_A} = 100^{\circ}\mbox{C} \\ -\mbox{ Single Pulse ($t_p \leq 10$ μs)} \end{array} $	I _D I _D I _{DM}	12 10 45	Adc Apk
Total Power Dissipation @ T _A = 25°C Derate above 25°C Total Power Dissipation @ T _A = 25°C (Note 1) Total Power Dissipation @ T _A = 25°C (Note 2)	P _D	48 0.32 2.1 1.5	W W/°C W W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, L = 1.0 mH $I_{L(pk)}$ = 11 A, V_{DS} = 60 Vdc)	E _{AS}	61	mJ
Thermal Resistance, - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$egin{array}{l} R_{ hetaJC} \ R_{ hetaJA} \ R_{ hetaJA} \end{array}$	3.13 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
- When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
60 V	104 m Ω	12 A



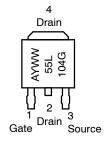


DPAK CASE 369C STYLE 2



IPAK CASE 369D STYLE 2

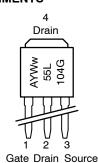
MARKING DIAGRAMS & PIN ASSIGNMENTS



55L104

Υ

WW



= Assembly Location*= Device Code= Year= Work Week

= Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)			60 -	70 62.9	_ _	Vdc mV/°C
Zero Gate Voltage Drain Current $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_J$	= 150°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS}	= ±15 Vdc, V _{DS} = 0 Vdc)	I_{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient Static Drain-to-Source On-Resista	(0 /	V _{GS(th)}	1.0	1.6 4.2	2.0	Vdc mV/°C mΩ
(V _{GS} = 5.0 Vdc, I _D = 6.0 Adc)	(*)	1 100(011)	_	89	104	
Static Drain-to-Source On-Voltage ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 12 \text{ Adc}$) ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 6.0 \text{ Adc}$, T_J	V _{DS(on)}	_ _	0.98 0.86	1.50 –	Vdc	
Forward Transconductance (Note 3	3) (V _{DS} = 8.0 Vdc, I _D = 6.0 Adc)	9FS	-	9.1	_	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	-	316	440	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$	C _{oss}	-	105	150	1
Transfer Capacitance	f = 1.0 MHz)	C _{rss}	-	35	70	1
SWITCHING CHARACTERISTICS (Note 4)					
Turn-On Delay Time		t _{d(on)}	_	9.2	20	ns
Rise Time	(V _{DD} = 30 Vdc, I _D = 12 Adc,	t _r	-	104	210	
Turn-Off Delay Time	$V_{GS} = 5.0 \text{ Vdc}, R_G = 9.1 \Omega) \text{ (Note 3)}$	t _{d(off)}	-	19	40	1
Fall Time		t _f	-	40.5	80	
Gate Charge	0/ 40 \/d= 40 Ad=	Q_{T}	-	7.4	20	nC
	(V _{DS} = 48 Vdc, I _D = 12 Adc, V _{GS} = 5.0 Vdc) (Note 3)	Q ₁	-	2.0	-	
	VGS = 0.0 Vd0) (Note 0)		-	4.0	-	
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
Forward On-Voltage	$(I_S = 12 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 12 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$	V_{SD}	- -	0.95 0.82	1.2 -	Vdc
Reverse Recovery Time	(1. 40 A I.)/ 0)/	t _{rr}	-	35	-	ns
	$(I_S = 12 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, \\ dI_S/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 3)}$	ta	-	21	-	1
	uig/ut = 100 Α/μδ) (Νοτέ 3)	t _b	_	14	-	
Reverse Recovery Stored Charge		Q_{RR}	_	0.04	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

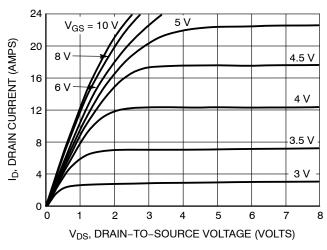


Figure 1. On-Region Characteristics

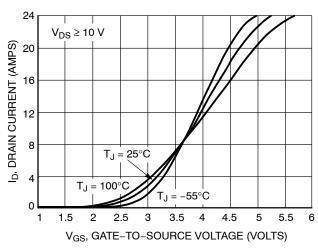


Figure 2. Transfer Characteristics

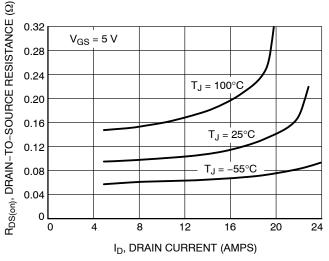


Figure 3. On–Resistance versus Gate–to–Source Voltage

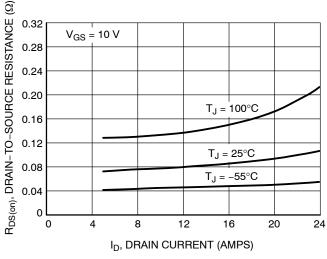


Figure 4. On-Resistance versus Drain Current and Gate Voltage

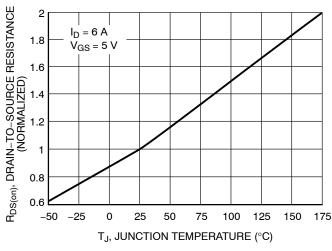


Figure 5. On–Resistance Variation with Temperature

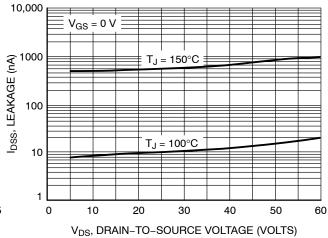


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP} Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 x R_G/(V_{GG} - V_{GSP})$$

$$t_f = Q_2 x R_G/V_{GSP}$$

where

 V_{GG} = the gate drive voltage, which varies from zero to V_{GG} R_G = the gate drive resistance

and Q₂ and V_{GSP} are read from the gate charge curve.

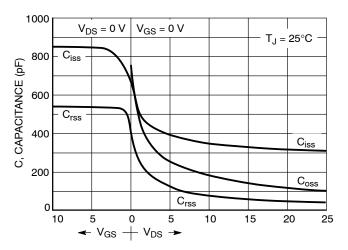
During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$\begin{split} t_{d(on)} &= R_G \ C_{iss} \ In \left[V_{GG} / (V_{GG} - V_{GSP}) \right] \\ t_{d(off)} &= R_G \ C_{iss} \ In \left(V_{GG} / V_{GSP} \right) \end{split}$$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on-state when calculating $t_{d(off)}$.

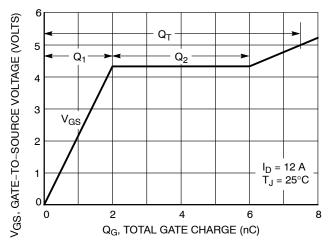
At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation



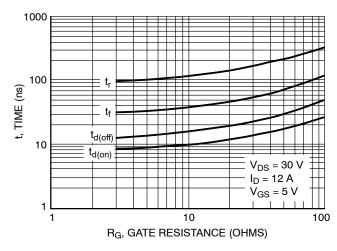


Figure 8. Gate-To-Source and Drain-To-Source
Voltage versus Total Charge

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

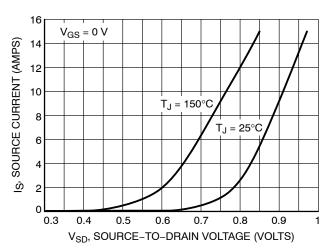


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r , t_f) do not exceed 10 μ s. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_{D}), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_{D} can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

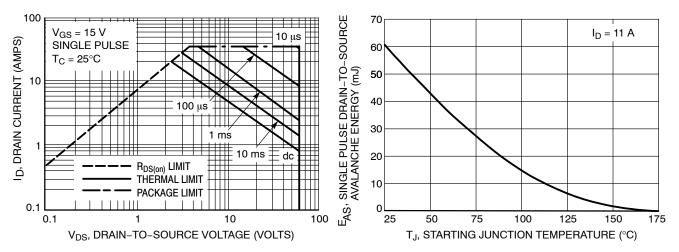


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

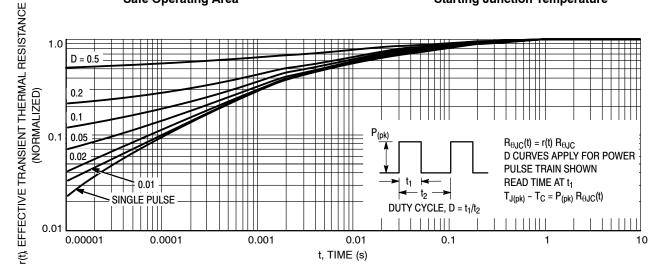


Figure 13. Thermal Response

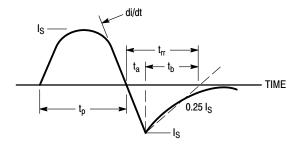


Figure 14. Diode Reverse Recovery Waveform

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD3055L104T4G	DPAK (Pb-Free)	2500 / Tape & Reel
STDV3055L104T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

NTD3055L104G	DPAK (Pb-Free)	75 Units / Rail
NTD3055L104-1G	IPAK (Pb-Free)	75 Units / Rail
NTDV3055L104-1G	IPAK (Pb-Free)	75 Units / Rail
NTDV3055L104T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NTDV and STDV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

^{5.} **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



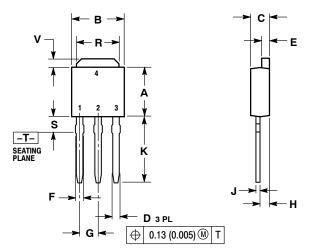


DPAK INSERTION MOUNT

CASE 369 ISSUE O

DATE 02 JAN 2000





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090	BSC	2.29	BSC
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
v	0.030	0.050	0.77	1 27

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:		STYLE 5:		STYLE 6:	
PIN 1.	BASE	PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	GATE	PIN 1.	MT1
2.	COLLECTOR	2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE	2.	MT2
3.	EMITTER	3.	SOURCE	3.	ANODE	3.	GATE	3.	CATHODE	3.	GATE
4.	COLLECTOR	4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE	4.	MT2

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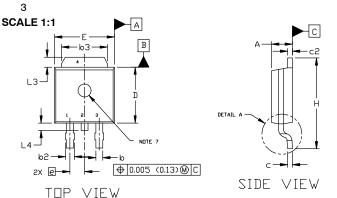
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DPAK (SINGLE GAUGE)

CASE 369C **ISSUE G**

DATE 31 MAY 2023



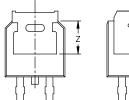


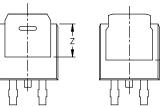
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. L3, AND Z.

 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
 GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
 DIMENSIONS D AND E ARE DETERMINED AT THE
 OUTERMOST EXTREMES OF THE PLASTIC BODY.
 DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
 DETININAL MOLD ESCALUPE.

- OPTIONAL MOLD FEATURE.

DIM	MATEL			
	MIN.	MAX.	MIN.	MAX.
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
_	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4		0.040	-	1.01
Z	0.155		3.93	





BOTTOM VIEW

2.58

[0.102]

1.60

5.80

BOTTOM VIEW AL TERNATE

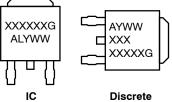
CONSTRUCTIONS [0.228] 6.20 -L2 GAUGE PLANE [0.244] 3.00 FN 1181 DETAIL A ROTATED 90° [0.063]



С

CW





GENERIC MARKING DIAGRAM*

XXXXXX	Davidaa Caala
XXXXXX	= Device Code
Α	= Assembly Location
L	= Wafer Lot
Υ	= Year
WW	= Work Week
G	= Pb-Free Package

[0.243] RECOMMENDED MOUNTING FOOTPRINT*

6.17

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:	STYLE 2:
PIN 1. BASE	PIN 1. GATE
COLLECTOR	DRAIN
3 FMITTER	3 SOURCE

STYLE 7: PIN 1. GATE 2. COLLECTOR

3 FMITTER

4. COLLECTOR

STYLE 3: PIN 1. ANODE 2. CATHODE 3 SOURCE 3 ANODE 4. DRAIN 4. CATHODE

STYLE 8:

STYLE 4: PIN 1. CATHODE 2. ANODE 3 GATE 4. ANODE

3 RESISTOR ADJUST

CATHODE

STYLE 9:

PIN 1. ANODE 2. CATHODE

STYLE 5: PIN 1. GATE 2. ANODE 3 CATHODE ANODE

STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE

4. ANODE

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:

4. COLLECTOR

STYLE 6:

PIN 1. MT1 2. MT2

3 GATE

98AON10527D

PIN 1. N/C 2. CATHODE 3. ANODE

4. CATHODE

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DESCRIPTION:

DPAK (SINGLE GAUGE)

PAGE 1 OF 1

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 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$

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