

MOSFET – Power, Single N-Channel, STD Gate, TCPAK1012

80 V, 0.79 mΩ, 643 A

Preliminary Document NTBYST0D8N08X

Features

- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

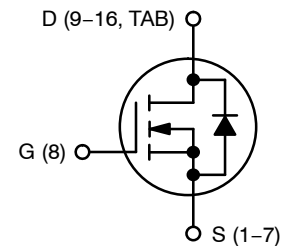
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	80	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	643	A
	T _C = 100 °C		455	
Power Dissipation	T _C = 25 °C	P _D	652	W
Pulsed Drain Current	T _C = 25 °C t _p = 100 μs	I _{DM}	1976	A
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to +175	°C
Continuous Source-Drain Current (Body Diode)		I _S	1097	A
Single Pulse Avalanche Energy (I _{PK} = 132 A)		E _{AS}	871	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)		T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

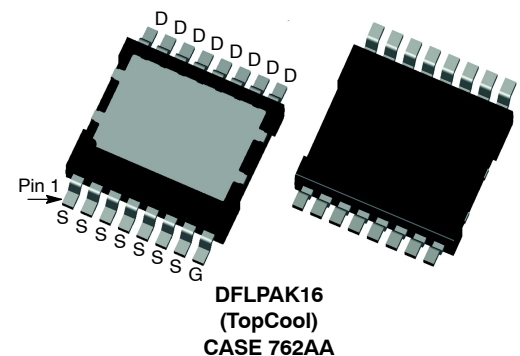
1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} is based on started $T_J = 25^\circ\text{C}$, rated IAS, $V_{DD} = 64 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

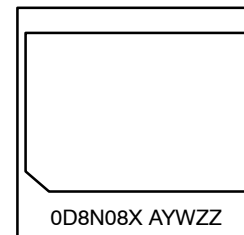
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	0.79 mΩ @ $V_{GS} = 10 \text{ V}$	643 A



N-CHANNEL MOSFET



MARKING DIAGRAM



0D8N08X = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTBYST0D8N08XTXG	TCPAK1012	1500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTBYST0D8N08X

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JC}$	0.23	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	38	
Thermal Characterization Parameter, Junction-to-Source Lead (Pin 1–7)*	Ψ_{JL}	3.9	
Thermal Characterization Parameter, Junction-to-Drain Lead (Pin 9–16)*	Ψ_{JL}	3.3	

* Low thermal conductivity test boards compliant with JEDEC Standard 51-3 for leaded surface-mount packages. 1s0p PCB board with a 1 in² copper plane, tested under natural convection conditions.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		37		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 80\text{ V}, T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_J = 25^\circ\text{C}$		0.67	0.79	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 703\text{ μA}, T_J = 25^\circ\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 703\text{ μA}$		–7.5		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 80\text{ A}$		324		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		13097		pF
Output Capacitance	C_{OSS}			3744		
Reverse Transfer Capacitance	C_{RSS}			56		
Output Charge	Q_{OSS}			268		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 40\text{ V}, I_D = 80\text{ A}, V_{GS} = 10\text{ V}$		182		nC
Threshold Gate Charge	$Q_{G(TH)}$			40		
Gate-to-Source Charge	Q_{GS}			59		
Gate-to-Drain Charge	Q_{GD}			28		
Gate Plateau Voltage	V_{GP}			4.6		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.26		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}$, $V_{DD} = 64\text{ V}, I_D = 80\text{ A}$, $R_G = 2.5\text{ Ω}$		50		ns
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(OFF)}$			86		
Fall Time	t_f			14		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$I_S = 80\text{ A}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$		0.79	1.2	V
		$I_S = 80\text{ A}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		0.63		

NTBYST0D8N08X

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $I_S = 80\text{ A}$, $di/dt = 1000\text{ A}/\mu\text{s}$, $V_{DD} = 64\text{ V}$		55		ns
Charge Time	t_a			28		
Discharge Time	t_b			27		
Reverse Recovery Charge	Q_{RR}			609		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

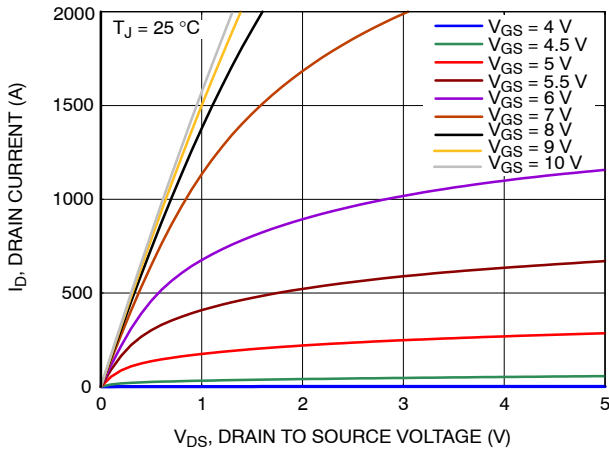


Figure 1. On-Region Characteristics

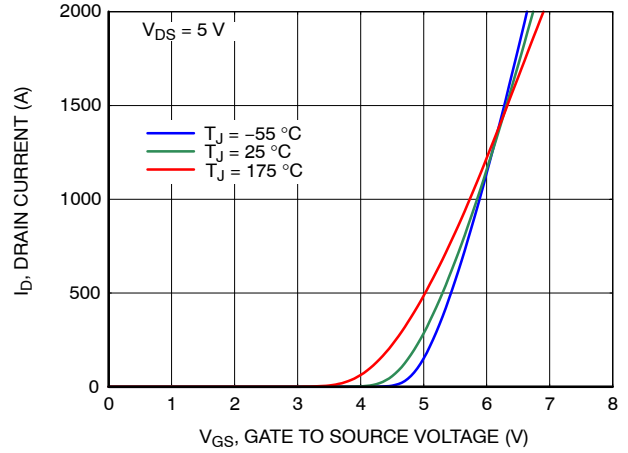


Figure 2. Transfer Characteristics

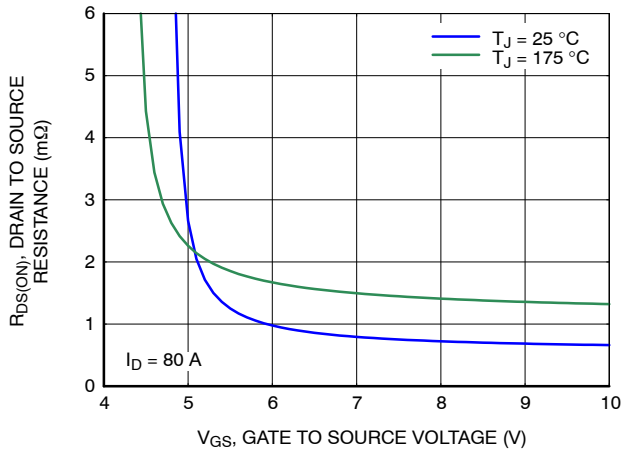


Figure 3. On-Resistance vs. Gate Voltage

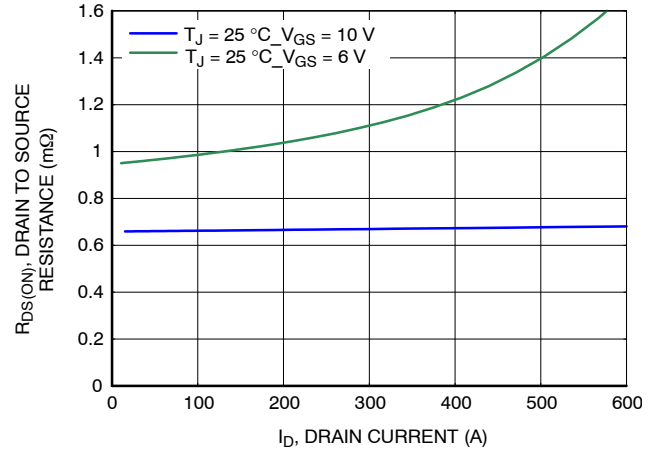


Figure 4. On-Resistance vs. Drain Current

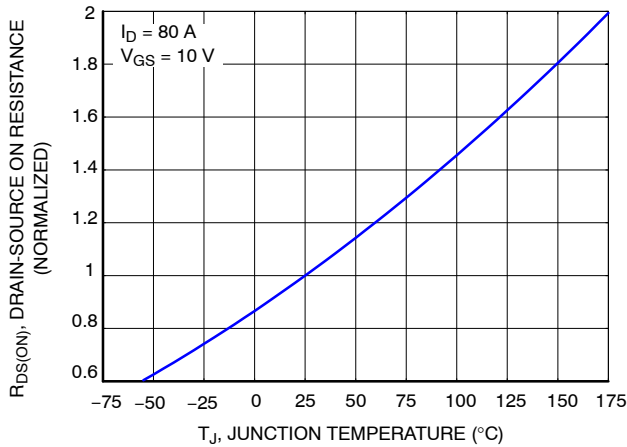


Figure 5. Normalized ON Resistance vs. Junction Temperature

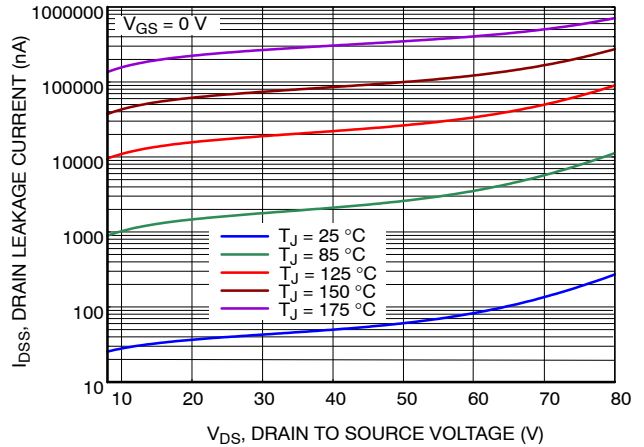


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS (continued)

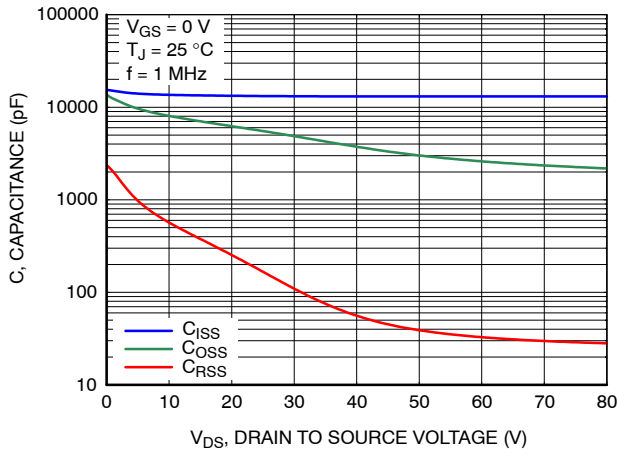


Figure 7. Capacitance Characteristics

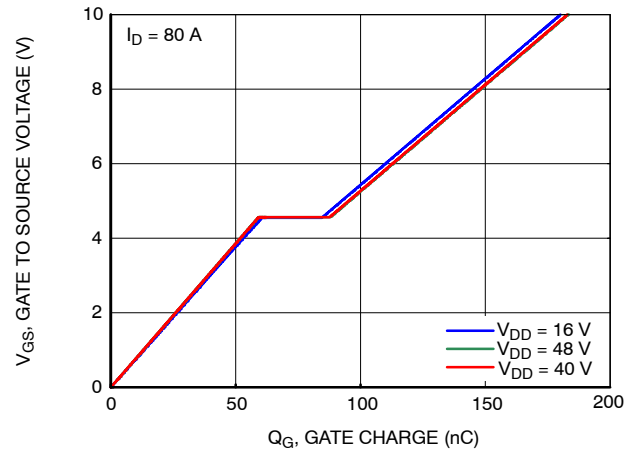


Figure 8. Gate Charge Characteristics

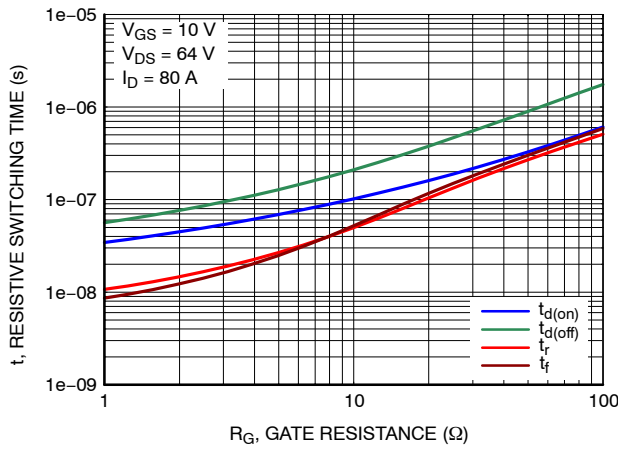


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

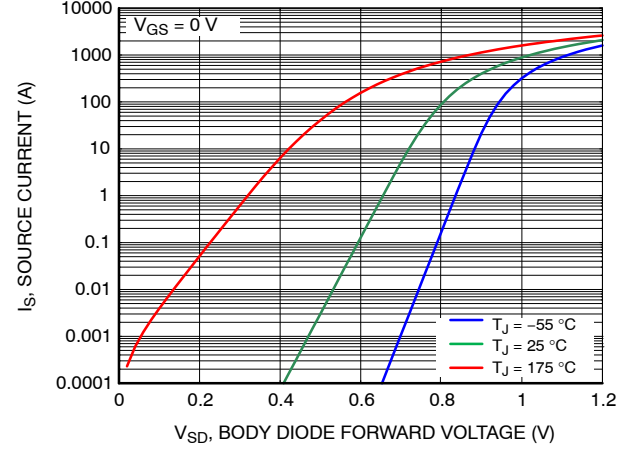


Figure 10. Diode Forward Characteristics

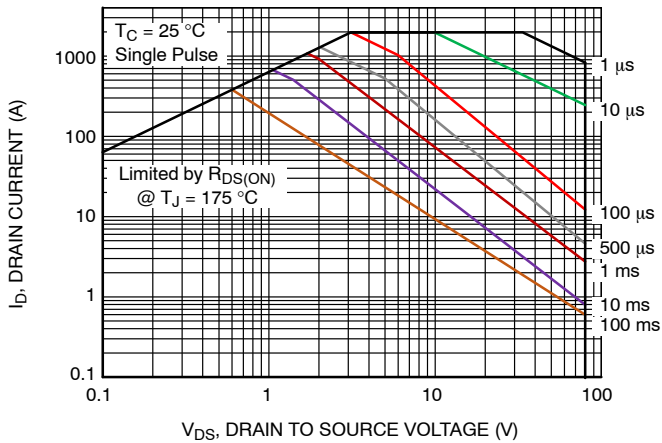


Figure 11. Safe Operating Area (SOA)

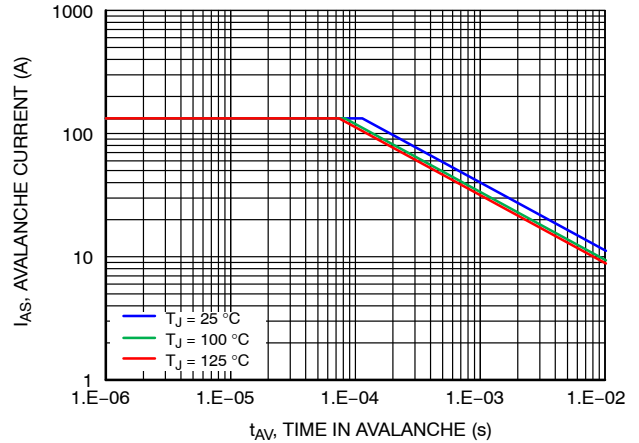


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS (continued)

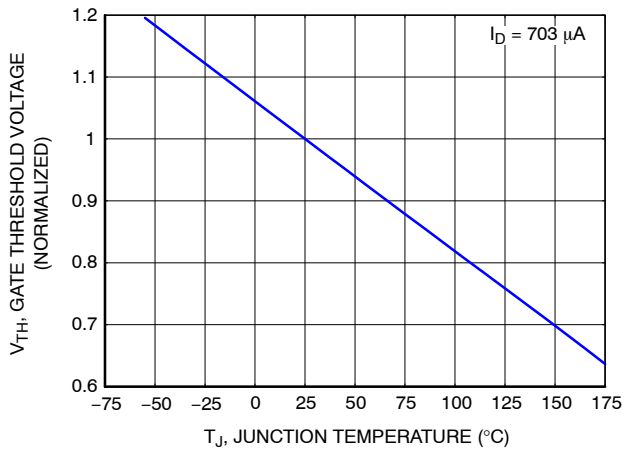


Figure 13. Gate Threshold Voltage vs. Junction Temperature

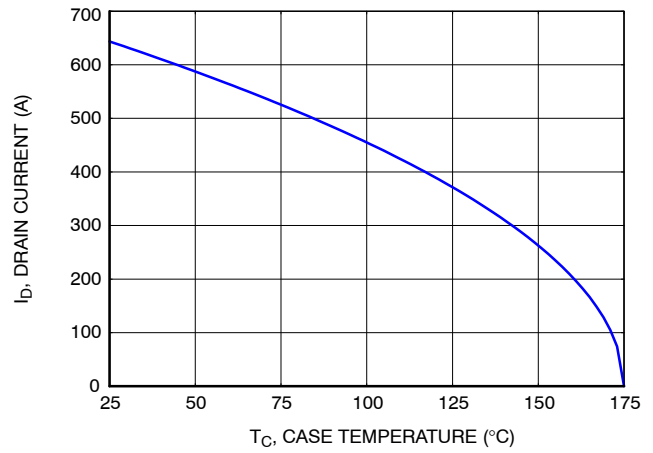


Figure 14. Maximum Current vs. Case Temperature

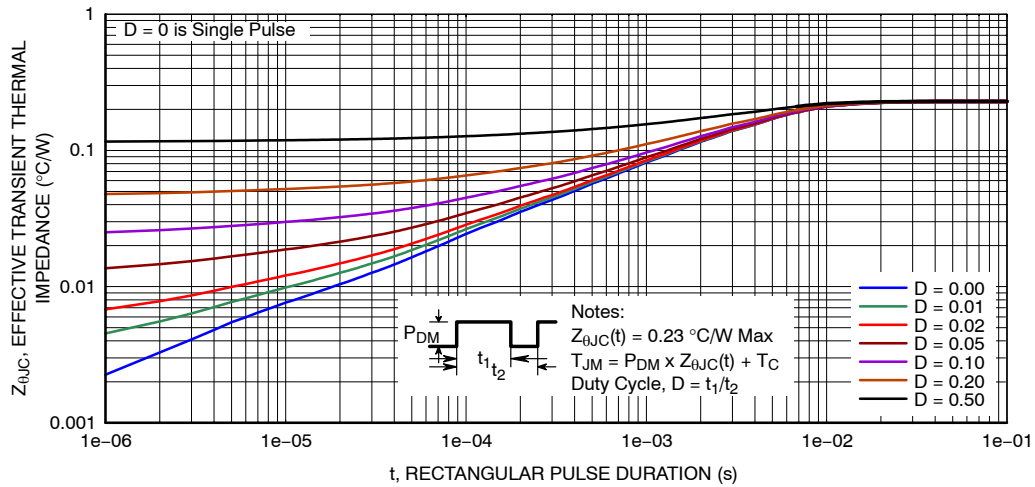


Figure 15. Transient Thermal Response

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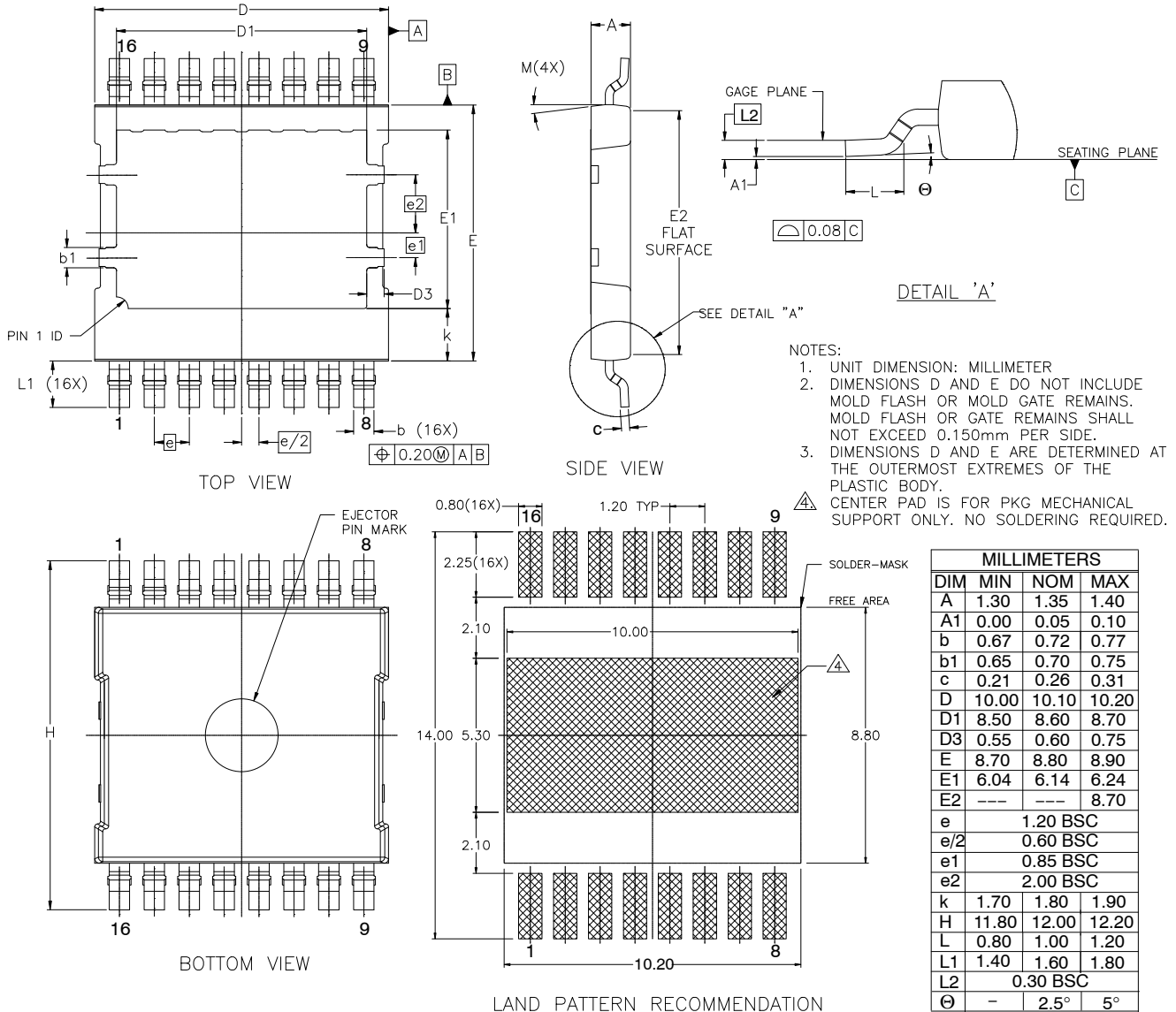
REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	8/18/2026
P1	Updated the OPN to NTBYST0D8N08XTXG.	8/26/2026

NTBYST0D8N08X

PACKAGE DIMENSIONS

TCPAK16 8.80x10.10, 1.20P (TCPAK1012) CASE 762AA ISSUE E



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