

MOSFET - Power, Single N-Channel, TOLL

80 V, 2 mΩ, 238 A

NTBLS002N08MC

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	80	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	I _D	238	A
Power Dissipation R _{θJC} (Note 2)			P _D	208	W
Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	I _D	28	A
Power Dissipation R _{θJA} (Notes 1, 2)			P _D	2.9	W
Pulsed Drain Current	T _C = 25°C, t _p = 10 μs		I _{DM}	3523	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 28 A, L = 3 mH)			E _{AS}	1176	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

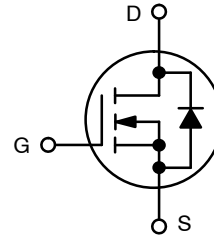
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.6	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	43	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	2 mΩ @ 10 V	238 A
	5 mΩ @ 6 V	

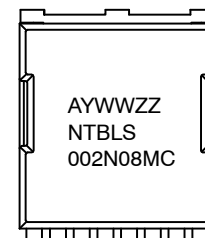


N-CHANNEL MOSFET



M0-299A
TOLL
CASE 100CU

MARKING DIAGRAM



NTBLS002N08MC = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NTBLS002N08MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, ref to 25°C		64		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C		1	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 530 μA	2.0	3.0	4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 530 μA, ref to 25°C		-8.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 80 A		1.7	2.0	mΩ
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 6 V, I _D = 47 A		2.8	5.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 80 A		186		S
Gate Resistance	R _G	T _A = 25°C		0.4		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 40 V		6580		pF
Output Capacitance	C _{OSS}			1950		
Reverse Transfer Capacitance	C _{RSS}			74		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 40 V; I _D = 80 A		92		nC
Threshold Gate Charge	Q _{G(TH)}			19		
Gate-to-Source Charge	Q _{GS}			30		
Gate-to-Drain Charge	Q _{GD}			21		
Output Charge	Q _{OSS}			123		
Sync Charge	Q _{sync}			81		
Plateau Voltage	V _{plateau}			5		V

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 80 A, R _G = 6 Ω		34		ns
Rise Time	t _r			30		
Turn-Off Delay Time	t _{d(OFF)}			62		
Fall Time	t _f			24		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2 A		0.7	1.2	V
		V _{GS} = 0 V, I _S = 80 A		0.8	1.3	
Reverse Recovery Time	t _{RR}	I _F = 40 A, di/dt = 300 A/μs		35		nS
Reverse Recovery Charge	Q _{RR}			74		nC
Reverse Recovery Time	t _{RR}	I _F = 40 A, di/dt = 1000 A/μs		27		nS
Reverse Recovery Charge	Q _{RR}			166		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

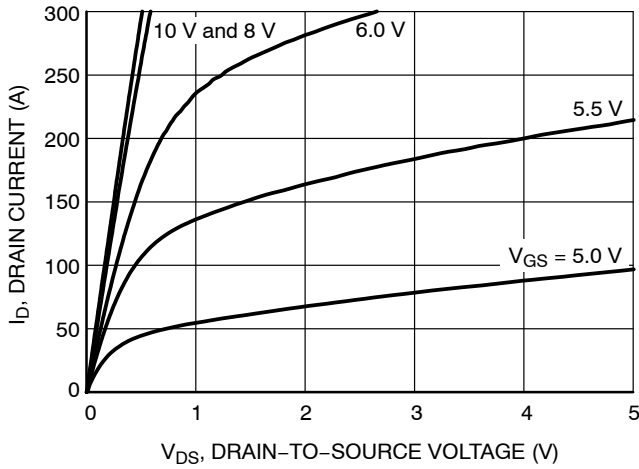


Figure 1. On-Region Characteristics

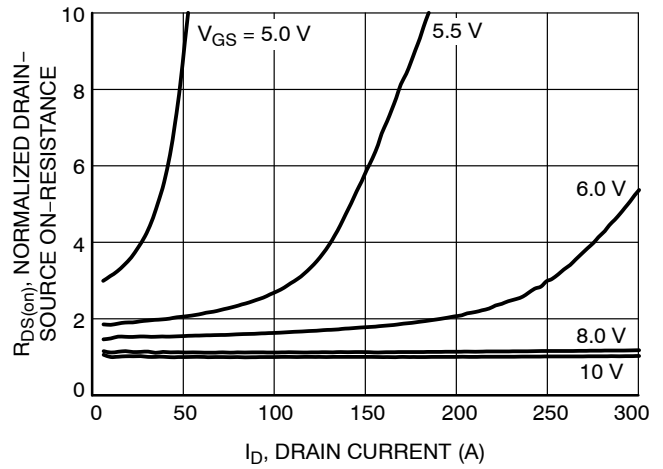


Figure 2. $R_{DS(on)}$ Normalized vs. I_D

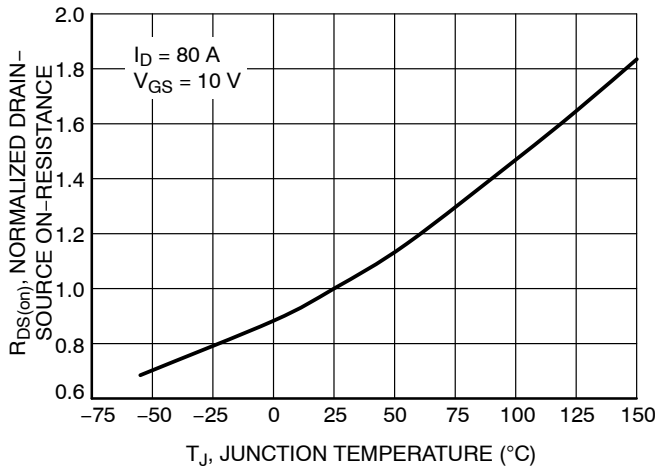


Figure 3. $R_{DS(on)}$ vs. Junction Temperature

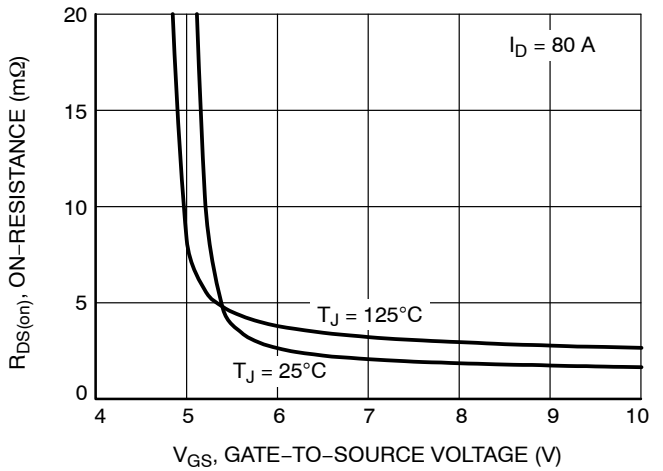


Figure 4. On-Resistance vs. Gate-to-Source Voltage

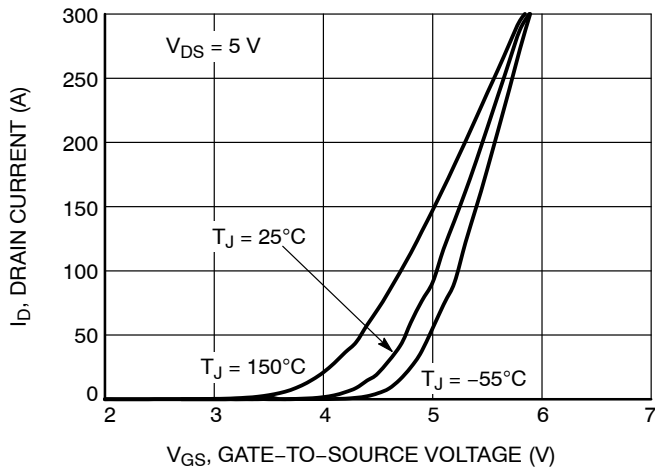


Figure 5. Drain Current vs. Gate-to-Source Voltage

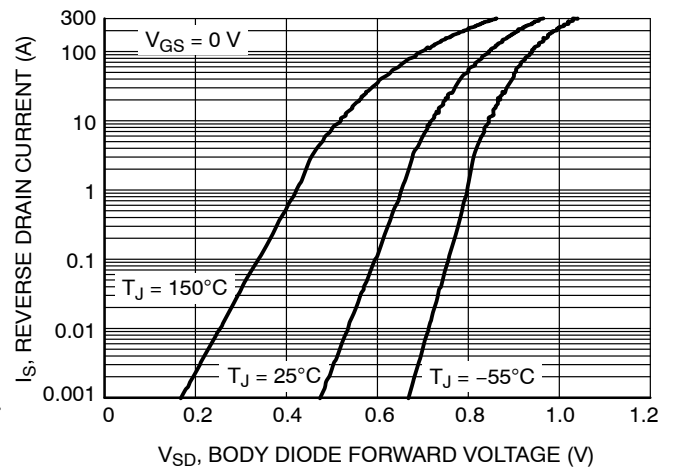


Figure 6. Reverse Drain Current vs. Body Diode Forward Voltage

TYPICAL CHARACTERISTICS

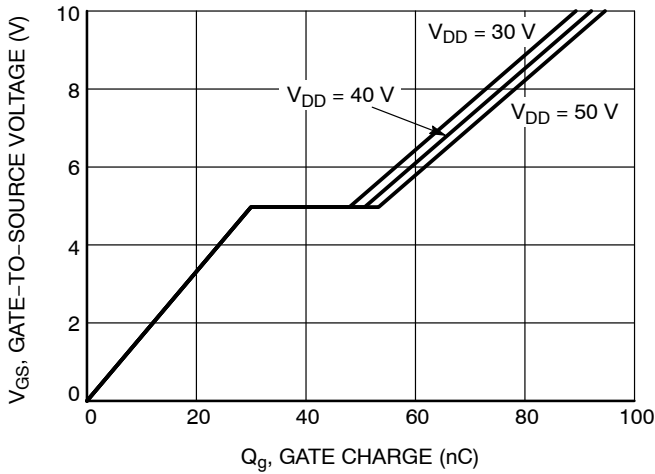


Figure 7. Gate Charge

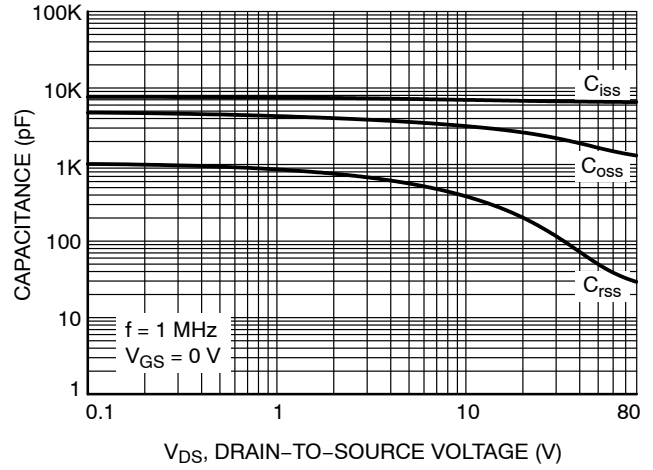


Figure 8. Capacitance Variation

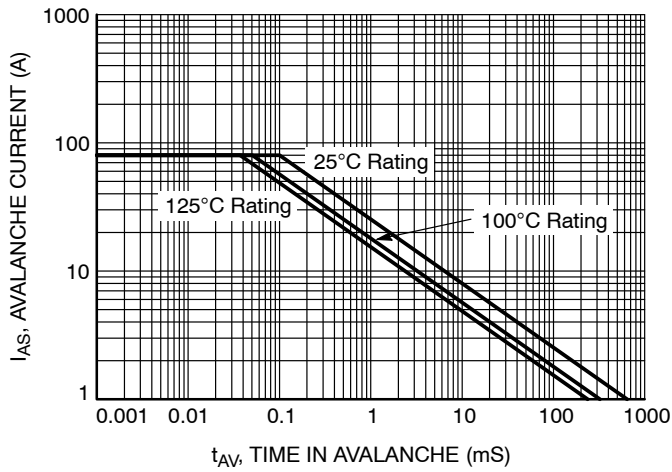


Figure 9. UIL

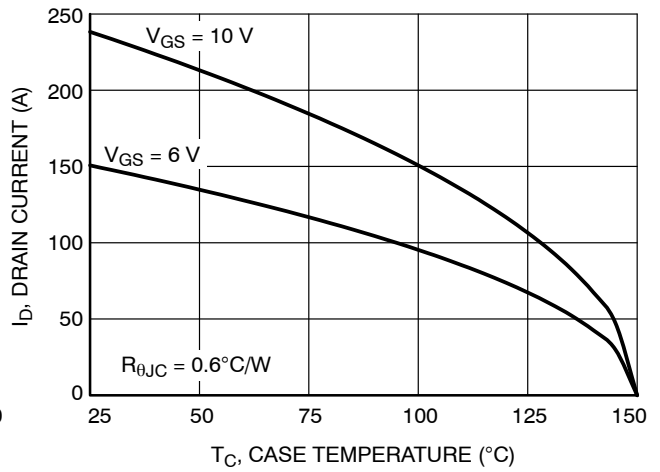


Figure 10. Drain Current vs. Case Temperature

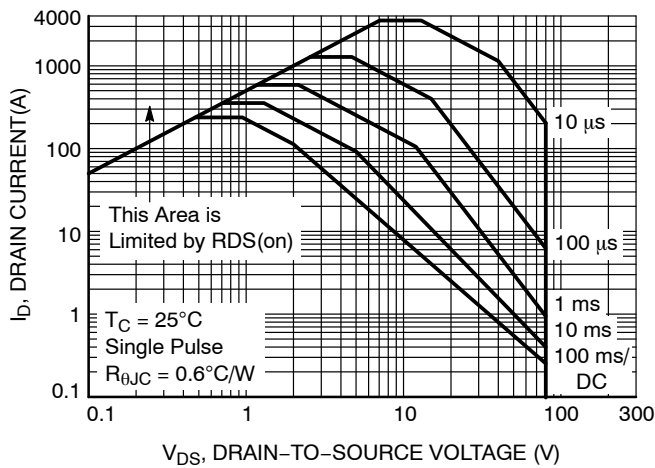


Figure 11. Maximum Rated Forward Biased Safe Operating Area

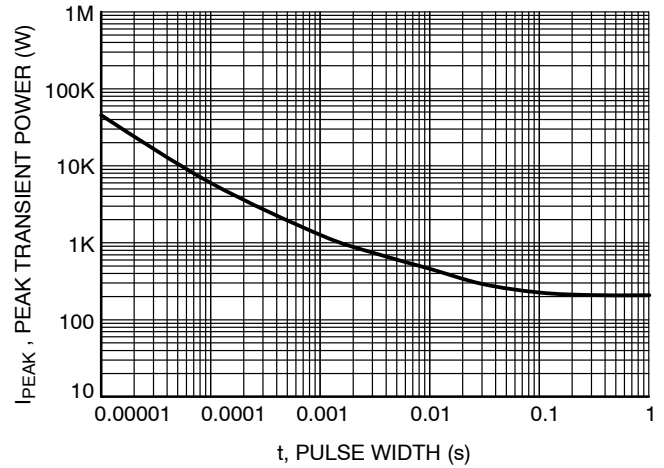


Figure 12. Peak Power

NTBLS002N08MC

TYPICAL CHARACTERISTICS

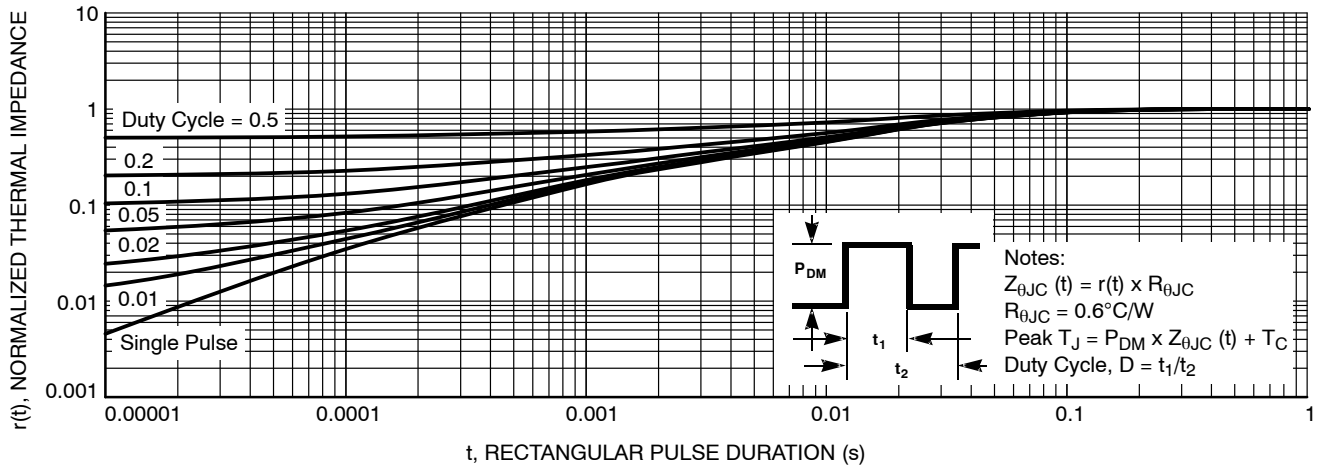
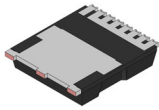


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

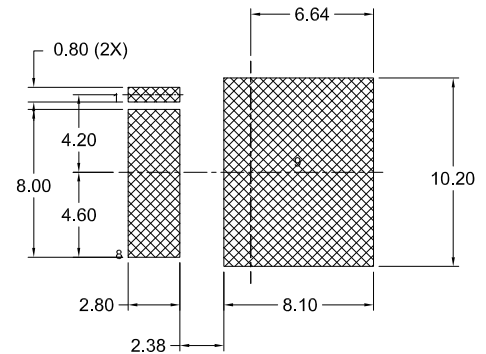
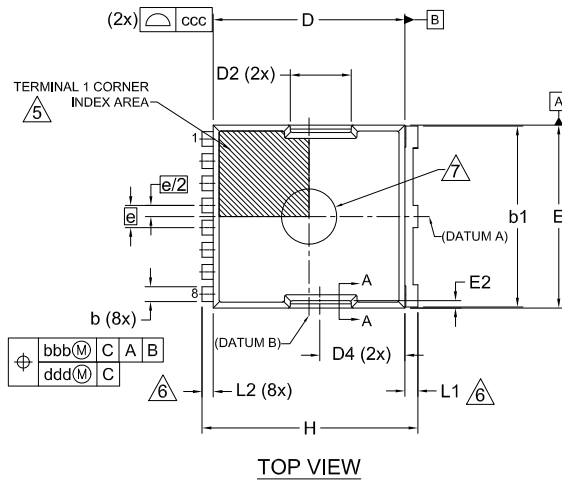
Device	Marking	Package	Shipping [†]
NTBLS002N08MC	NTBLS 002N08MC	M0-299A (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

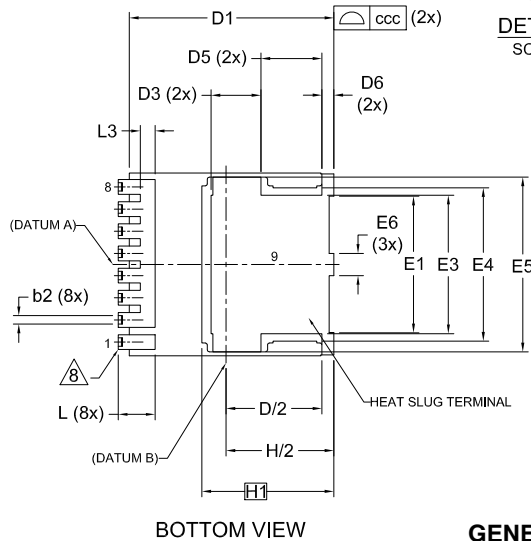
DATE 30 JUL 2024



*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

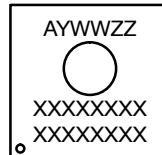


- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 3. "e" REPRESENTS THE TERMINAL PITCH.
 4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
 5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
 6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
 7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
 8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



GENERIC
MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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DESCRIPTION: H-PSOF8L 11.68x9.80x2.30, 1.20P

PAGE 1 OF 1

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