

# Silicon Carbide (SiC) MOSFET - EliteSiC, 16 mohm 650 V, M3S, TOLL

## NTBL016N065M3S

### Features

- Typical  $R_{DS(on)}$  = 16 m $\Omega$  @  $V_{GS} = 18$  V
- Ultra Low Gate Charge ( $Q_{G(tot)} = 104$  nC)
- High Speed Switching with Low Capacitance ( $C_{OSS} = 195$  pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Applications

- SMPS, Solar Inverters, UPS, Energy Storage, EV Charging Infrastructure

### MAXIMUM RATINGS ( $T_J = 25$ °C unless otherwise noted)

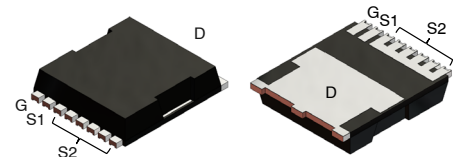
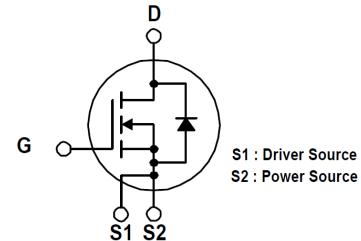
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	650	V
Gate-to-Source Voltage	$V_{GS}$	-10/+22.6	V
Continuous Drain Current	$T_C = 25$ °C	$I_D$	103 A
Power Dissipation		$P_D$	416 W
Continuous Drain Current	$T_C = 100$ °C	$I_D$	74 A
Power Dissipation		$P_D$	208 W
Pulsed Drain Current (Note 1)	$T_C = 25$ °C $t_p = 100$ $\mu$ s	$I_{DM}$	225 A
Continuous Source-Drain Current (Body Diode)	$T_C = 25$ °C $V_{GS} = -3$ V	$I_S$	63
	$T_C = 100$ °C $V_{GS} = -3$ V		35
Pulsed Source-Drain Current (Body Diode) (Note 1)	$T_C = 25$ °C $V_{GS} = -3$ V $t_p = 100$ $\mu$ s	$I_{SM}$	243
Single Pulse Avalanche Energy ( $I_{LPK} = 52$ A, $L = 0.1$ mH) (Note 2)	$E_{AS}$	135	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Single pulse, limited by max junction temperature.
2. EAS of 135 mJ is based on starting  $T_J = 25$  °C,  $L = 0.1$  mH,  $I_{AS} = 52$  A,  $V_{DD} = 100$  V,  $V_{GS} = 18$  V.

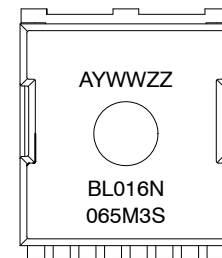
$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
650 V	16 m $\Omega$ @ $V_{GS} = 18$ V	103 A

### N-Channel MOSFET



H-PSOF8L  
CASE 100DC

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code  
BL016N065M3S = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTBL016N065M3S	H-PSOF8L	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

# NTBL016N065M3S

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 3)	$R_{\theta JC}$	0.36	$^{\circ}\text{C}/\text{W}$

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operation Values of Gate-to-Source Voltage	$V_{GSop}$	-3/+18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^{\circ}\text{C}$	650	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$ , Referenced to $25^{\circ}\text{C}$ (Note 5)	-	87	-	$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650\text{ V}, T_J = 25^{\circ}\text{C}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 650\text{ V}, T_J = 175^{\circ}\text{C}$ (Note 5)	-	-	500	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = -10\text{ V}, V_{DS} = 0\text{ V}$	-1.0	-	-	$\mu\text{A}$
		$V_{GS} = +22.6\text{ V}, V_{DS} = 0\text{ V}$	-	-	+1.0	$\mu\text{A}$

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 30\text{ A}, T_J = 25^{\circ}\text{C}$	-	16	23.5	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}, I_D = 30\text{ A}, T_J = 175^{\circ}\text{C}$ (Note 5)	-	26	-	
		$V_{GS} = 15\text{ V}, I_D = 30\text{ A}, T_J = 25^{\circ}\text{C}$	-	22	-	
		$V_{GS} = 15\text{ V}, I_D = 30\text{ A}, T_J = 175^{\circ}\text{C}$ (Note 5)	-	29	-	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 15\text{ mA}, T_J = 25^{\circ}\text{C}$	2.0	2.7	4.0	V
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 30\text{ A}$ (Note 5)	-	27	-	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ (Note 5)	-	2305	-	$\text{pF}$
Output Capacitance	$C_{OSS}$		-	195	-	
Reverse Transfer Capacitance	$C_{RSS}$		-	16	-	
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 400\text{ V}, I_D = 30\text{ A}, V_{GS} = -3/18\text{ V}$ (Note 5)	-	104	-	$\text{nC}$
Gate-to-Source Charge	$Q_{GS}$		-	25	-	
Gate-to-Drain Charge	$Q_{GD}$		-	26	-	
Gate Resistance	$R_G$	$f = 1\text{ MHz}$	-	3.4	-	$\Omega$

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -3/18\text{ V}$ , $V_{DD} = 400\text{ V}$ , $I_D = 30\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $T_J = 25\text{ }^\circ\text{C}$ . $L_{stray} = 11\text{ nH}$ (Notes 4, 5)	-	17	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	42	-	
Rise Time	$t_r$		-	15	-	
Fall Time	$t_f$		-	10	-	
Turn-On Switching Loss	$E_{ON}$		-	167	-	$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$		-	67	-	
Total Switching Loss	$E_{TOT}$		-	234	-	
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -3/18\text{ V}$ , $V_{DD} = 400\text{ V}$ , $I_D = 30\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $T_J = 175\text{ }^\circ\text{C}$ . $L_{stray} = 11\text{ nH}$ (Notes 4, 5)	-	13	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	51	-	
Rise Time	$t_r$		-	17	-	
Fall Time	$t_f$		-	12	-	
Turn-On Switching Loss	$E_{ON}$		-	174	-	$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$		-	79	-	
Total Switching Loss	$E_{TOT}$		-	253	-	

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$I_{SD} = 30\text{ A}$ , $V_{GS} = -3\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	4.6	6.0	V
		$I_{SD} = 30\text{ A}$ , $V_{GS} = -3\text{ V}$ , $T_J = 175\text{ }^\circ\text{C}$ (Note 5)	-	4.3	-	
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -3\text{ V}$ , $I_S = 30\text{ A}$ , $di/dt = 1000\text{ A}/\mu\text{s}$ , $V_{DS} = 400\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ (Note 5)	-	21	-	ns
Charge Time	$t_a$		-	13	-	
Discharge Time	$t_b$		-	8.4	-	
Reverse Recovery Charge	$Q_{RR}$		-	130	-	nC
Reverse Recovery Energy	$E_{REC}$		-	8.9	-	$\mu\text{J}$
Peak Reverse Recovery Current	$I_{RRM}$		-	12	-	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. EON/EOFF result is with body diode.

5. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

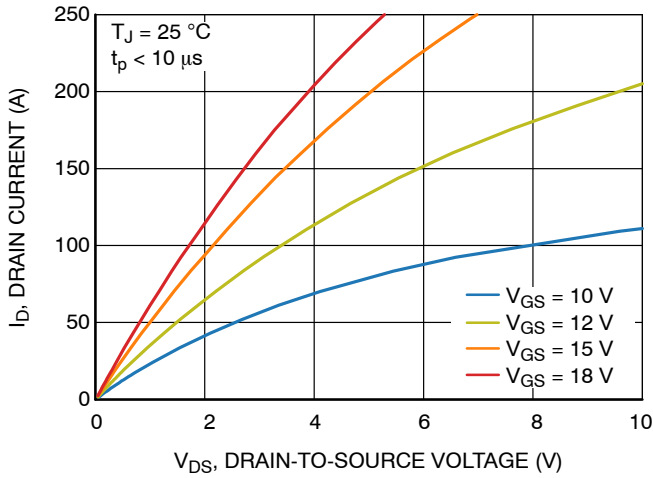


Figure 1. Output Characteristics

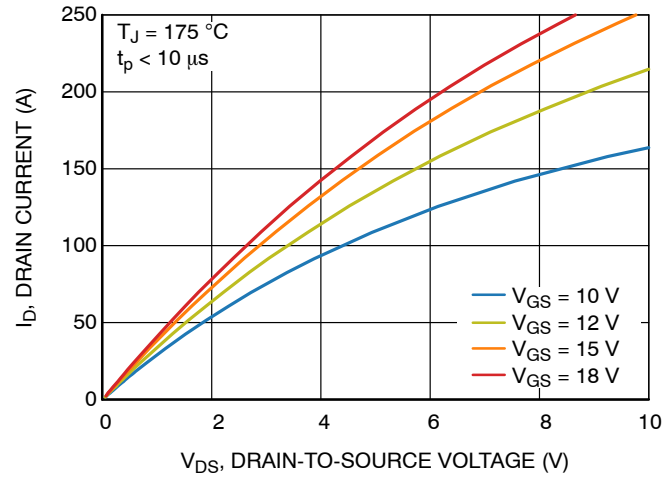


Figure 2. Output Characteristics

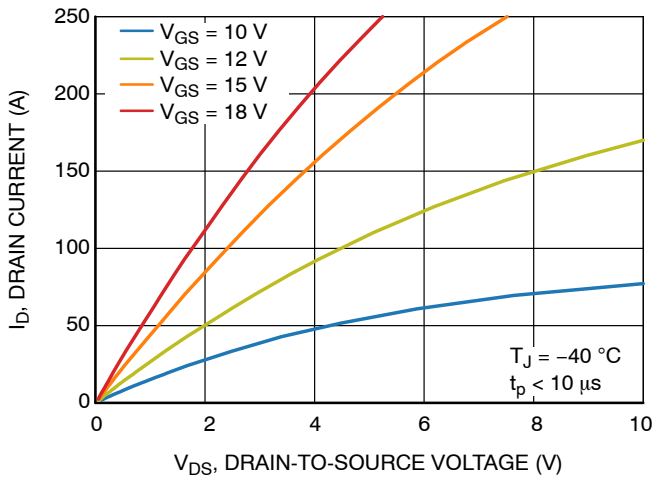


Figure 3. Output Characteristics

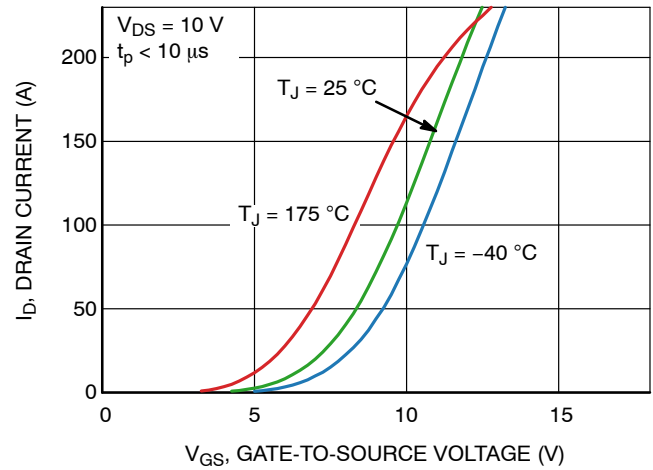


Figure 4. Transfer Characteristics

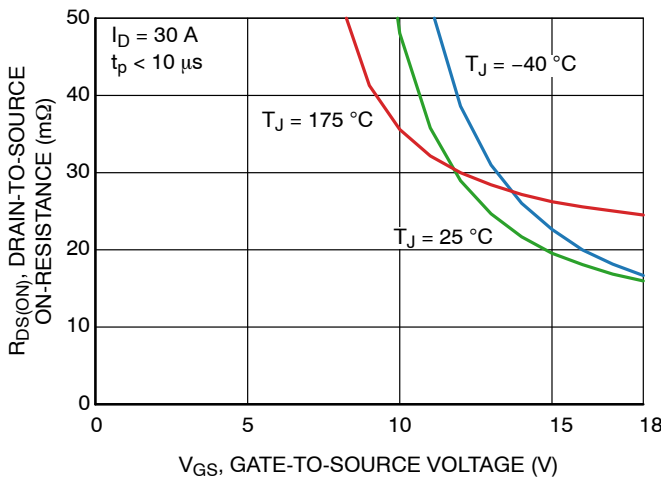


Figure 5. On-Resistance vs Gate Voltage

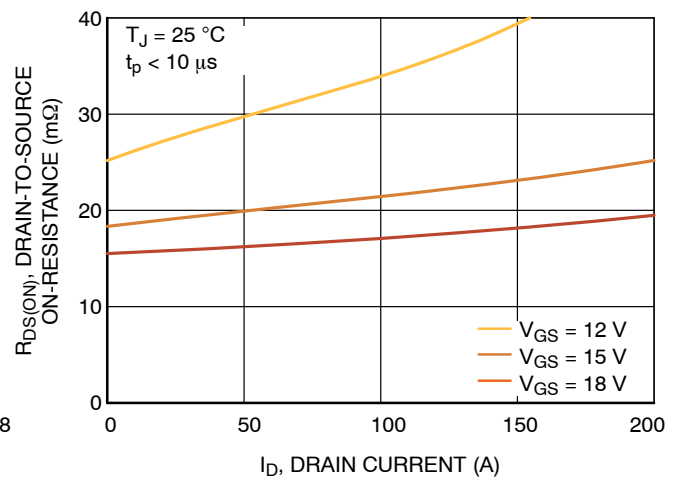


Figure 6. On-Resistance vs Drain Current

TYPICAL CHARACTERISTICS

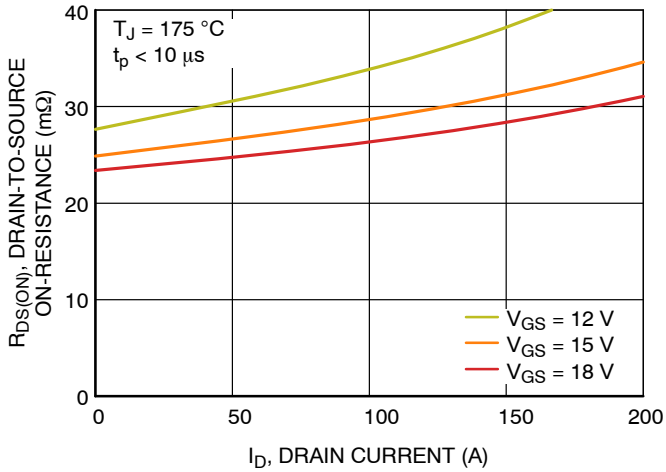


Figure 7. On-Resistance vs Drain Current

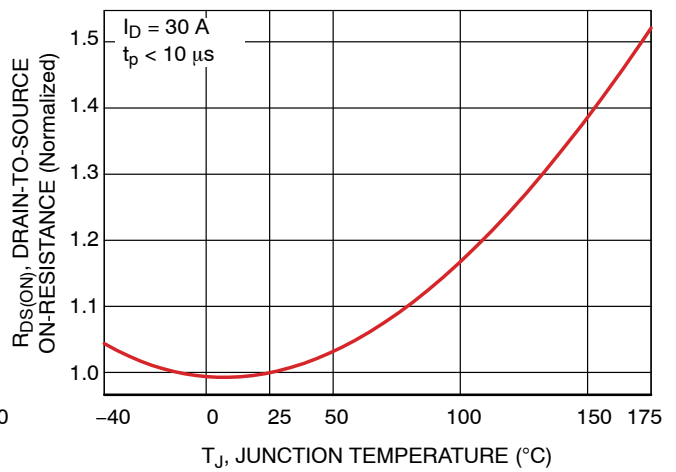


Figure 8. On-Resistance vs Junction Temperature

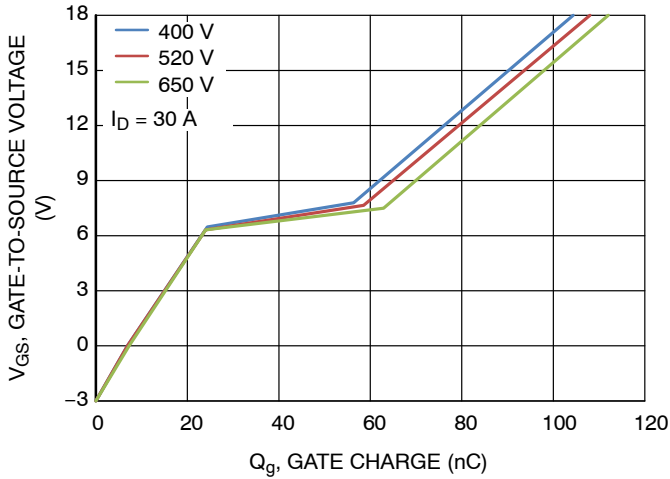


Figure 9. Gate Charge Characteristics

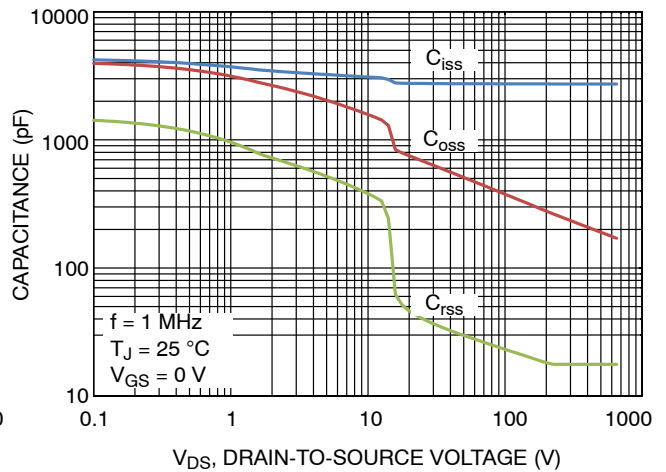


Figure 10. Capacitance Characteristics

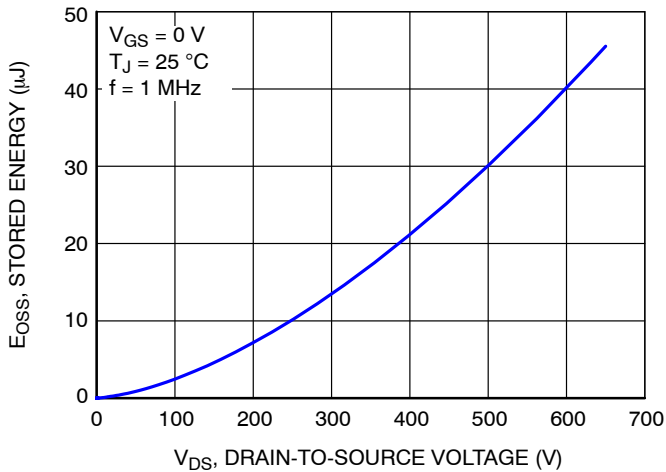


Figure 11. Stored energy vs Drain to Source Voltage

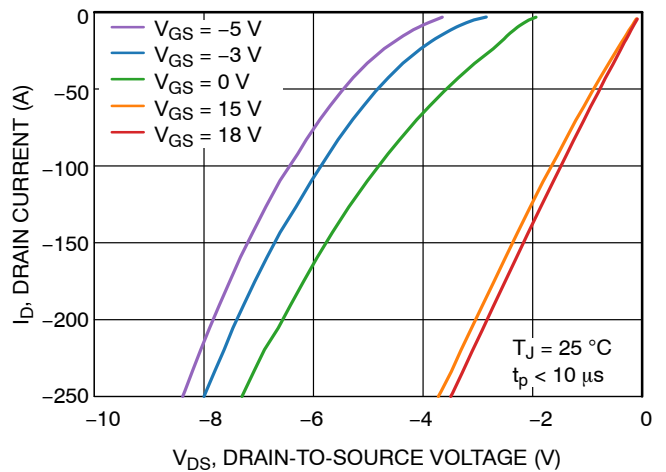


Figure 12. Reverse Conduction Characteristics

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## TYPICAL CHARACTERISTICS

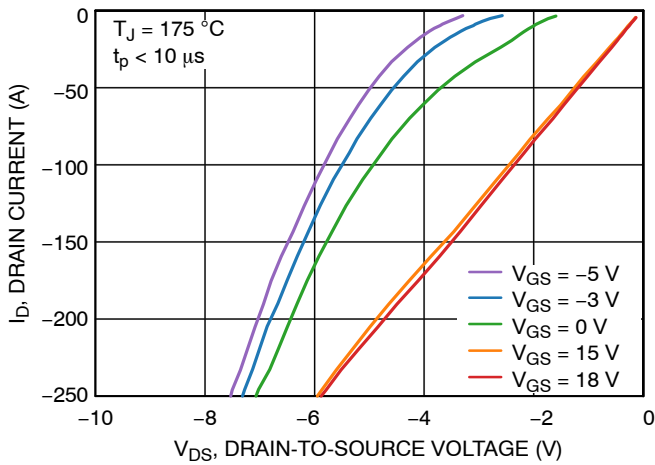


Figure 13. Reverse Conduction Characteristics

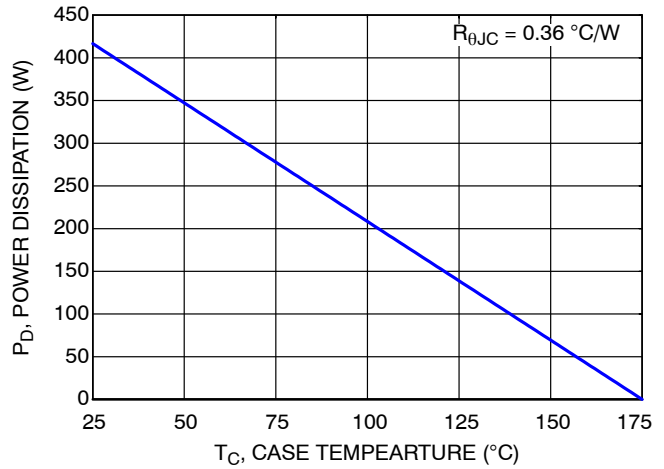


Figure 14. Maximum Power Dissipation vs Case Temperature

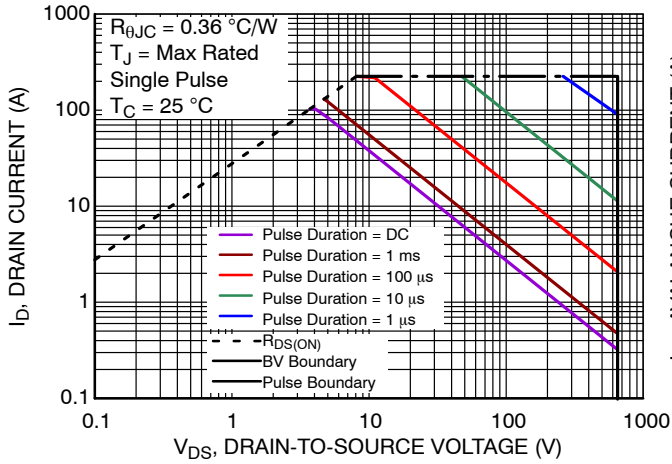


Figure 15. Safe Operating Area

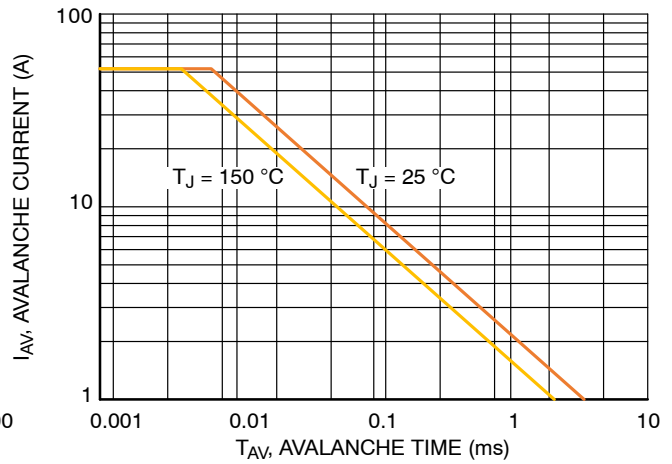


Figure 16. Avalanche Current vs. Pulse Time (UIS)

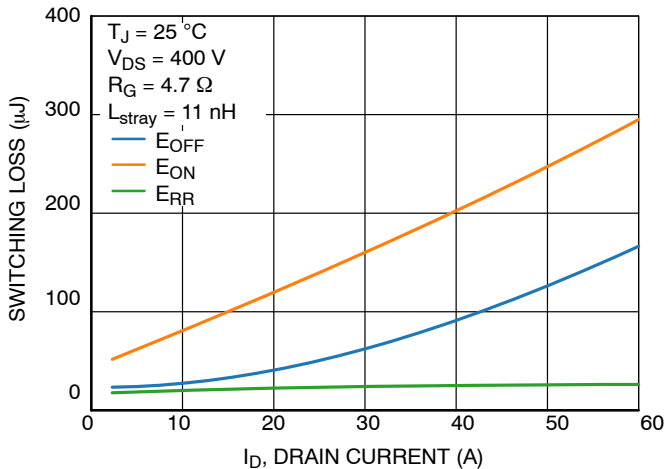


Figure 17. Inductive Switching Loss vs. Drain Current

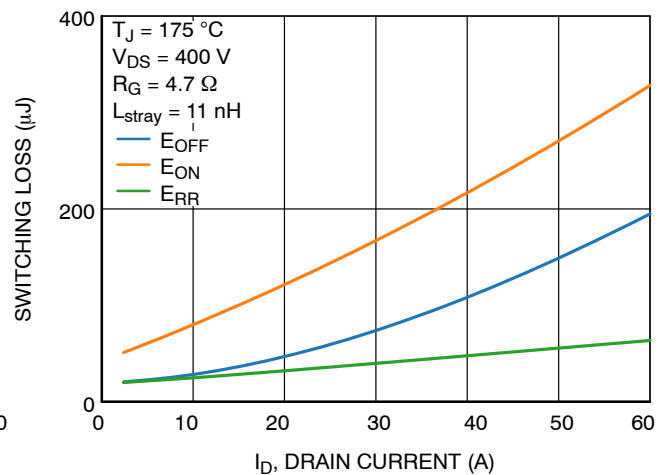


Figure 18. Inductive Switching Loss vs. Drain Current

TYPICAL CHARACTERISTICS

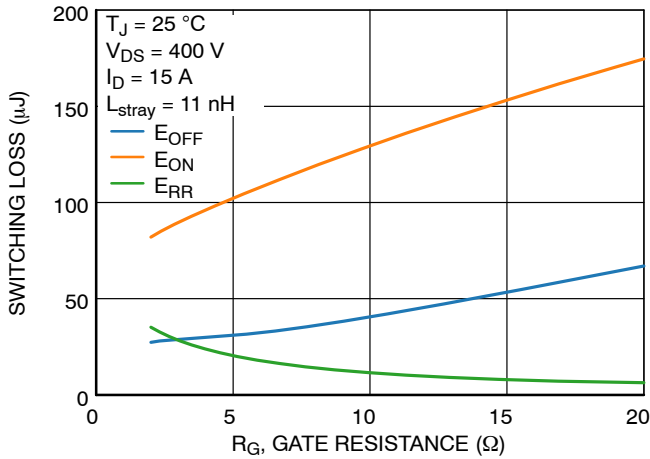


Figure 19. Inductive Switching Loss vs. Gate Resistance

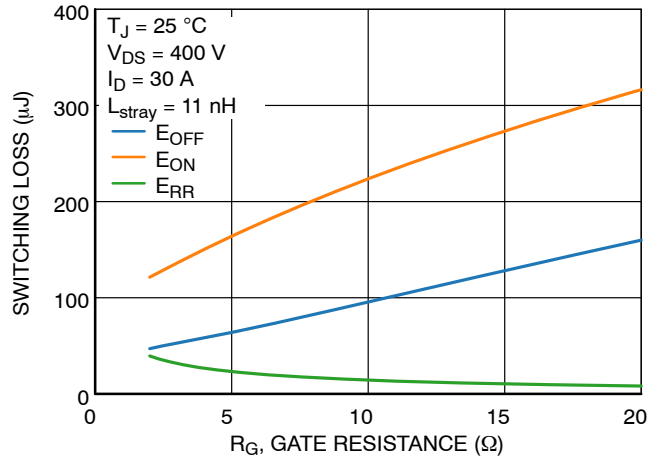


Figure 20. Inductive Switching Loss vs. Gate Resistance

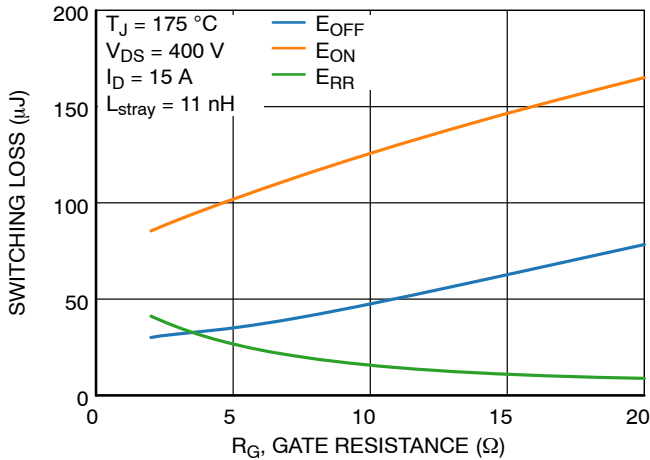


Figure 21. Inductive Switching Loss vs. Gate Resistance

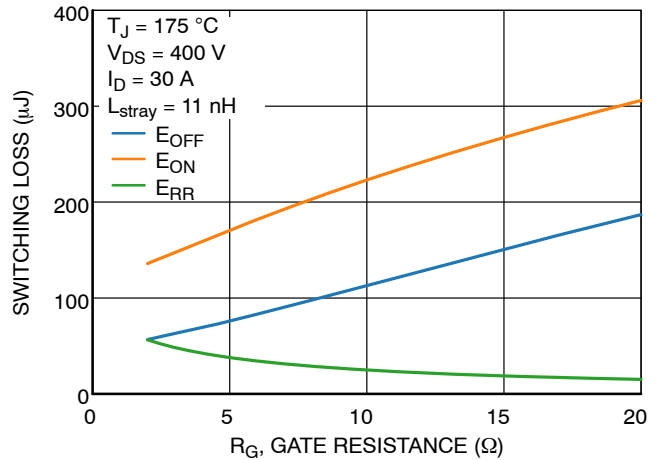


Figure 22. Inductive Switching Loss vs. Gate Resistance

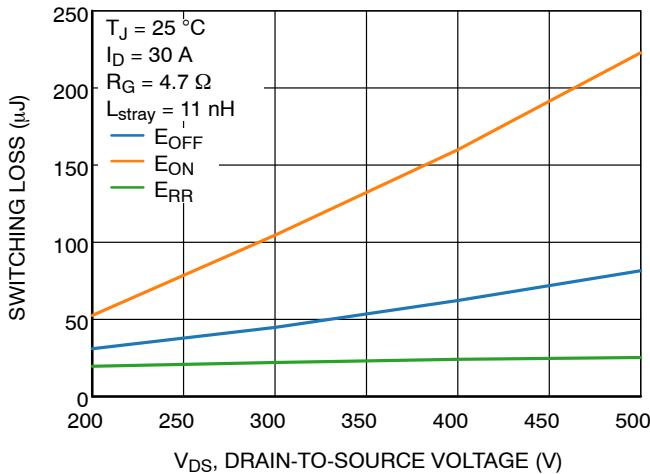


Figure 23. Inductive Switching Loss vs. Drain Voltage

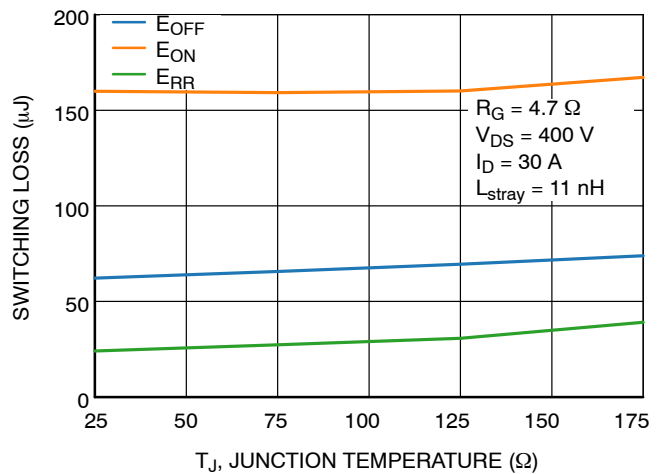
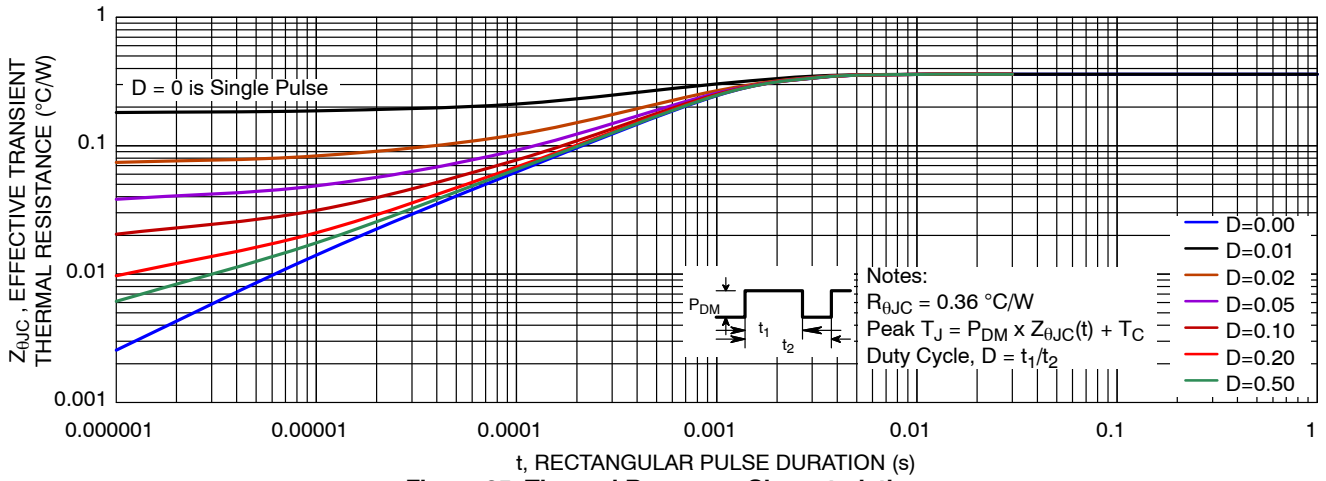


Figure 24. Inductive Switching Loss vs. Junction Temperature

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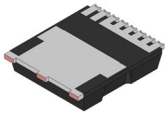
**Figure 25. Thermal Response Characteristics**

# NTBL016N065M3S

## REVISION HISTORY

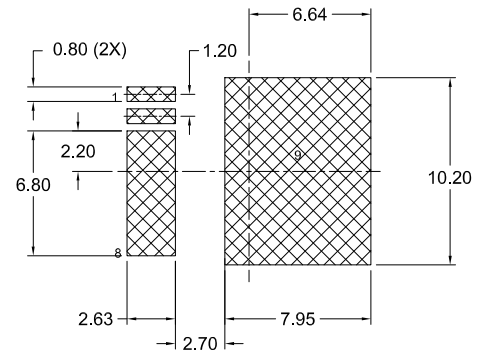
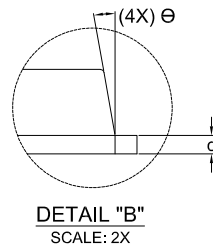
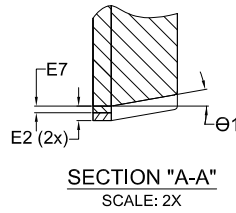
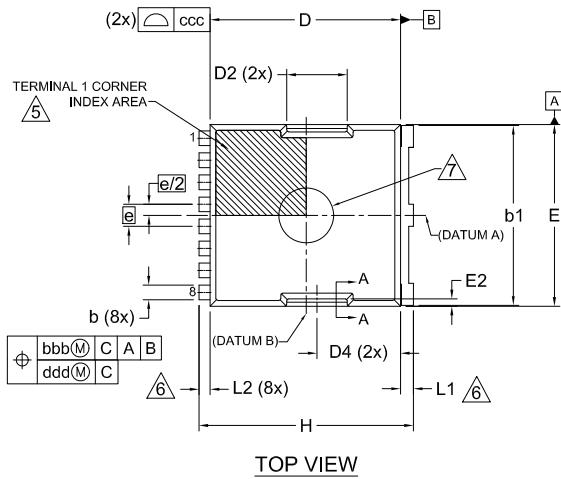
Revision	Description of Changes	Date
0	Initial document release.	1/21/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

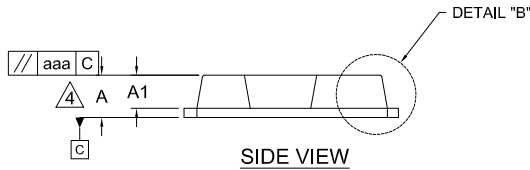


H-PSOF8L 9.90x10.38x2.30, 1.20P  
CASE 100DC  
ISSUE D

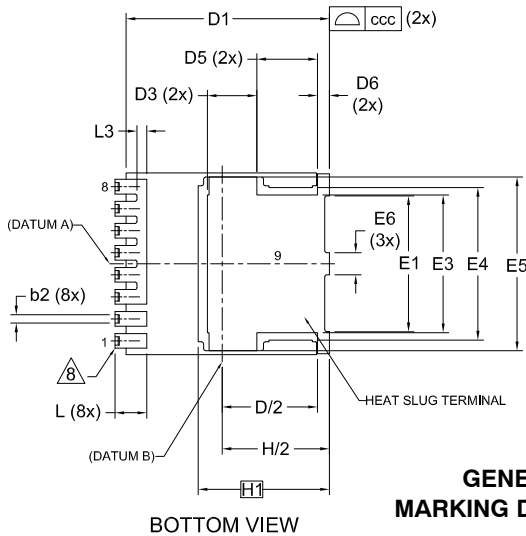
DATE 30 JUL 2024



LAND PATTERN RECOMMENDATION  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
  3. "e" REPRESENTS THE TERMINAL PITCH.
  4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
  5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
  6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
  7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
  8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
theta	10° REF		
theta 1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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