DATA SHEET
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Silicon Carbide (SiC) MOSFET – EliteSiC, 12 mohm, 650 V, M3S, TOLL

NTBL012N065M3S

Features

- Typical $R_{DS(ON)}$ = 12 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 143 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 268 pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

- SMPS, Solar Inverters, UPS, Energy Storage, EV Charging Infrastructure

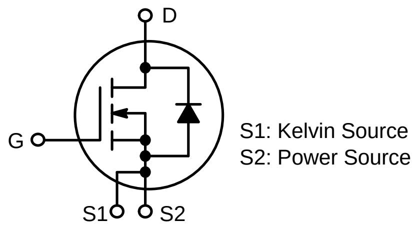
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	650	V
Gate-to-Source Voltage		V_{GS}	−10/+22.6	V
Continuous Drain Current	T_C = 25 °C	I_D	142	A
Power Dissipation		P_D	576	W
Continuous Drain Current	T_C = 100 °C	I_D	101	A
Power Dissipation		P_D	288	W
Pulsed Drain Current (Note 1)	T_C = 25 °C t_p = 100 µs	I_{DM}	302	A
Continuous Source-Drain Current (Body Diode)	T_C = 25 °C V_{GS} = −3 V	I_S	90	
	T_C = 100 °C V_{GS} = −3 V		51	
Pulsed Source-Drain Current (Body Diode) (Note 1)	T_C = 25 °C V_{GS} = −3 V t_p = 100 µs	I_{SM}	335	
Single Pulse Avalanche Energy (I_{LPK} = 63 A, L = 0.1 mH) (Note 2)		E_{AS}	199	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Lead Temperature for Soldering Purposes (1/8″ from Case for 10 Seconds)		T_L	260	°C

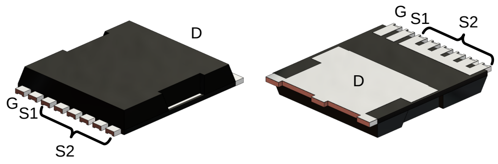
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Single pulse, limited by max junction temperature.
2. E_{AS} of 199 mJ is based on starting T_J = 25 °C, L = 0.1 mH, I_{AS} = 63 A, V_{DD} = 100 V, V_{GS} = 18 V.

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
650 V	12 mΩ @ 18 V	142 A

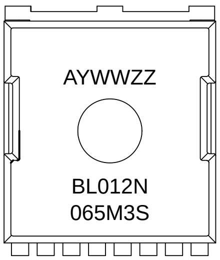


N-Channel MOSFET



H-PSOF8L
CASE 100DC

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
BL012N065M3S = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBL012N065M3S	H-PSOF8L	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 3)	$R_{\theta JC}$	0.26	°C/W

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted

RECOMMENDED OPERTATING CONDITIONS

Parameter	Symbol	Value	Unit
Operation Values of Gate-to-Source Voltage	V_{GSop}	−3/+18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	650	−	−	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C (Note 5)	−	86	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, T_J = 25 °C	−	−	10	μA
		V_{DS} = 650 V, T_J = 175 °C (Note 5)	−	−	500	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = −10, V_{DS} = 0 V	−1.0	−	−	μA
		V_{GS} = +22.6 V, V_{DS} = 0 V	−	−	+1.0	
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 40 A, T_J = 25 °C	−	12	16.8	mΩ
		V_{GS} = 18 V, I_D = 40 A, T_J = 175 °C (Note 5)	−	18	−	
		V_{GS} = 15 V, I_D = 40 A, T_J = 25 °C	−	15	−	
		V_{GS} = 15 V, I_D = 40 A, T_J = 175 °C (Note 5)	−	20	−	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 20 mA, T_J = 25 °C	2.0	2.7	4.0	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 40 A (Note 5)	−	38	−	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz (Note 5)	−	3217	−	pF
Output Capacitance	C_{OSS}		−	268	−	
Reverse Transfer Capacitance	C_{RSS}		−	22	−	
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 400 V, I_D = 40 A, V_{GS} = −3/18 V (Note 5)	−	143	−	nC
Gate-to-Source Charge	Q_{GS}		−	34	−	
Gate-to-Drain Charge	Q_{GD}		−	33	−	
Gate Resistance	R_G	f = 1 MHz	−	1.7	−	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, I_D = 40 A, V_{DD} = 400 V, R_G = 4.7 Ω, T_J = 25 °C, L_{stray} = 11 nH (Notes 4, 5)	−	17	−	ns
Turn-Off Delay Time	$t_{d(OFF)}$		−	50	−	
Rise Time	t_r		−	20	−	
Fall Time	t_f		−	12	−	
Turn-On Switching Loss	E_{ON}		−	203	−	μJ
Turn-Off Switching Loss	E_{OFF}		−	98	−	
Total Switching Loss	E_{TOT}		−	301	−	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, I_D = 40 A, V_{DD} = 400 V, R_G = 4.7 Ω, T_J = 175 °C, L_{stray} = 11 nH (Notes 4, 5)	–	13	–	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	60	–	
Rise Time	t_r		–	20	–	
Fall Time	t_f		–	13	–	
Turn-On Switching Loss	E_{ON}		–	220	–	μJ
Turn-Off Switching Loss	E_{OFF}		–	120	–	
Total Switching Loss	E_{TOT}		–	340	–	
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_{SD} = 40 A, V_{GS} = −3 V, T_J = 25 °C	–	4.5	6.0	V
		I_{SD} = 40 A, V_{GS} = −3 V, T_J = 175 °C (Note 5)	–	4.2	–	
Reverse Recovery Time	t_{RR}	V_{GS} = −3 V, I_S = 40 A, dI/dt = 1000 A/μs, V_{DS} = 400 V, T_J = 25 °C (Note 5)	–	23	–	ns
Charge Time	t_a		–	14	–	
Discharge Time	t_b		–	9.1	–	
Reverse Recovery Charge	Q_{RR}		–	157	–	nC
Reverse Recovery Energy	E_{REC}		–	9.8	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	12	–	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. E_{ON}/E_{OFF} result is with body diode.
5. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

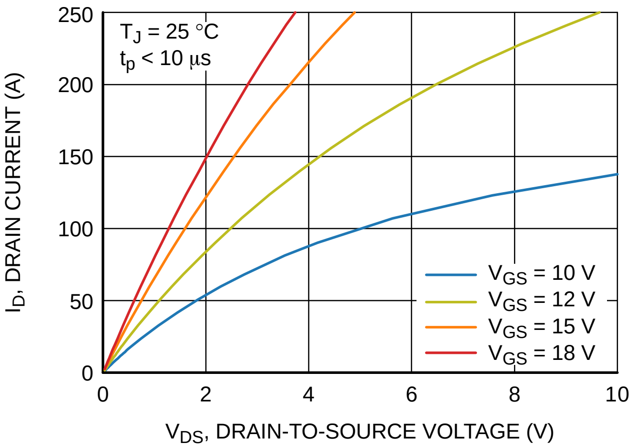


Figure 1. Output Characteristics

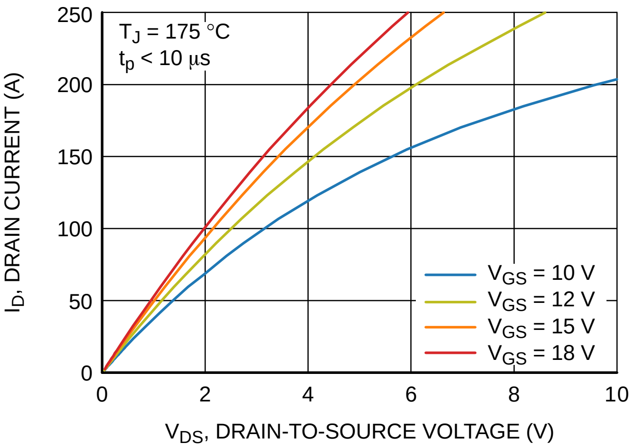


Figure 2. Output Characteristics

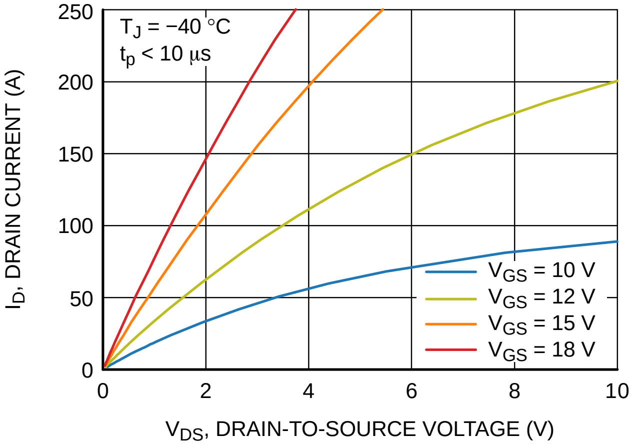


Figure 3. Output Characteristics

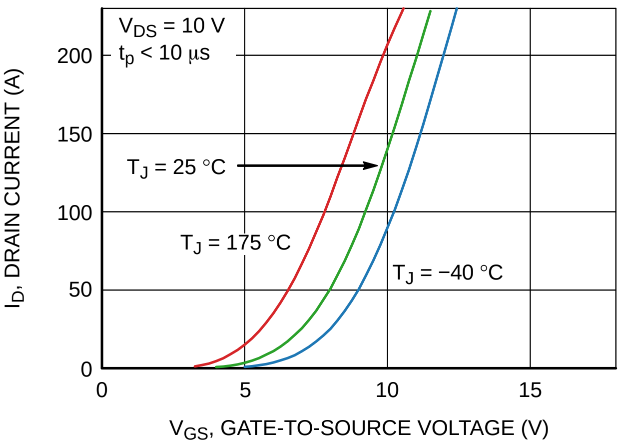


Figure 4. Transfer Characteristics

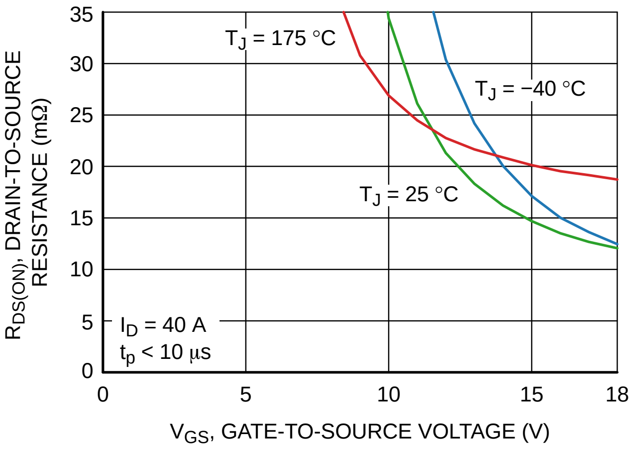


Figure 5. On-Resistance vs. Gate Voltage

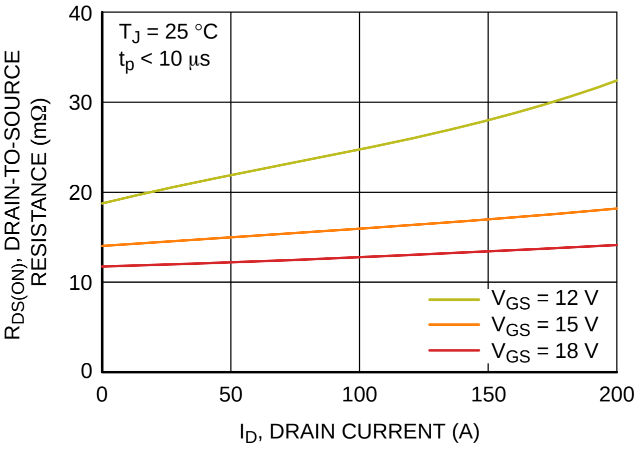


Figure 6. On-Resistance vs. Drain Current

TYPICAL CHARACTERISTICS

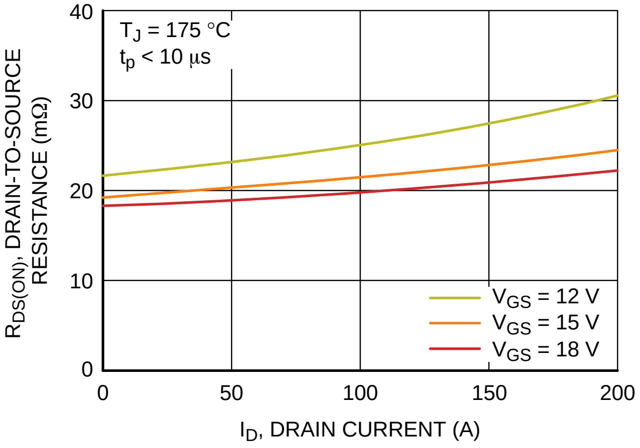


Figure 7. On-Resistance vs. Drain Current

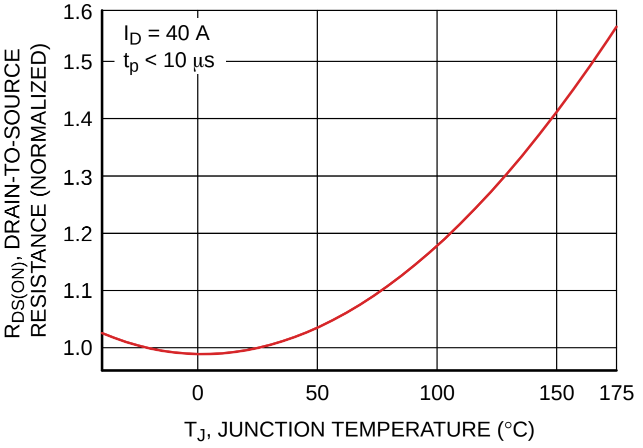


Figure 8. On-Resistance vs. Junction Temperature

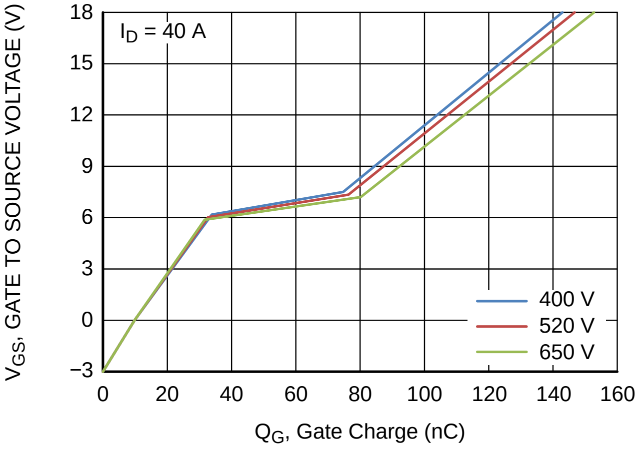


Figure 9. Gate Charge Characteristics

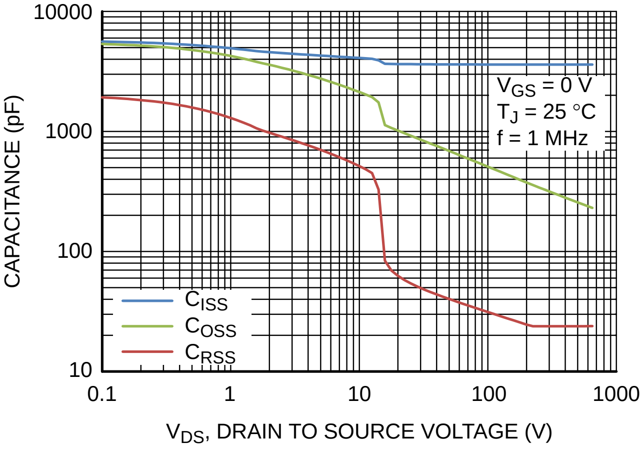


Figure 10. Capacitance Characteristics

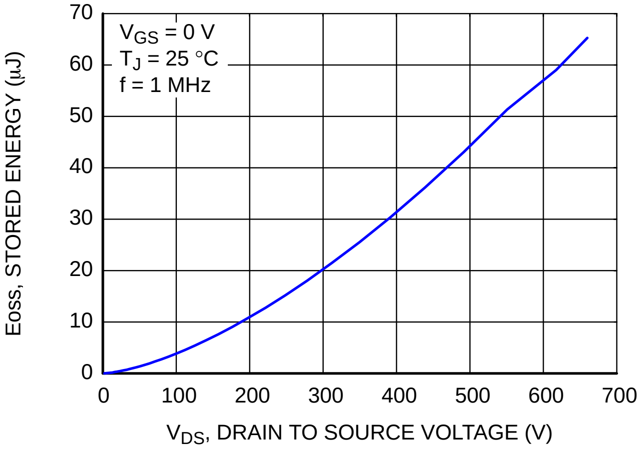


Figure 11. Stored Energy vs. Drain to Source Voltage

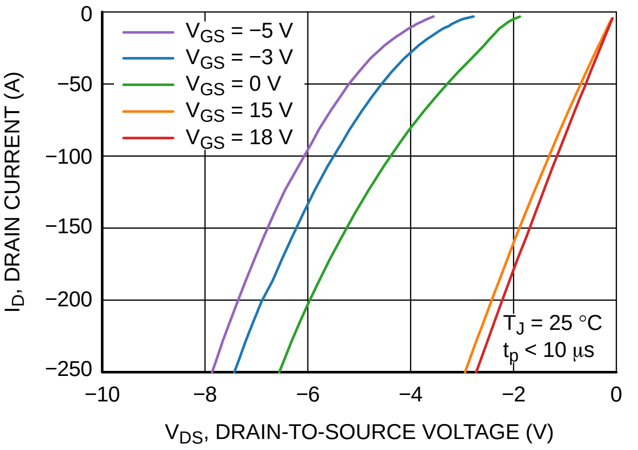


Figure 12. Reverse Conduction Characteristics

TYPICAL CHARACTERISTICS

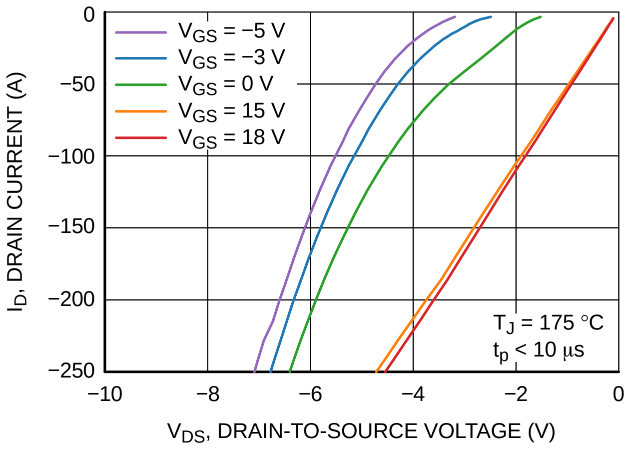


Figure 13. Reverse Conduction Characteristics

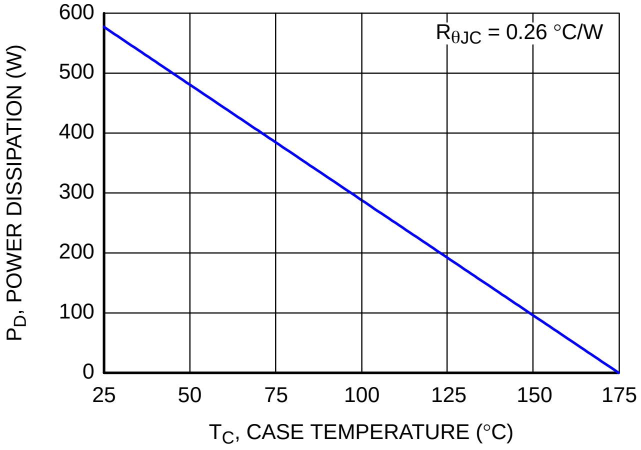


Figure 14. Maximum Power Dissipation vs. Case Temperature

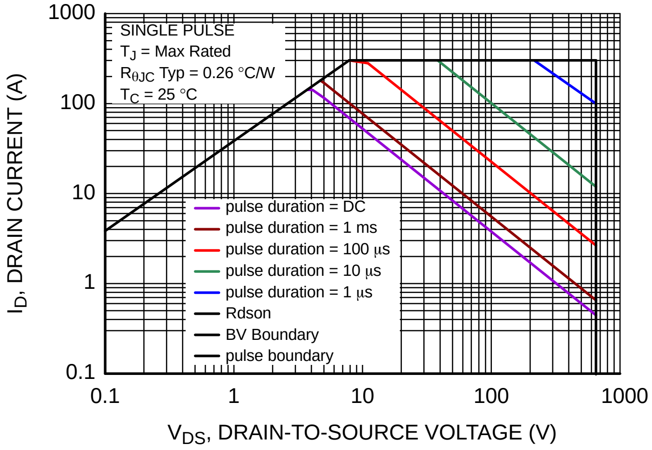


Figure 15. Safe Operating Area

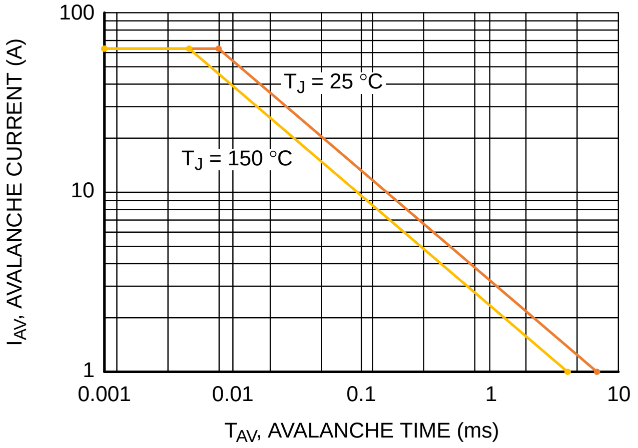


Figure 16. Avalanche Current vs. Pulse Time (UIS)

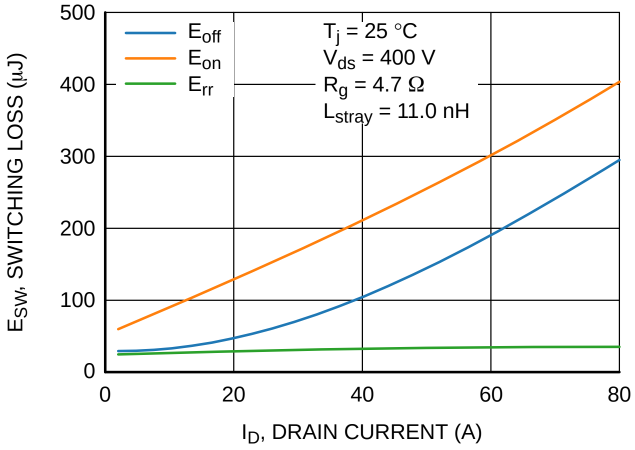


Figure 17. Inductive Switching Loss vs. Drain Current

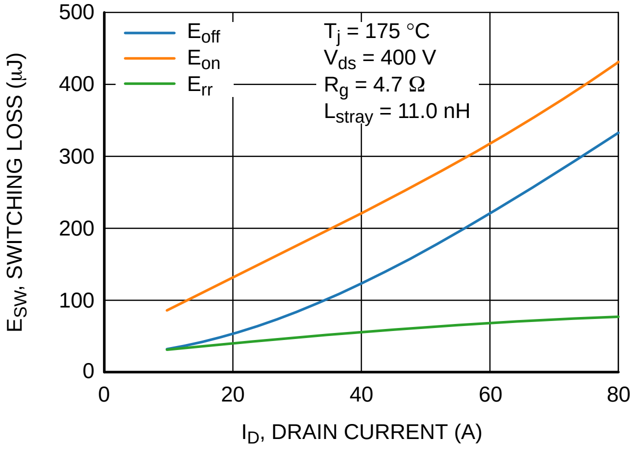


Figure 18. Inductive Switching Loss vs. Drain Current

TYPICAL CHARACTERISTICS

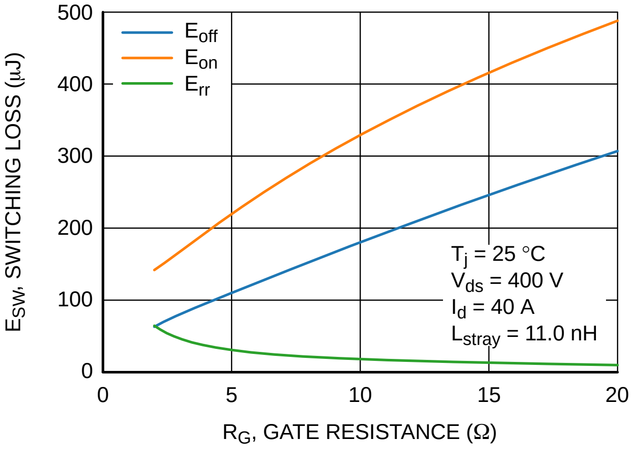


Figure 19. Inductive Switching Loss vs. Gate Resistance

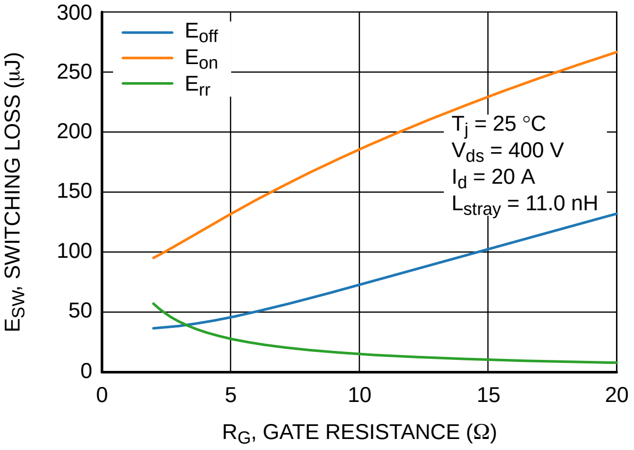


Figure 20. Inductive Switching Loss vs. Gate Resistance

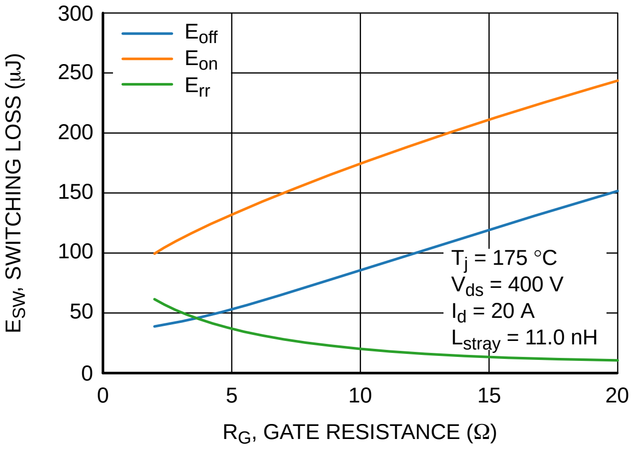


Figure 21. Inductive Switching Loss vs. Gate Resistance

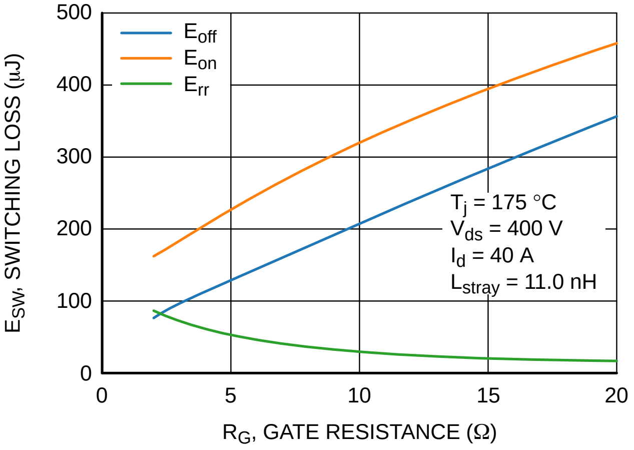


Figure 22. Inductive Switching Loss vs. Gate Resistance

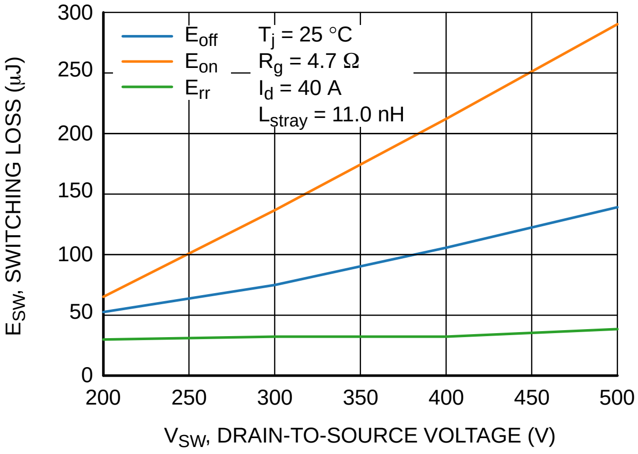


Figure 23. Inductive Switching Loss vs. Drain Voltage

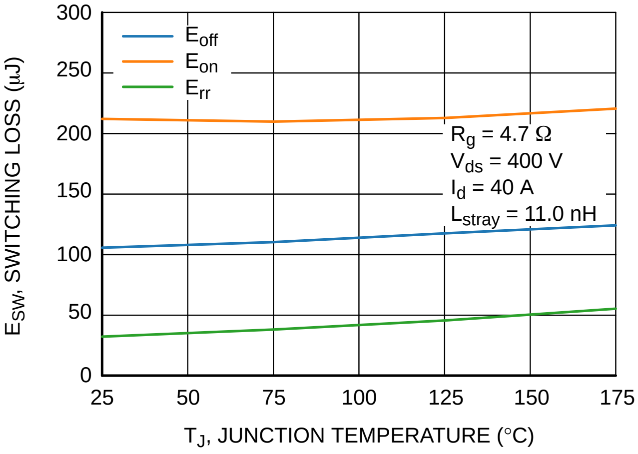


Figure 24. Inductive Switching Loss vs. Junction Temperature

TYPICAL CHARACTERISTICS

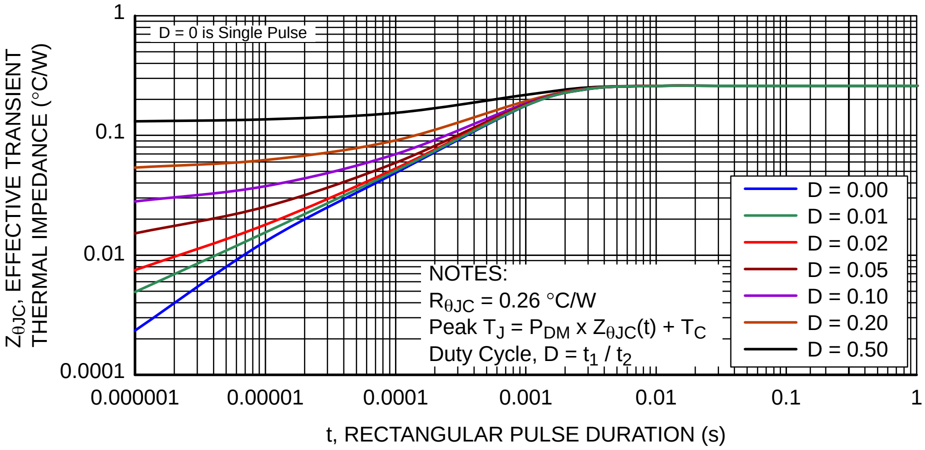
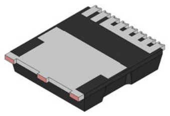


Figure 25. Transient Thermal Response

REVISION HISTORY

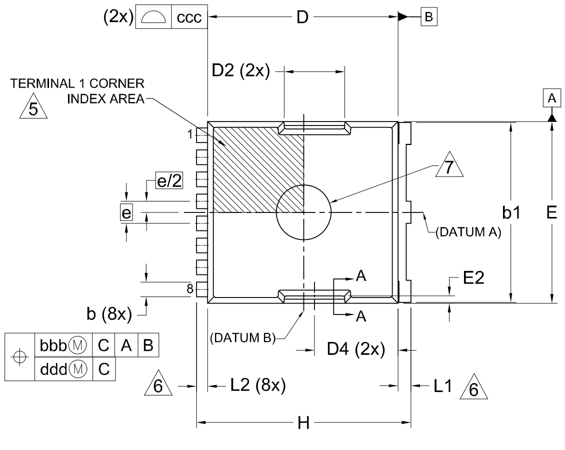
Revision	Description of Changes	Date
0	Initial document release.	1/21/2026

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

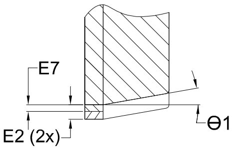


H−PSOF8L 9.90x10.38x2.30, 1.20P
CASE 100DC
ISSUE D

DATE 30 JUL 2024



TOP VIEW



SECTION "A-A"
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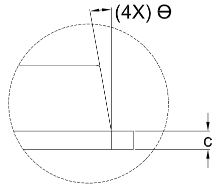

DETAIL "B"
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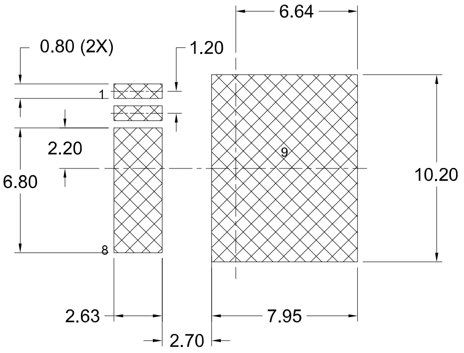
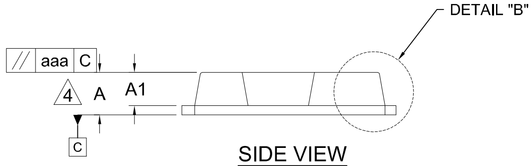
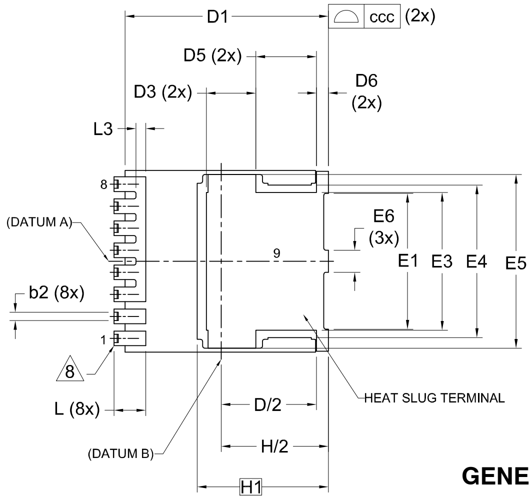


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



SIDE VIEW

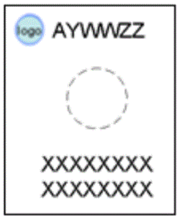


BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**H−PSOF8L 9.90x10.38x2.30, 1.20P**	**PAGE 1 OF 1**

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