

Silicon Carbide (SiC) MOSFET – EliteSiC, 14 mohm, 1200 V, M3P, D2PAK-7L

NTBG014N120M3P

Features

- Typ. $R_{DS(on)}$ = 14 m Ω
- Low Switching Losses (Typ. E_{ON} 1331 μ J at 74 A, 800 V)
- 100% Avalanche Tested

Typical Applications

- Solar Inverters
- Electric Vehicle Charging Stations
- UPS (Uninterruptible Power Supplies)
- Energy Storage Systems
- SMPS (Switch Mode Power Supplies)

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

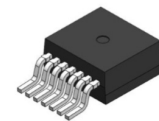
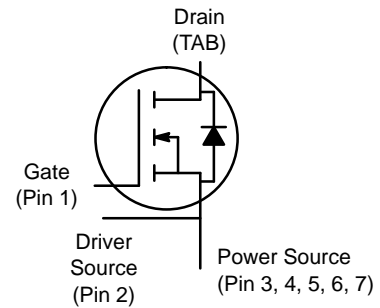
Symbol	Parameter		Value	Unit	
V_{DSS}	Drain-to-Source Voltage		1200	V	
V_{GS}	Gate-to-Source Voltage		-10 +22	V	
V_{GSop}	Recommended Operation Values of Gate-Source Voltage	$T_C < 175^\circ\text{C}$	-3/+18	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	104	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 2)			454	W
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 1, 2)	Steady State	$T_C = 100^\circ\text{C}$	73	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1, 2)			227	W
I_{DM}	Pulsed Drain Current (Note 3)	$T_A = 25^\circ\text{C}$	257	A	
T_J, T_{STG}	Operating Junction and Storage Temperature		-55 to 175	$^\circ\text{C}$	
I_S	Source Current (Body Diode) $T_C = 25^\circ\text{C}, V_{GS} = -3\text{ V}$		92	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy (Note 5) ($I_L = 28.9\text{ A}_{pk}, L = 1\text{ mH}$) (Note 4)		418	mJ	
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 seconds		245	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in² pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. Peak current might be limited by transconductance.
5. E_{AS} of 418 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1\text{ mH}$, $I_{AS} = 28.9\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 18\text{ V}$.

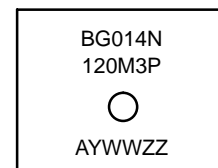
$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1200 V	20 m Ω @ 18 V	104 A

N-CHANNEL MOSFET



D2PAK-7L
CASE 418BJ

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Lot Traceability
- BG014N120M3P = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBG014N120M3P	D2PAK-7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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THERMAL CHARACTERISTICS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction-to-Case (Note 2)	0.33	–	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (Note 1, 2)	–	40	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF-STATE CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200			V
$V_{(BR)DSS} / T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, refer to 25°C		0.3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}, T_J = 25^\circ\text{C}$			100	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = +22/-10\text{ V}, V_{DS} = 0\text{ V}$			± 1	μA

ON-STATE CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 37\text{ mA}$	2.08	3.0	4.63	V
V_{GOP}	Recommended Gate Voltage		–3		+18	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 18\text{ V}, I_D = 74\text{ A}, T_J = 25^\circ\text{C}$		14	20	m Ω
		$V_{GS} = 18\text{ V}, I_D = 74\text{ A}, T_J = 175^\circ\text{C}$		29		m Ω
		$V_{GS} = 15\text{ V}, I_D = 74\text{ A}, T_J = 25^\circ\text{C}$		16	27	m Ω
		$V_{GS} = 15\text{ V}, I_D = 74\text{ A}, T_J = 150^\circ\text{C}$		27		m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 74\text{ A}$		29		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 800\text{ V}$		6313		pF
C_{OSS}	Output Capacitance			259		
C_{RSS}	Reverse Transfer Capacitance			27		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = -3/18\text{ V}, V_{DS} = 800\text{ V}, I_D = 74\text{ A}$		337		nC
$Q_{G(TH)}$	Threshold Gate Charge			43		
Q_{GS}	Gate-to-Source Charge			78		
Q_{GD}	Gate-to-Drain Charge			98		
R_G	Gate Resistance	$f = 1\text{ MHz}$		1.4		Ω

SWITCHING CHARACTERISTICS

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = -3/18\text{ V}, V_{DS} = 800\text{ V}, I_D = 74\text{ A}, R_G = 2\text{ }\Omega$ Inductive Load (Note 6)		24		ns
t_r	Rise Time			40		
$t_{d(OFF)}$	Turn-Off Delay Time			74		
t_f	Fall Time			14		
E_{ON}	Turn-On Switching Loss			1331		μJ
E_{OFF}	Turn-Off Switching Loss			620		
E_{TOT}	Total Switching Loss			1951		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_{SD}	Continuous Drain-Source Diode Forward Current	$V_{GS} = -3\text{ V}, T_C = 25^\circ\text{C}$			92	A
I_{SDM}	Pulsed Drain-Source Diode Forward Current (Note 3)	$V_{GS} = -3\text{ V}, T_C = 25^\circ\text{C}$			257	A
V_{SD}	Forward Diode Voltage	$V_{GS} = -3\text{ V}, I_{SD} = 74\text{ A}, T_J = 25^\circ\text{C}$		5.1		V
t_{RR}	Reverse Recovery Time	$V_{GS} = -3/18\text{ V}, I_{SD} = 74\text{ A},$ $di_S/dt = 1000\text{ A}/\mu\text{s}, V,$ $V_{DS} = 800\text{ V}$		37		ns
Q_{RR}	Reverse Recovery Charge			347		nC
E_{REC}	Reverse Recovery Energy			12		μJ
I_{RRM}	Peak Reverse Recovery Current			19		A
t_A	Charge Time			19		ns
t_B	Discharge Time			17		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. E_{ON}/E_{OFF} result is with body diode.

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TYPICAL CHARACTERISTICS

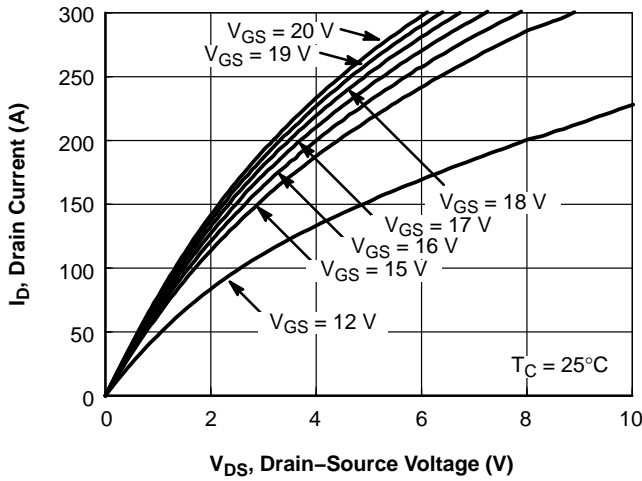


Figure 1. On-Region Characteristics

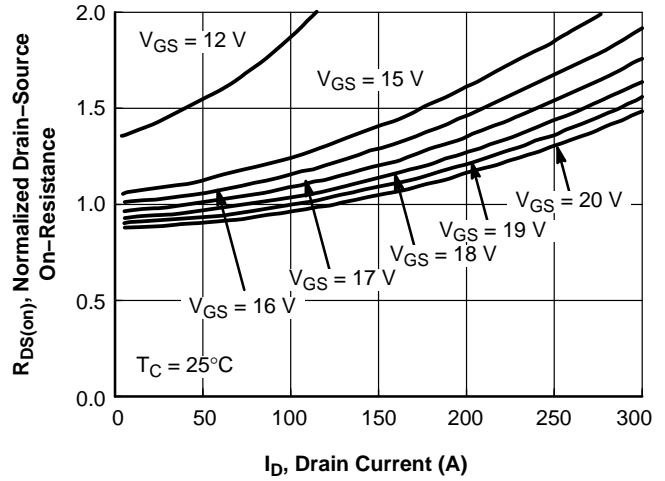


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

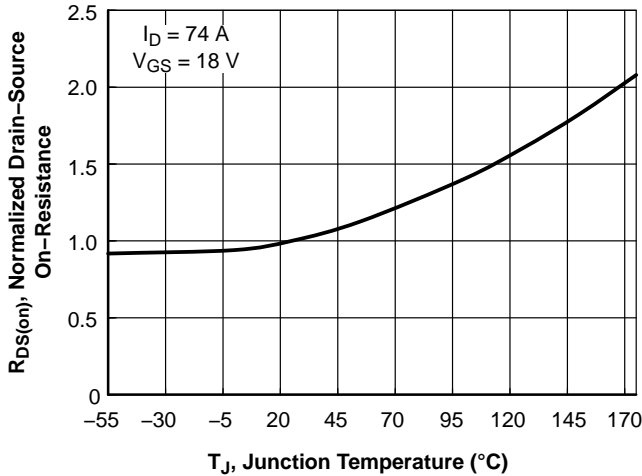


Figure 3. On-Resistance Variation with Temperature

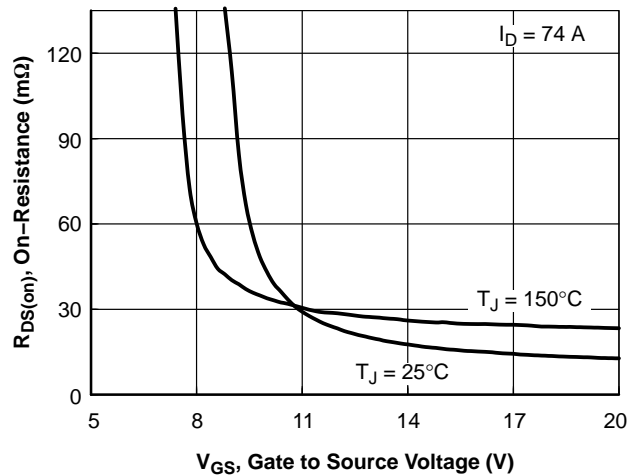


Figure 4. On-Resistance vs. Gate-to-Source Voltage

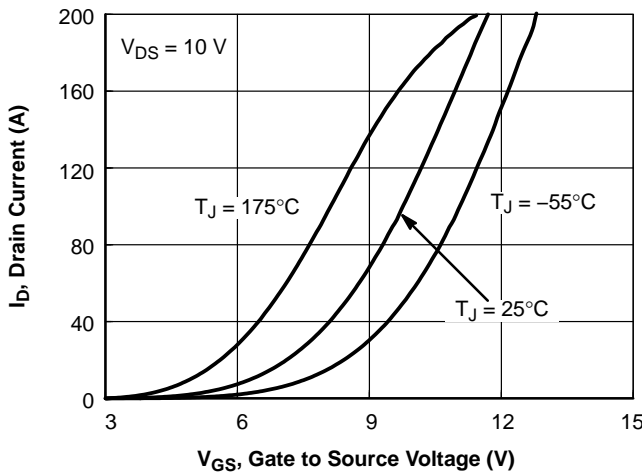


Figure 5. Transfer Characteristics

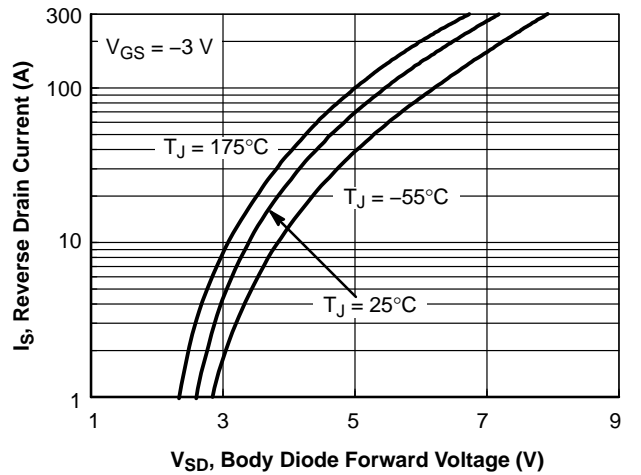


Figure 6. Diode Forward Voltage vs. Current

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TYPICAL CHARACTERISTICS (CONTINUED)

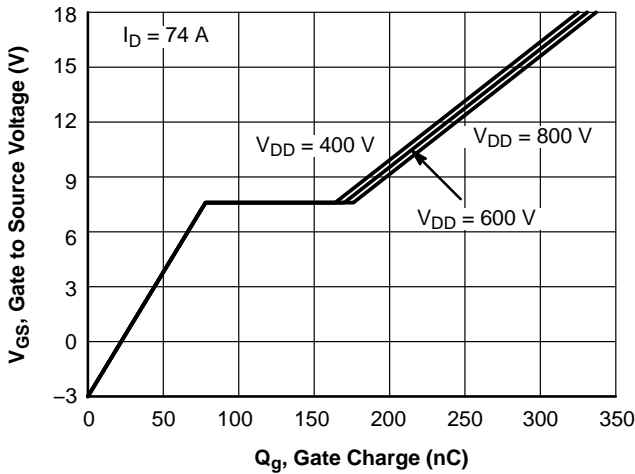


Figure 7. Gate-to-Source Voltage vs. Total Charge

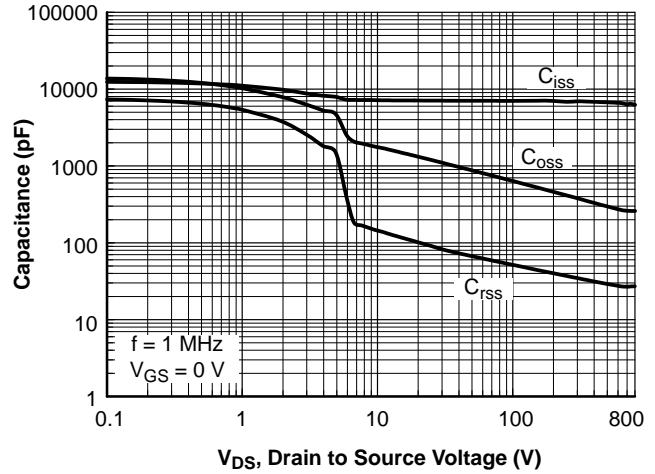


Figure 8. Capacitance vs. Drain to Source Voltage

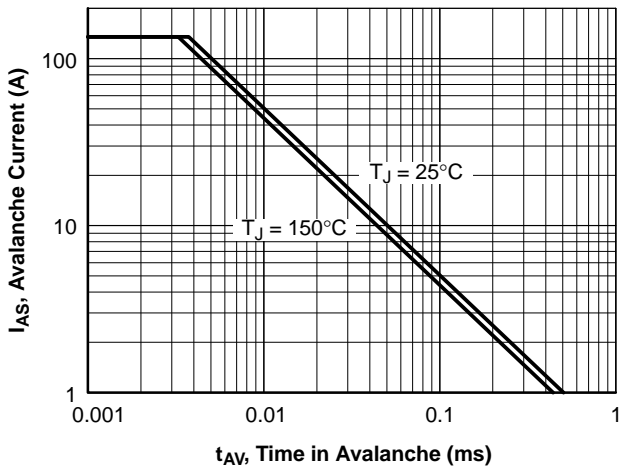


Figure 9. Unclamped Inductive Switching Capability

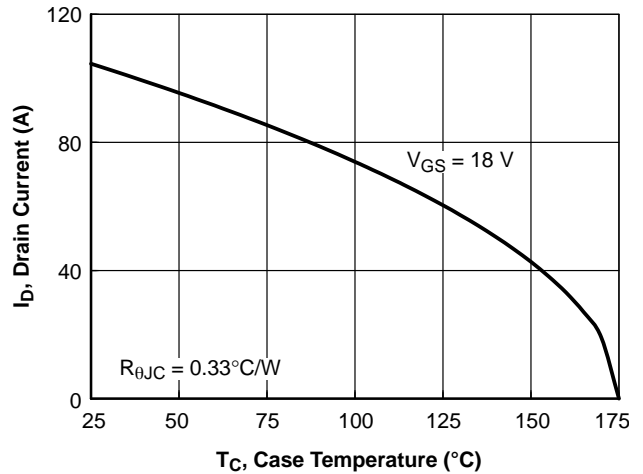


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

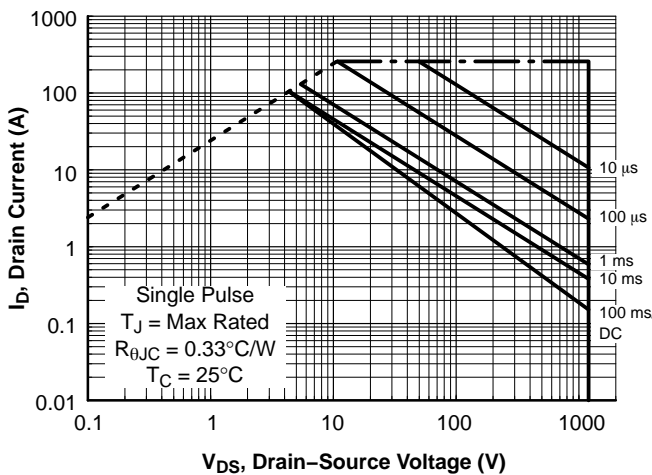


Figure 11. Safe Operating Area

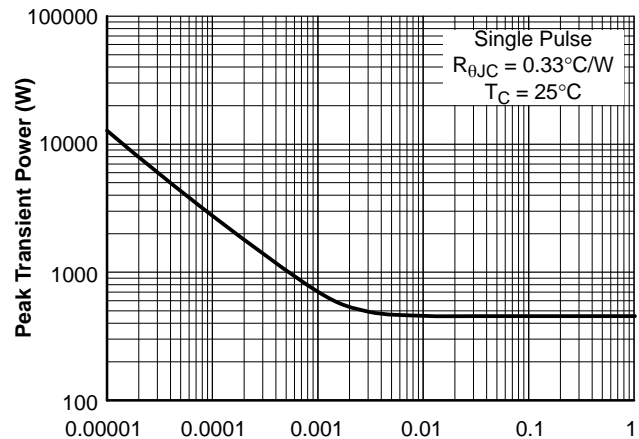


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (CONTINUED)

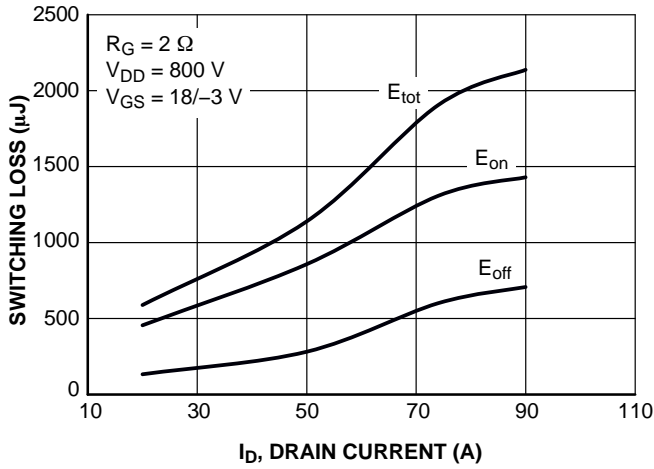


Figure 13. Switching Loss vs. Drain Current

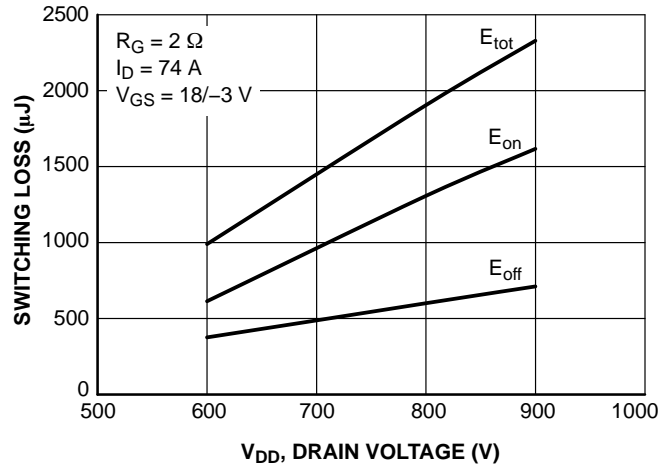


Figure 14. Switching Loss vs. Drain Voltage

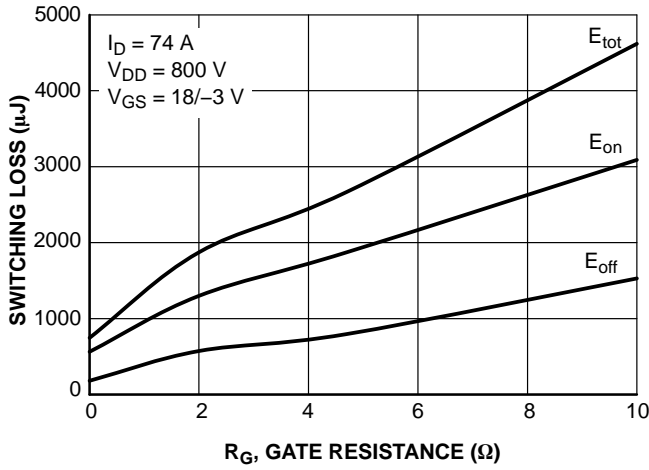


Figure 15. Switching Loss vs. Gate Resistance

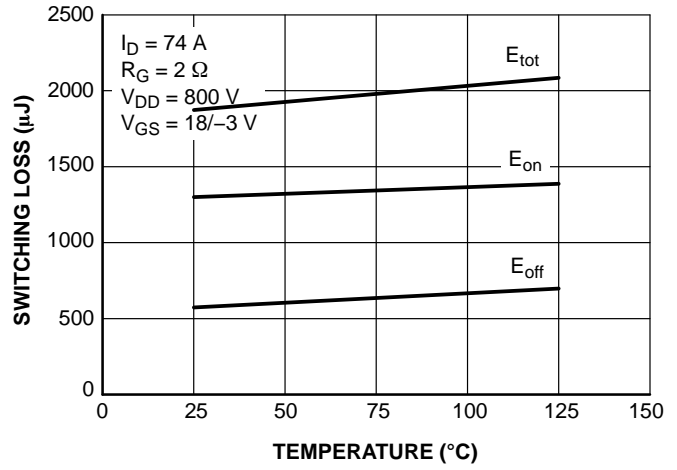


Figure 16. Switching Loss vs. Temperature

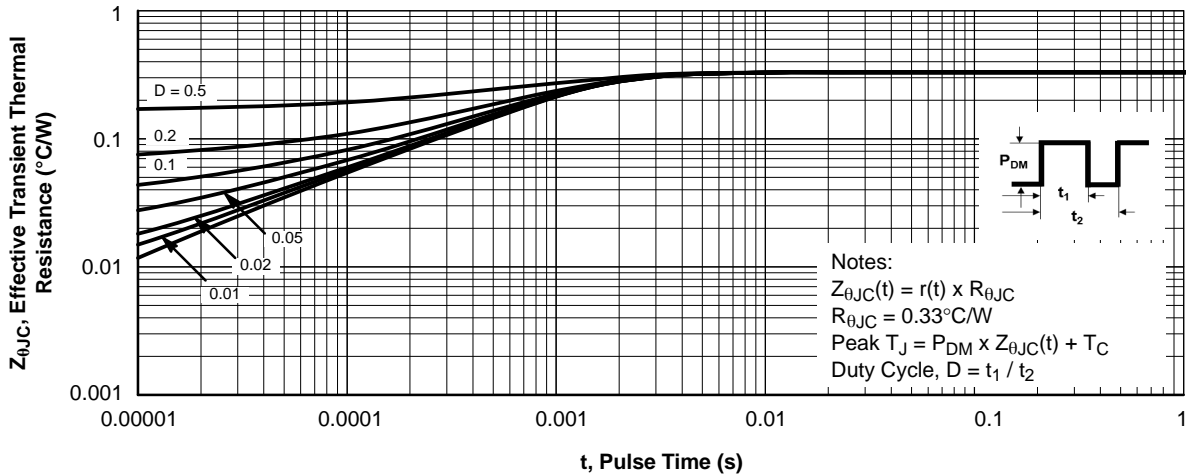


Figure 17. Junction-To-Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

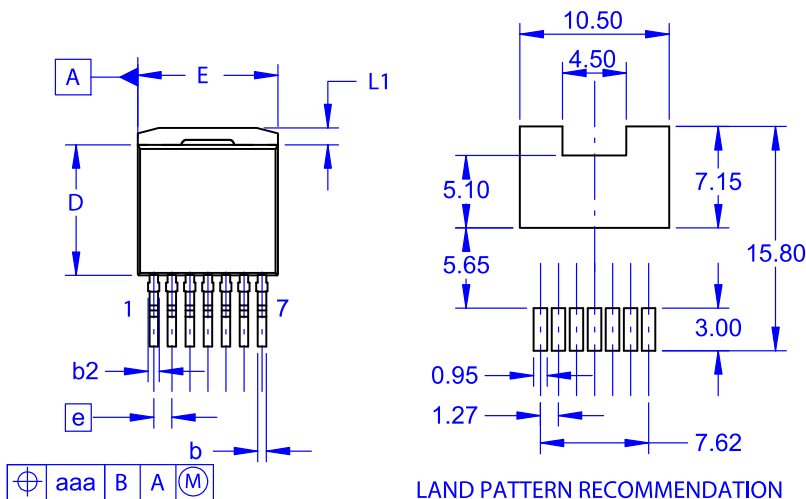
PACKAGE DIMENSIONS

ON Semiconductor®



D²PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

DATE 16 AUG 2019



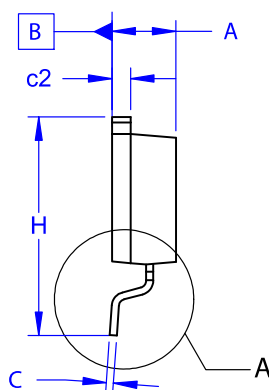
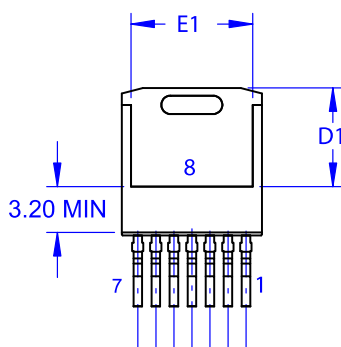
NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

\triangle OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

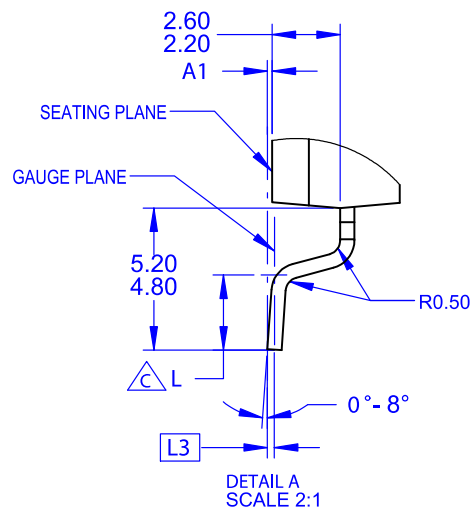


GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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