MOSFET – N-Channel, SUPERFET III, FRFET

650 V, 36 A, 95 mΩ

NTB095N65S3HF

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	95 mΩ @ 10 V	36 A

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

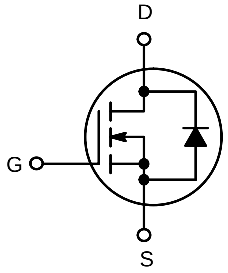
SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

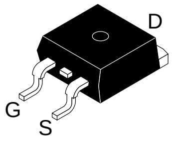
Features

- 700 V @ $T_J = 150$ °C
- Typ. $R_{DS(on)} = 80$ mΩ
- Ultra Low Gate Charge (Typ. $Q_g = 66$ nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 569$ pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

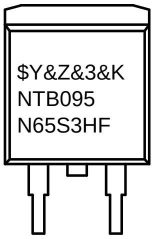
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar





D²PAK
CASE 418AJ

MARKING DIAGRAM



$Y = **onsemi** Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot
NTB095N65S3HF = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	− DC	±30	V
		− AC (f > 1 Hz)	±30	
I_D	Drain Current	− Continuous (T_C = 25 °C)	36	A
		− Continuous (T_C = 100 °C)	22.8	
I_{DM}	Drain Current	− Pulsed (Note 1)	90	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		440	mJ
I_{AS}	Avalanche Current (Note 2)		4.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.72	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25 °C)	272	W
		− Derate Above 25 °C	2.176	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 4.6 A, R_G = 25 Ω, starting T_J = 25 °C.
3. $I_{SD} \le 18$ A, di/dt ≤ 200 A/μs, $V_{DD} \le 400$ V, starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.46	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. Device on 1 in^2 2-oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
NTB095N65S3HF	NTB095N65S3HF	D^2PAK	330 mm	24 mm	800 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150 °C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 15 mA, Referenced to 25 °C		0.63		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125 °C		97		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.86 mA	3.0		5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 18 A		80	95	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 18 A		17		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		2930		pF
C_{oss}	Output Capacitance			61		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		569		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		110		pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 18 A, V_{GS} = 10 V (Note 5)		66		nC
Q_{gs}	Gate to Source Gate Charge			21		nC
Q_{gd}	Gate to Drain “Miller” Charge			25		nC
ESR	Equivalent Series Resistance	f = 1 MHz		2.4		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 18 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 5)		28		ns
t_r	Turn-On Rise Time			28		ns
$t_{d(off)}$	Turn-Off Delay Time			72		ns
t_f	Turn-Off Fall Time			24		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				36	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				90	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 18 A			1.3	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 18 A, dI_F/dt = 100 A/μs		106		ns
Q_{rr}	Reverse Recovery Charge			414		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

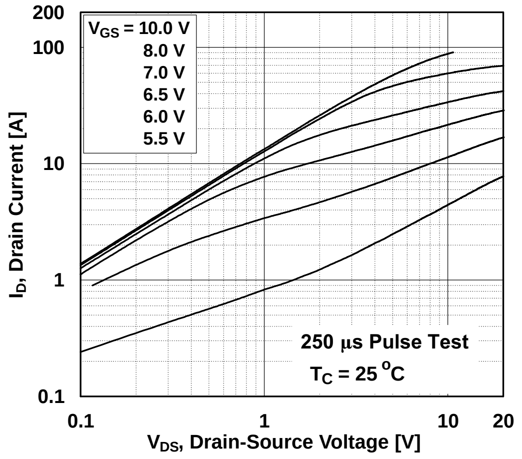


Figure 1. On-Region Characteristics

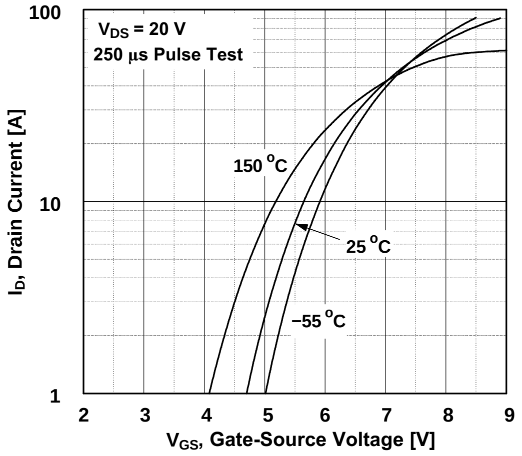


Figure 2. Transfer Characteristics

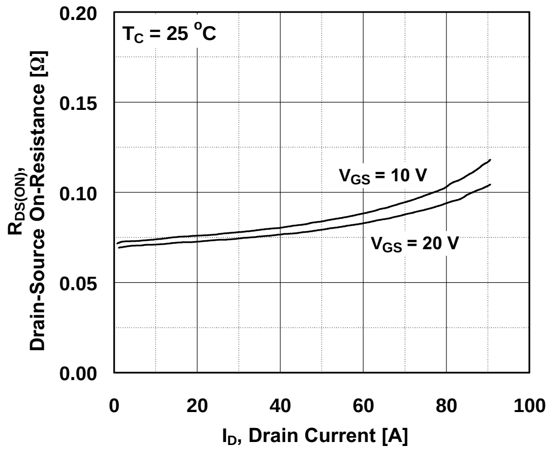


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

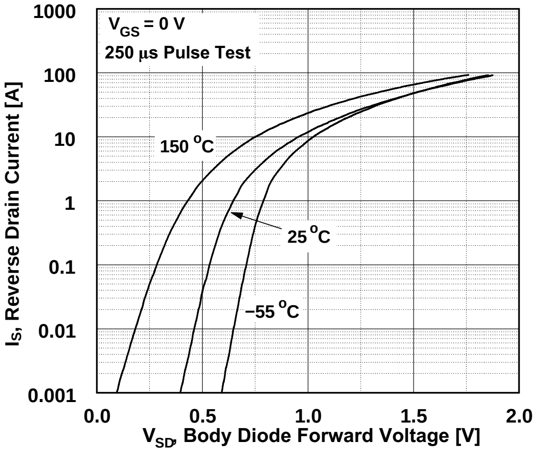


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

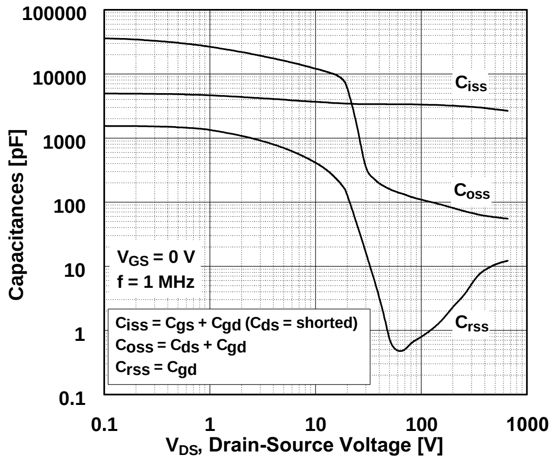


Figure 5. Capacitance Characteristics

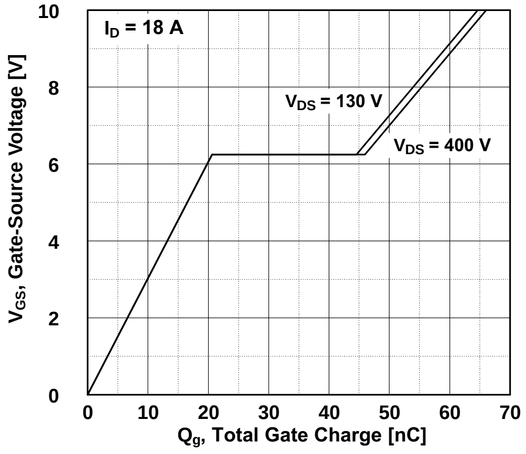


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

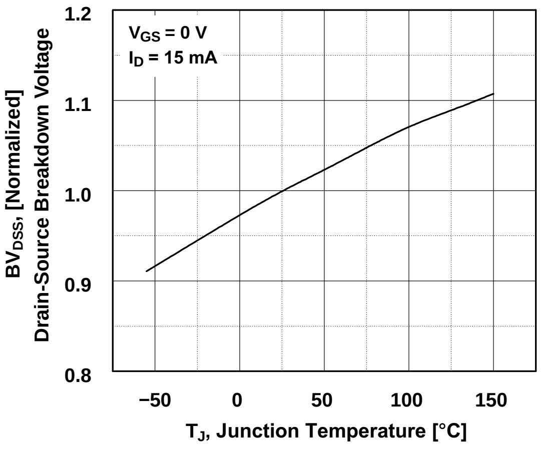


Figure 7. Breakdown Voltage Variation vs. Temperature

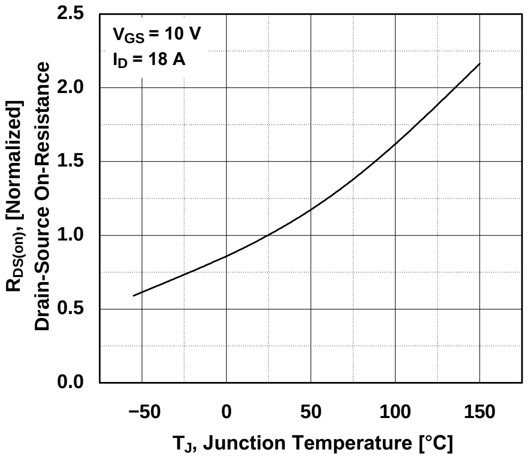


Figure 8. On-Resistance Variation vs. Temperature

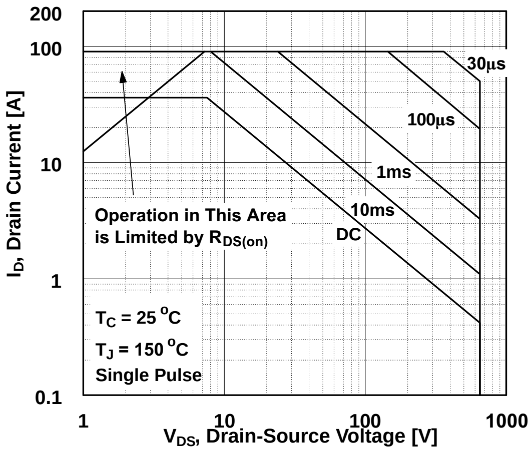


Figure 9. Maximum Safe Operating Area

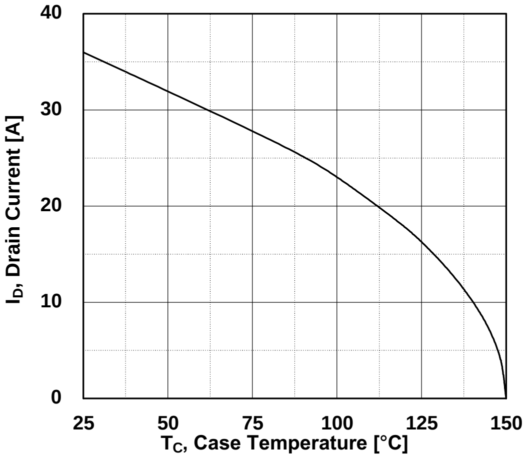


Figure 10. Maximum Drain Current vs. Case Temperature

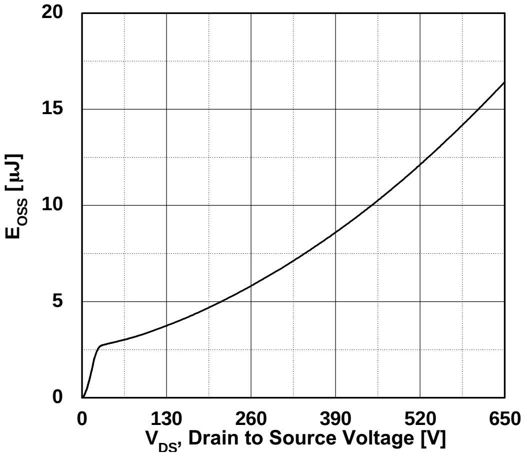


Figure 11. Eoss vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS

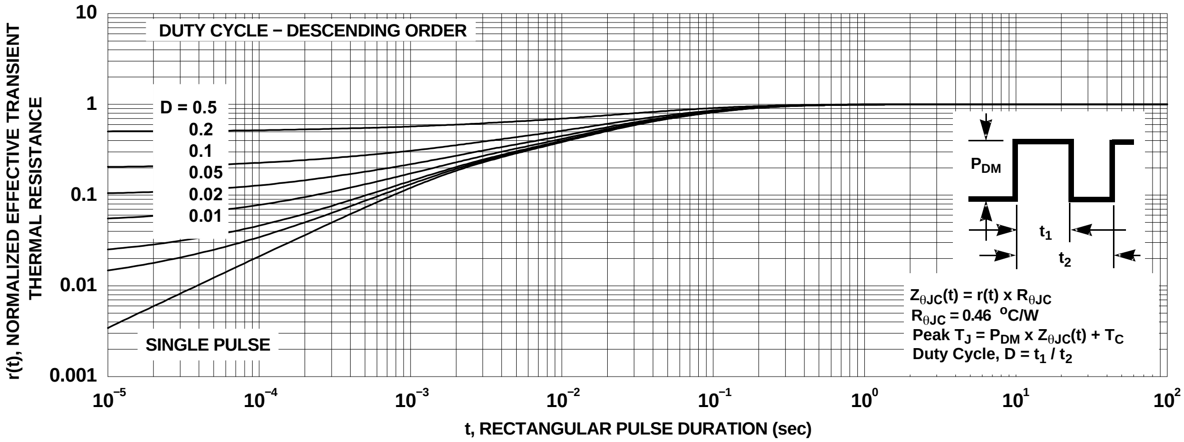


Figure 12. Transient Thermal Response Curve

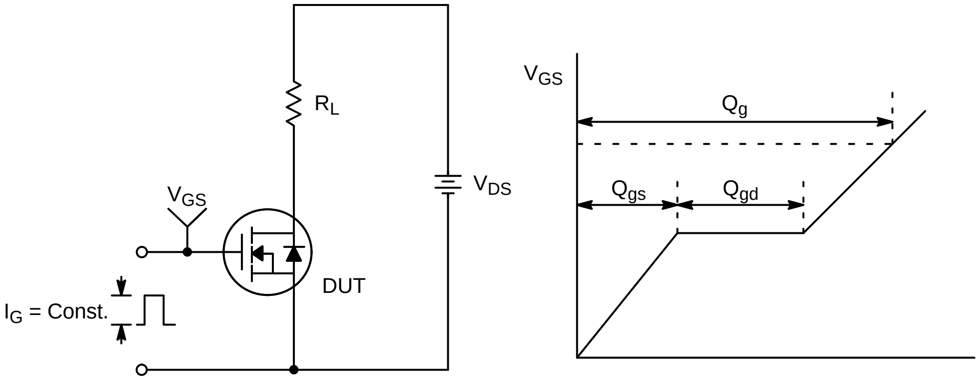


Figure 13. Gate Charge Test Circuit & Waveform

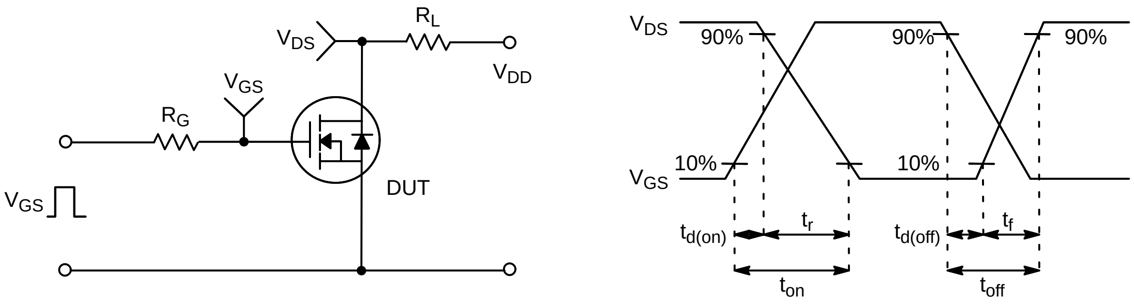


Figure 14. Resistive Switching Test Circuit & Waveforms

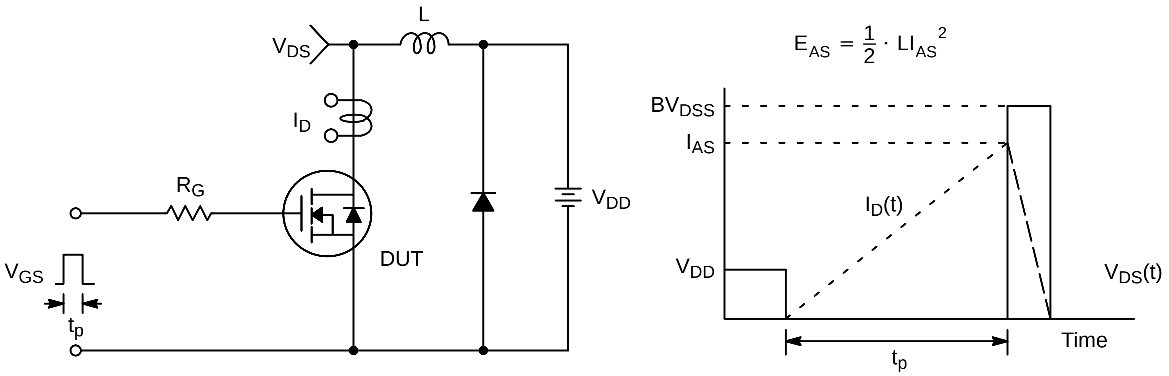


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

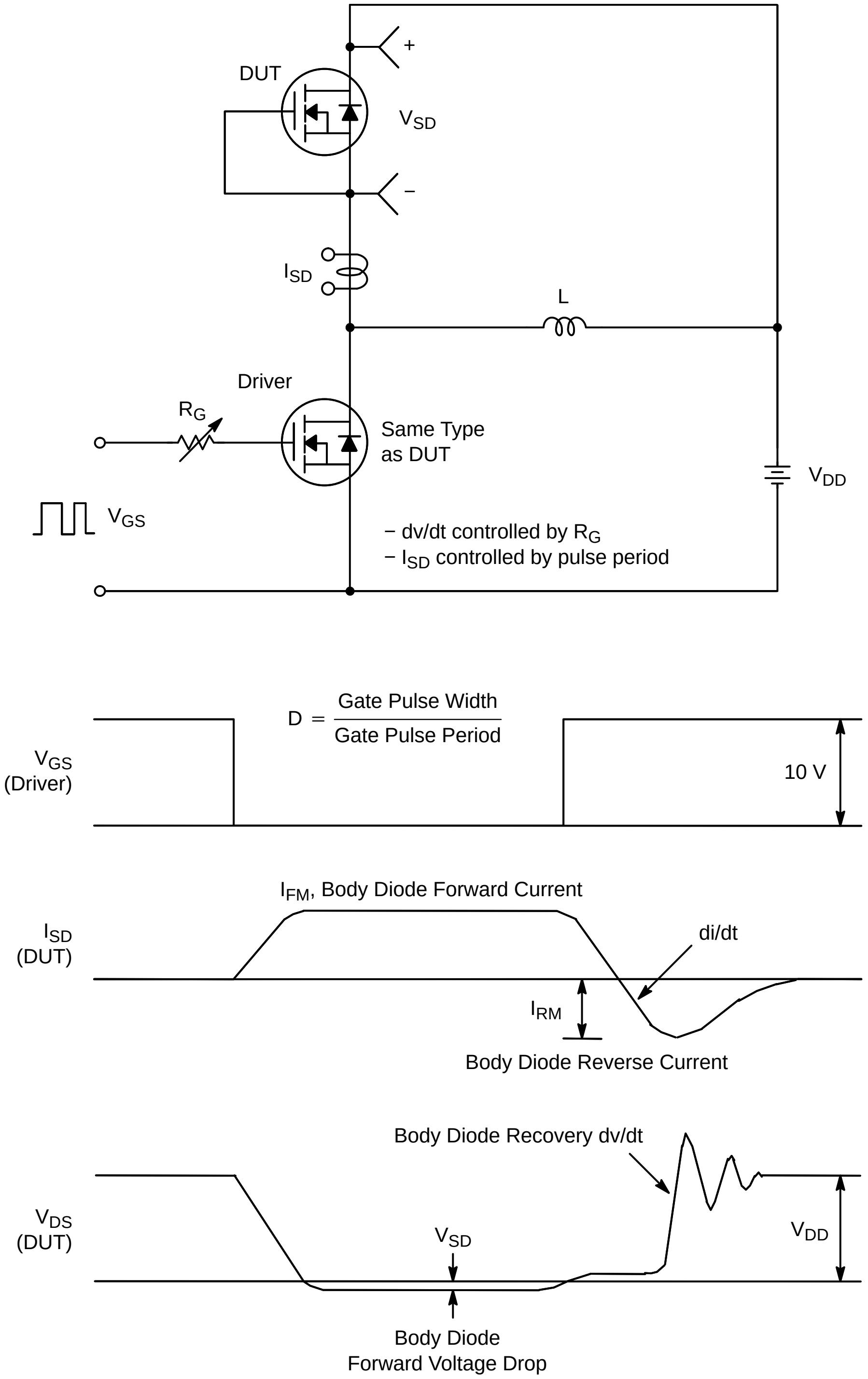


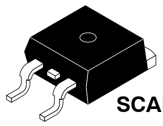
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

REVISION HISTORY

Revision	Description of Changes	Date
1	Rebranded the Data Sheet to **onsemi** format.	6/26/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

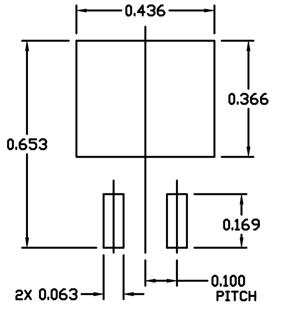
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

D^2PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



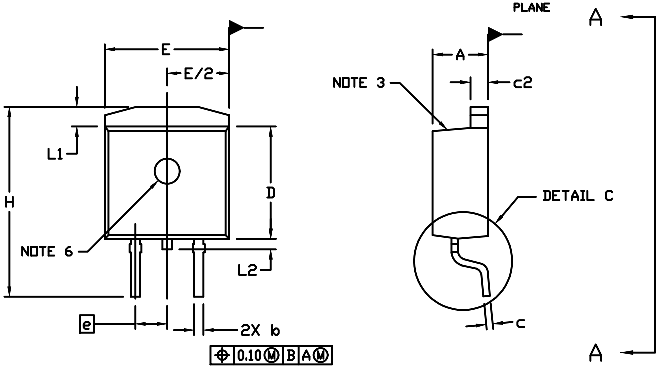
RECOMMENDED
MOUNTING FOOTPRINT

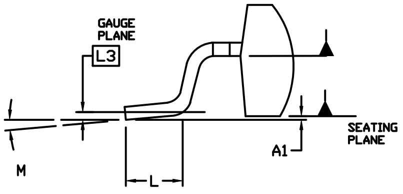
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

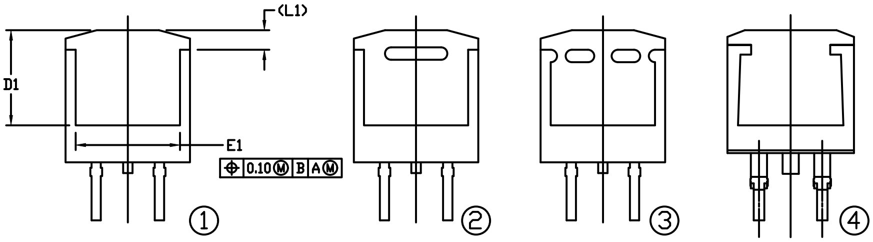
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°





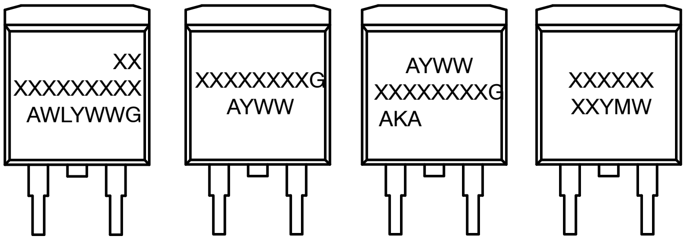
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A−A

VIEW A−A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC Standard Rectifier SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D^2PAK−3 (TO−263, 3−LEAD)**	**PAGE 1 OF 1**

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