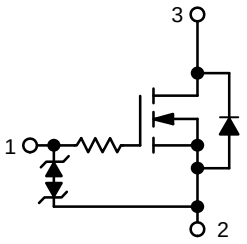
MOSFET – Single, N-Channel, Gate ESD Protection, Small Signal, SC-75

20 V, 238 mA

NTA4001N, NVA4001N

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ @ V_{GS}	I_D MAX (Note 1)
20 V	1.5 Ω @ 4.5 V	238 mA
	2.2 Ω @ 2.5 V	



N−Channel

Features

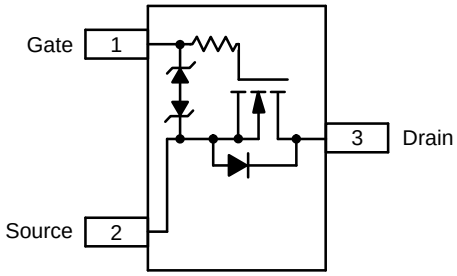
- Low Gate Charge for Fast Switching
- Small 1.6 x 1.6 mm Footprint
- ESD Protected Gate
- AEC-Q101 Qualified and PPAP Capable − NVA4001N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Management Load Switch
- Level Shift
- Portable Applications such as Cell Phones, Media Players, Digital Cameras, PDA's, Video Games, Hand Held Computers, etc.

PIN CONNECTIONS

SC-75 (3-Leads)



(Top View)

MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	20	V
Gate-to-Source Voltage		V_{GS}	±10	V
Continuous Drain Current (Note 1)	Steady State = 25 °C	I_D	238	mA
Power Dissipation (Note 1)	Steady State = 25 °C	P_D	300	mW
Pulsed Drain Current	$t_P \le 10$ μs	I_{DM}	714	mA
Operating Junction and Storage Temperature		T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)		I_{SD}	238	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

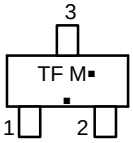
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	416	°C/W

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).

SC-75 / SOT-416
CASE 463
STYLE 5

MARKING DIAGRAM



TF = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V			1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V			±100	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = 3 V, I_D = 100 μA	0.5	1.0	1.5	V
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 10 mA		1.5	3.0	Ω
		V_{GS} = 2.5 V, I_D = 10 mA		2.2	3.5	
Forward Transconductance	g_{FS}	V_{DS} = 3 V, I_D = 10 mA		80		mS
CAPACITANCES						
Input Capacitance	C_{ISS}	V_{DS} = 5 V, f = 1 MHz, V_{GS} = 0 V		11.5	20	pF
Output Capacitance	C_{OSS}			10	15	
Reverse Transfer Capacitance	C_{RSS}			3.5	6.0	
SWITCHING CHARACTERISTICS (Note 3)						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 5 V, I_D = 10 mA, R_G = 10 Ω		13		ns
Rise Time	t_r			15		ns
Turn-Off Delay Time	$t_{d(OFF)}$			98		
Fall Time	t_f			60		
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 mA		0.66	0.8	V

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

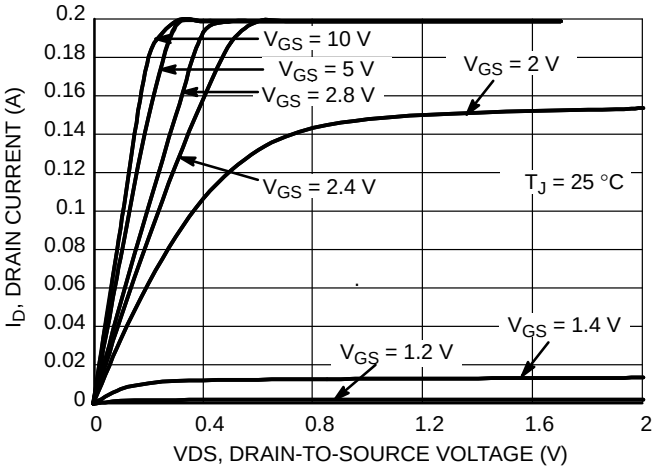


Figure 1. On-region Characteristics

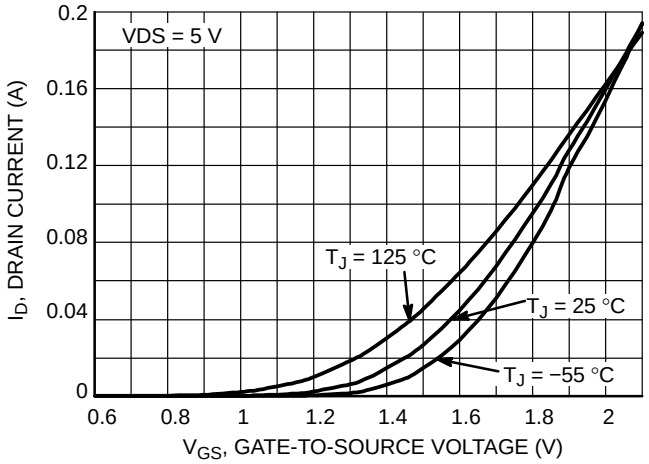


Figure 2. Transfer Characteristics

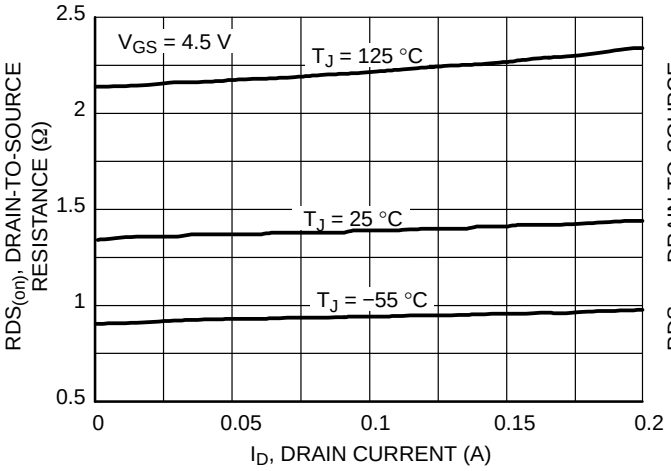


Figure 3. On-resistance versus Drain Current and Temperature

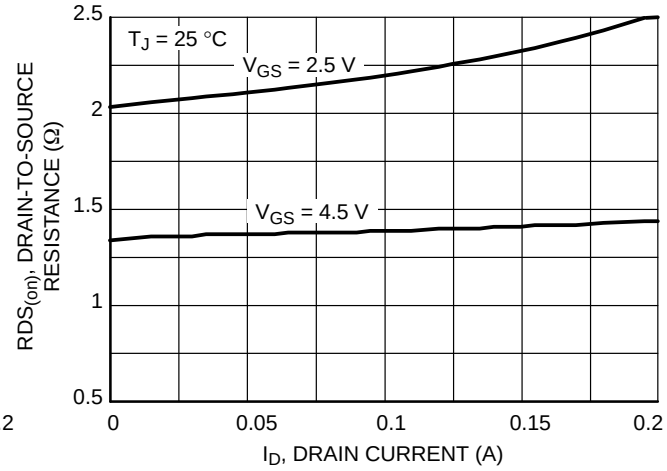


Figure 4. On-resistance versus Drain Current and Gate Voltage

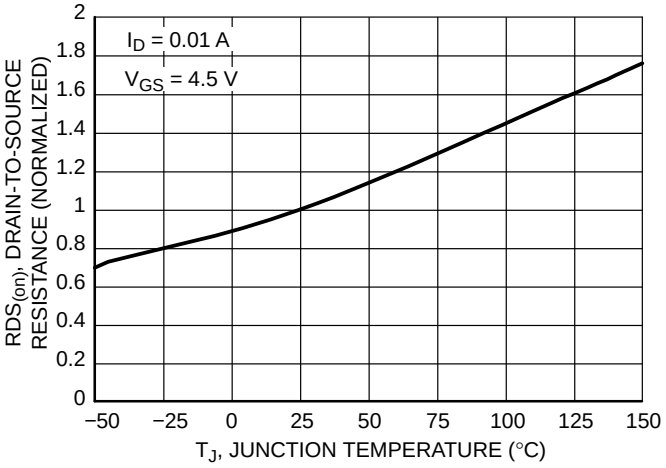


Figure 5. On-resistance Variation with Temperature

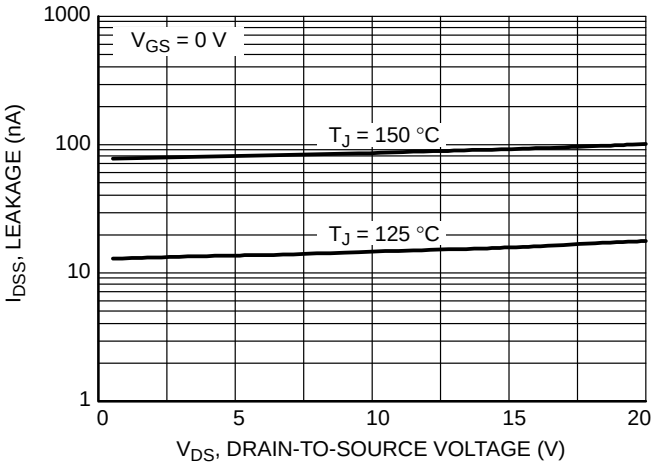


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES

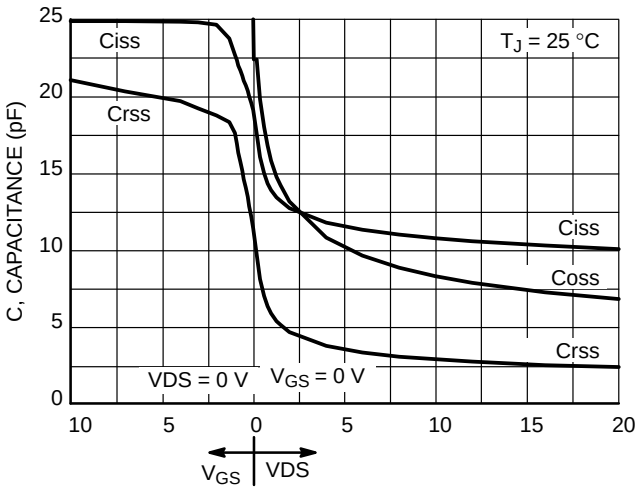


Figure 7. Capacitance Variation

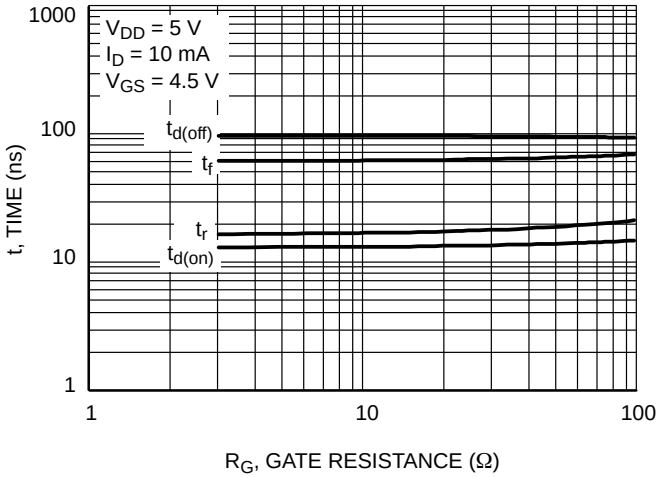


Figure 8. Resistive Switching Time Variation versus Gate Resistance

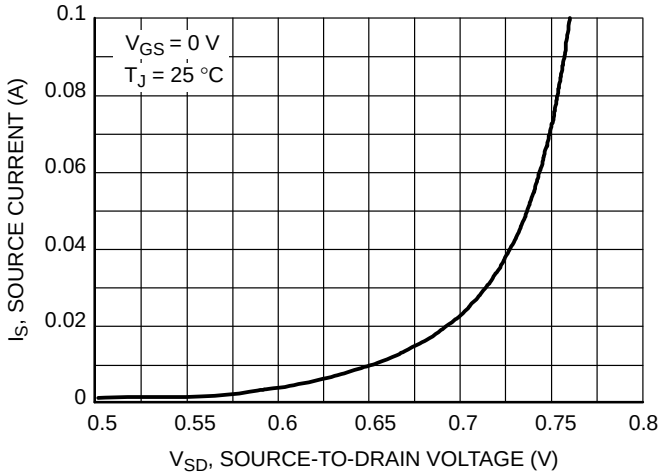


Figure 9. Diode Forward Voltage versus Current

ORDERING INFORMATION

Order Number	Package	Shipping†
NTA4001NT1G	SC-75 (Pb-Free)	3000 / Tape & Reel
NVA4001NT1G	SC-75 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

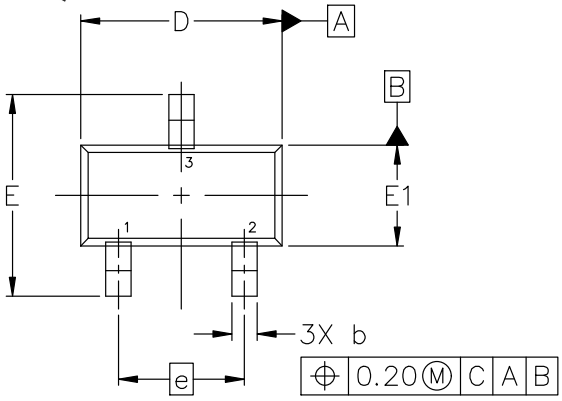
REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the Data Sheet to **onsemi** format.	6/26/2025

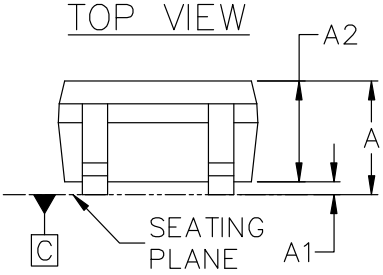
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

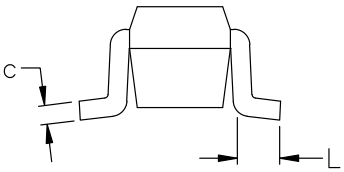
DATE 01 FEB 2024



TOP VIEW



SIDE VIEW



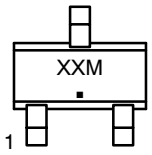
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

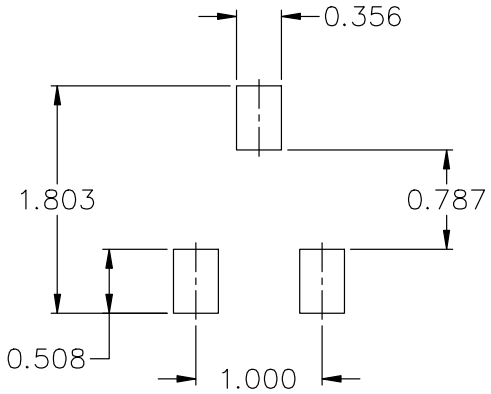
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB15184C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC75−3 1.60x0.80x0.80, 1.00P	PAGE 1 OF 1

ADDITIONAL INFORMATION

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