Low $V_{CE(sat)}$ NPN Transistors, 60 V, 1 A

NSS60101DMR6

onsemi's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and LED lightning, power management…etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25 °C)

Symbol	Rating	Max	Unit
V_{CEO}	Collector-Emitter Voltage	60	Vdc
V_{CBO}	Collector-Base Voltage	80	Vdc
V_{EBO}	Emitter-Base Voltage	6	Vdc
I_C	Collector Current - Continuous	1	A
I_{CM}	Collector Current - Peak	2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

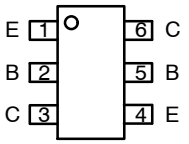
Symbol	Characteristic	Max	Unit
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (Notes 1 and 2)	234	°C/W
P_D	Total Power Dissipation per Package @ T_A = 25 °C (Note 2)	0.53	W
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient (Note 3)	300	°C/W
P_D	Power Dissipation per Transistor @ T_A = 25 °C (Note 3)	0.40	W
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C

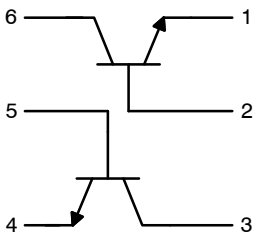
1. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Dual Operation).
2. P_D per Transistor when both are turned on is one half of Total P_D or 0.53 Watts.
3. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Single-Operation).

60 Volt, 1 Amp
NPN Low $V_{CE(sat)}$ Transistors

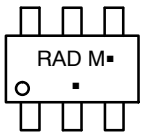
SC-74
CASE 318F

PIN CONNECTIONS





MARKING DIAGRAM



RAD = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSS60101DMR6T1G	SC-74 (Pb-Free)	3,000/ Tape & Reel
NSV60101DMR6T1G		

DISCONTINUED (Note 1)

NSS60101DMR6T2G	SC-74 (Pb-Free)	3,000/ Tape & Reel
NSV60101DMR6T2G		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	60			V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (Ic = 0.1 mA, I_E = 0)	80			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	6			V
I_{CBO}	Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)			100	nA
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 V)			100	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (Note 4) (I_C = 100 mA, V_{CE} = 2 V) (I_C = 500 mA, V_{CE} = 2 V) (I_C = 1 A, V_{CE} = 2 V) (I_C = 1 mA, V_{CE} = 5 V) (I_C = 100 mA, V_{CE} = 5 V) (I_C = 500 mA, V_{CE} = 5 V) (I_C = 1 A, V_{CE} = 5 V)	 200 150 70 250 250 200 100	 320 290 110 335 335 310 295		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 4) (I_C = 100 mA, I_B = 1 mA) (I_C = 500 mA, I_B = 50 mA) (I_C = 1 A, I_B = 50 mA) (I_C = 1 A, I_B = 100 mA)		 0.080 0.078 0.170 0.143	 0.200 0.150 0.250 0.200	V
$V_{BE(sat)}$	Base – Emitter Saturation Voltage (Note 4) (I_C = 500 mA, I_B = 50 mA) (I_C = 1 A, I_B = 50 mA) (I_C = 1 A, I_B = 100 mA)		 0.87 0.91 0.94	 1.50 1.50 1.60	V
$V_{BE(on)}$	Base-Emitter Turn-on Voltage (Note 4) (I_C = 1 mA, V_{CE} = 1 V) (I_C = 500 mA, V_{CE} = 2 V)	 0.27	 0.57 0.76	 0.90	V
DYNAMIC CHARACTERISTICS					
C_{ibo}	Input Capacitance (V_{EB} = 1 V, f = 1.0 MHz)		100		pF
C_{obo}	Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)		8.0		pF
f_T	Cutoff Frequency (I_C = 50 mA, V_{CE} = 2.0 V, f = 100 MHz)		200		MHz
SWITCHING TIMES					
t_d	Delay Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		10		ns
t_{on}	ON Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		28		ns
t_r	Rise Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		18		ns
t_s	Storage Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		622		ns
t_{off}	OFF Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		709		ns
t_f	Fall Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} =-25 mA)		87		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

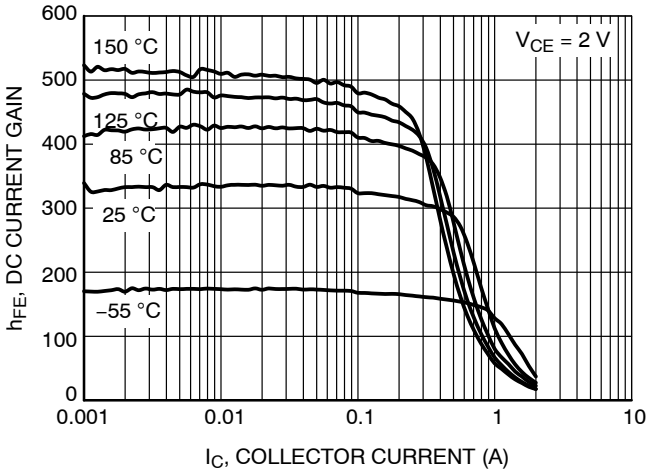


Figure 1. DC Current Gain

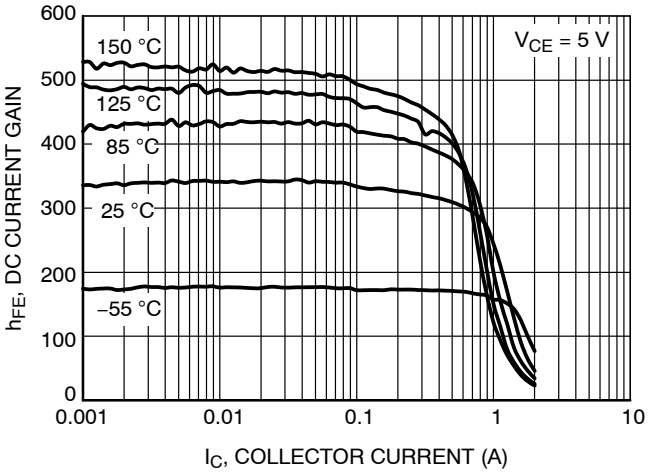


Figure 2. DC Current Gain

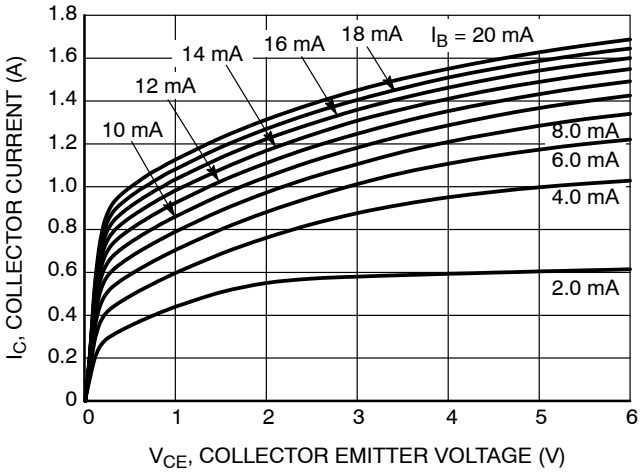


Figure 3. Collector Current as a Function of Collector Emitter Voltage

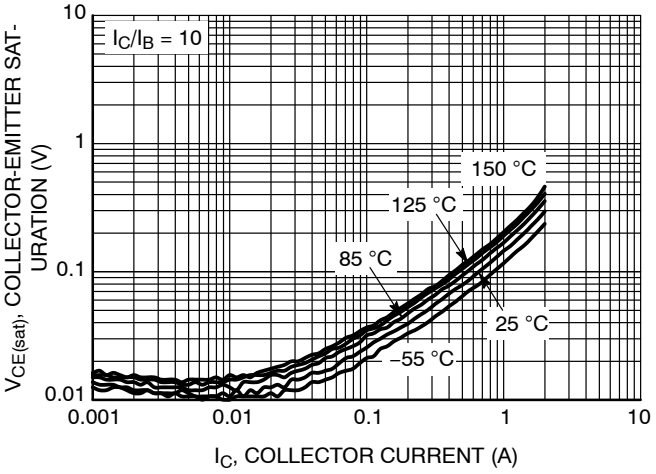


Figure 4. Collector-Emitter Saturation Voltage

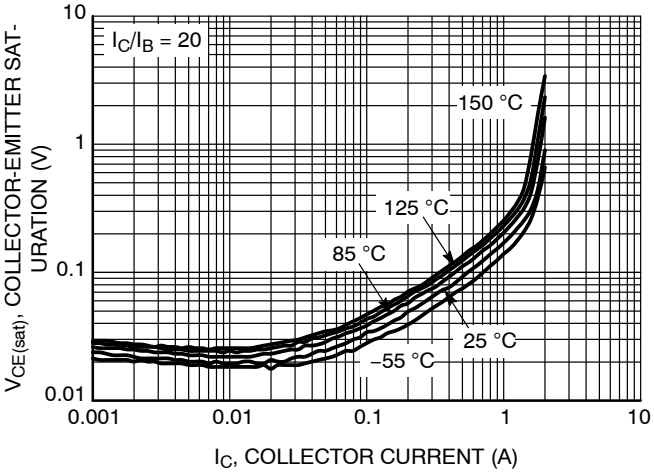


Figure 5. Collector-Emitter Saturation Voltage

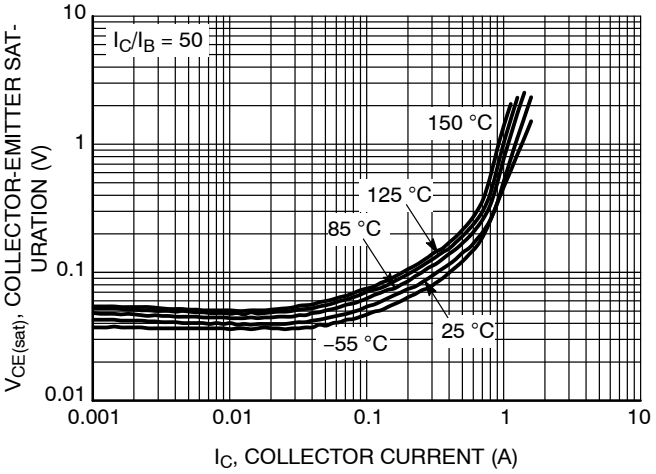


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL CHARACTERISTICS (continued)

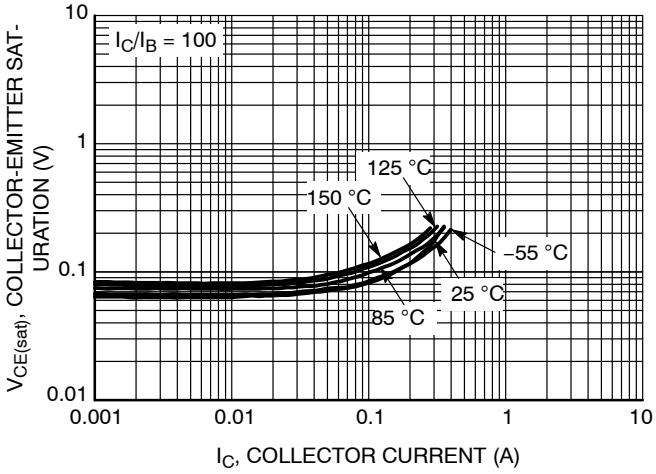


Figure 7. Collector-Emitter Saturation Voltage

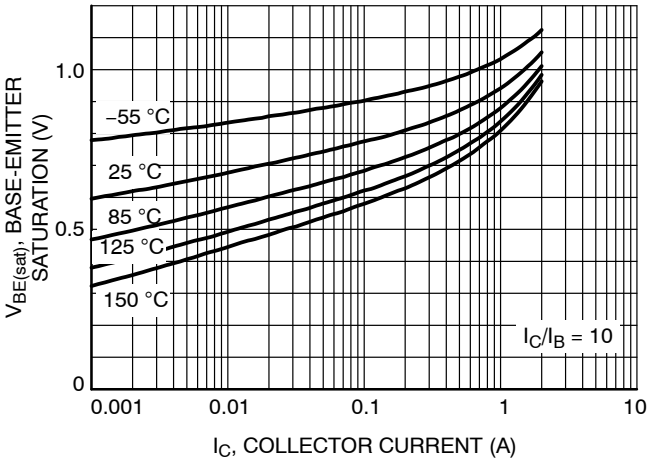


Figure 8. Base-Emitter Saturation Voltage

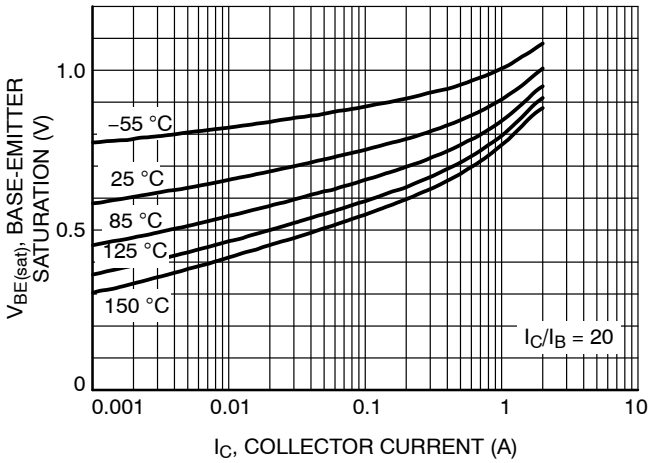


Figure 9. Base-Emitter Saturation Voltage

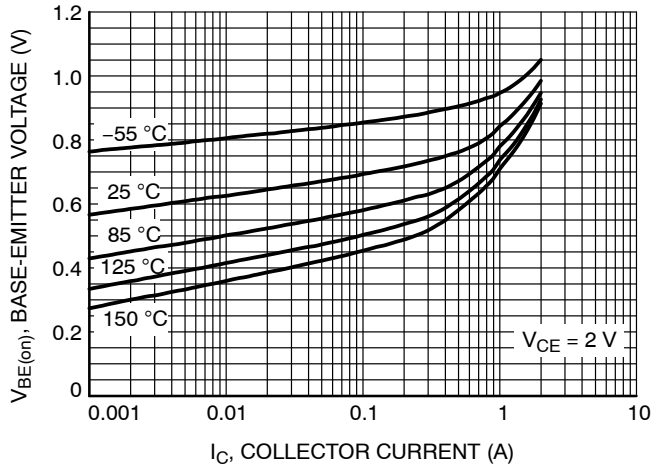


Figure 10. Base-Emitter “ON” Voltage

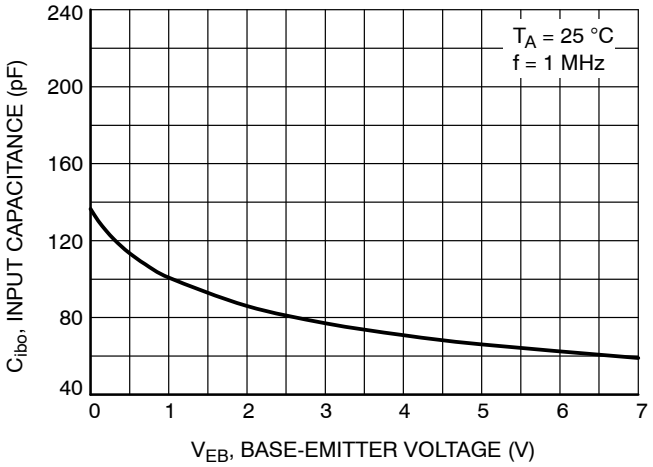


Figure 11. Input Capacitance

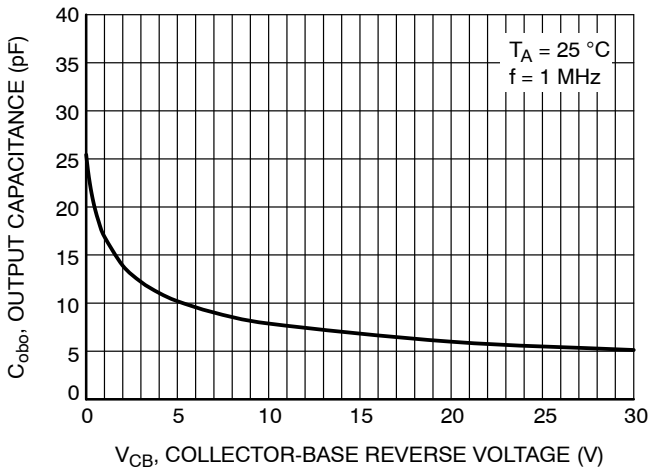


Figure 12. Output Capacitance

TYPICAL CHARACTERISTICS (continued)

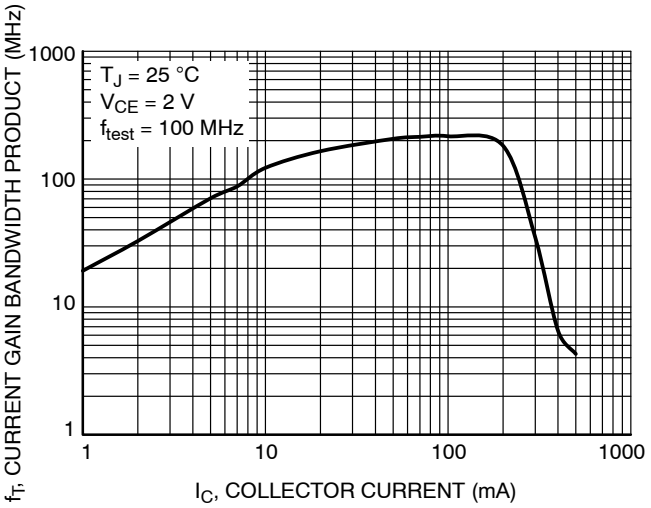


Figure 13. f_T, Current Gain Bandwidth Product

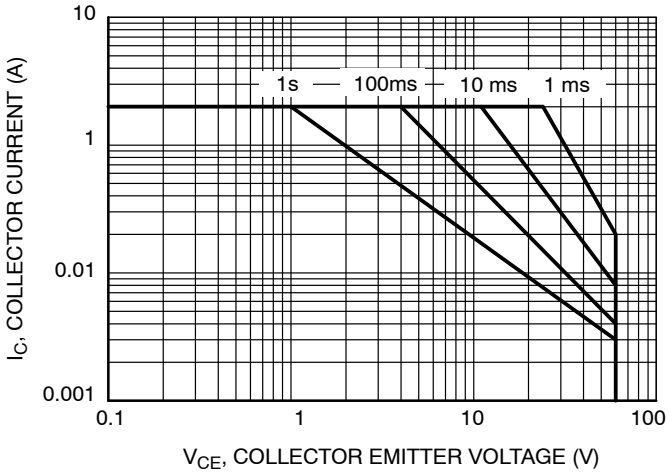


Figure 16. Safe Operating Area (T_A = 25°C)

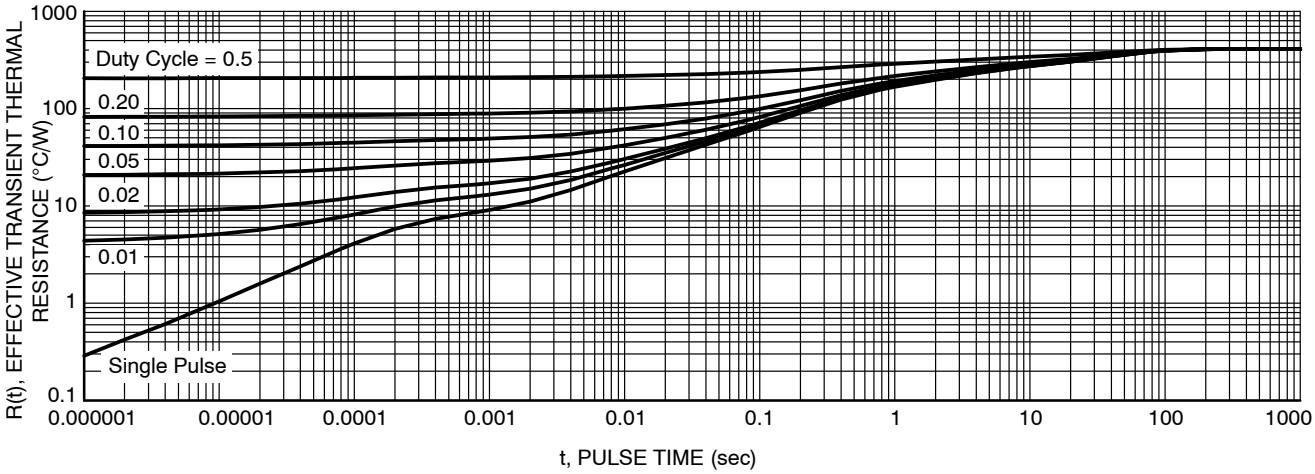


Figure 14. Thermal Resistance by Transistor

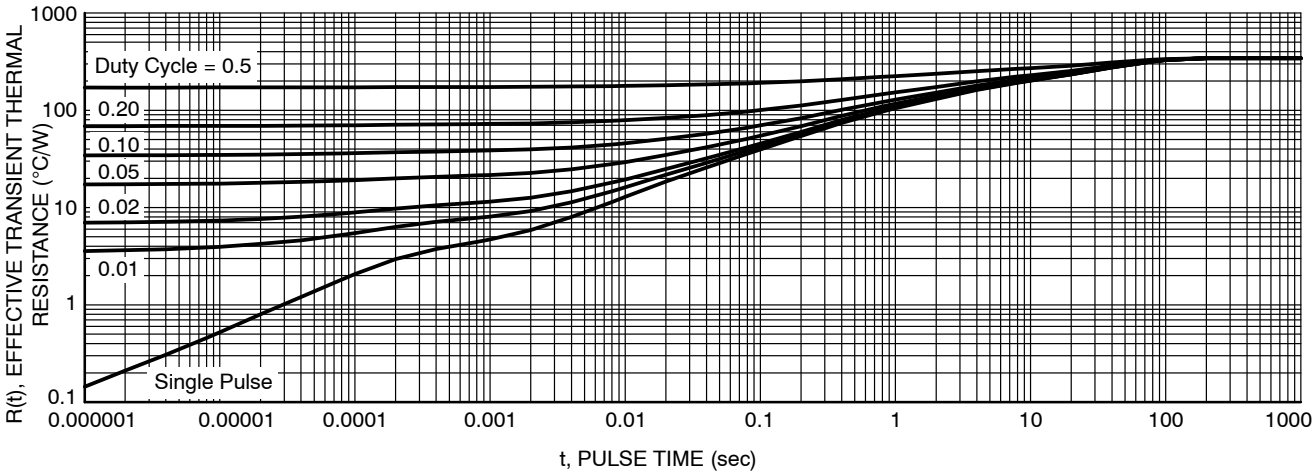
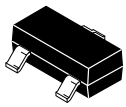


Figure 15. Thermal Resistance for Both Transistors

REVISION HISTORY

Revision	Description of Changes	Date
4	NVMFS5C456NLWFT1G, NVMFS5C456NLWFT3G OPN's Marked as Discontinued.	7/16/2025

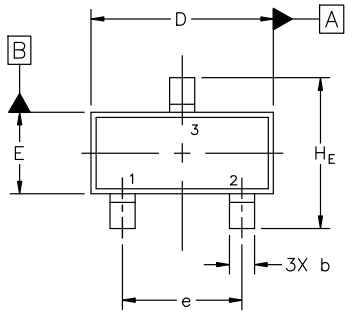
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



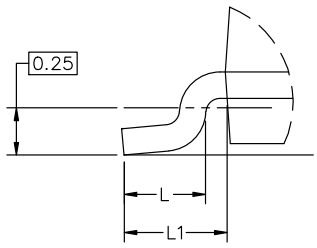
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

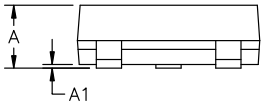
DATE 14 AUG 2024



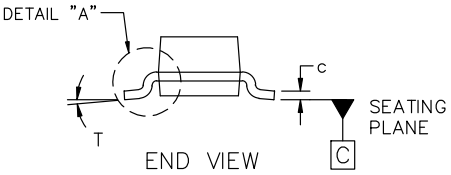
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

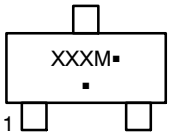


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

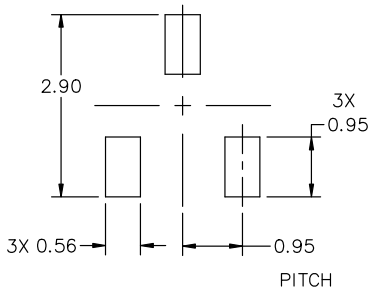
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales