NSPU3061

6.3 V Unidirectional ESD and Surge Protection Device

The NSPU3061 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, high peak pulse current handling capability and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, tablets, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

Features

- Low Clamping Voltage
- Low Leakage
- Small Body Outline: 1.0 mm x 0.6 mm
- Protection for the Following IEC Standards:
  IEC61000−4−2 Level 4: ±30 kV Contact Discharge
  IEC61000−4−5 (Lightning): 36 A (8/20 μs)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB V_{BUS} and CC Line Protection
- Microphone Line Protection
- GPIO Protection

Table 1. MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact		±30	kV
	Air		±30	
Operating Junction Temperature Range		T_J	−65 to + 150	°C
Storage Temperature Range		T_{STG}	−65 to + 150	°C
Minimum Peak Pulse Current		I_{PP}	36	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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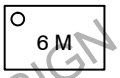
X2DFN2
CASE 714AB

MARKING DIAGRAM



6 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NSPU3061N2T5G	X2DFN2 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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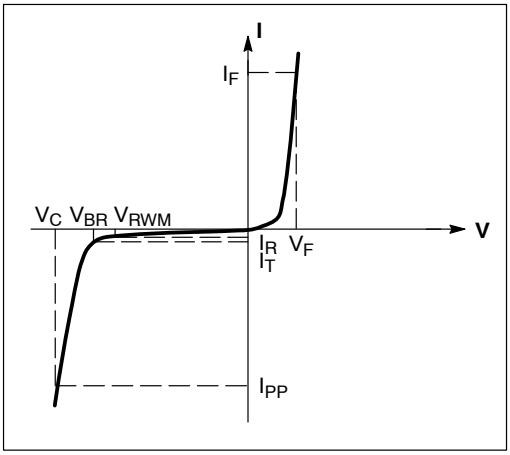
Table 2. ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional Surge Protection

Table 3. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			6.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	6.4	6.9	9.5	V
Reverse Leakage Current	I_R	V_{RWM} = 6.3 V, I/O Pin to GND		0.02	1	μA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ± 8 kV Contact	See Figures 2 & 3			V
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A IEC61000−4−2 Level 2 Equivalent (±4 kV Contact, ± 8 kV Air)		6.4		V
		I_{PP} = 16 A IEC61000−4−2 Level 4 Equivalent (±8 kV Contact, ± 15 kV Air)		6.6		
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8x20 μs) per Figure 1	36	40		A
Clamping Voltage 8x20 μs Waveform per Figure 1	V_C	I_{PP} = 20 A I_{PP} = 30 A I_{PP} = 36 A		6.6 7.3 7.7	8.0 9.0 9.7	V
Dynamic Resistance	R_{DYN}	100 ns TLP		0.025		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		90	110	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see application note AND8307/D
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

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TYPICAL CHARACTERISTICS

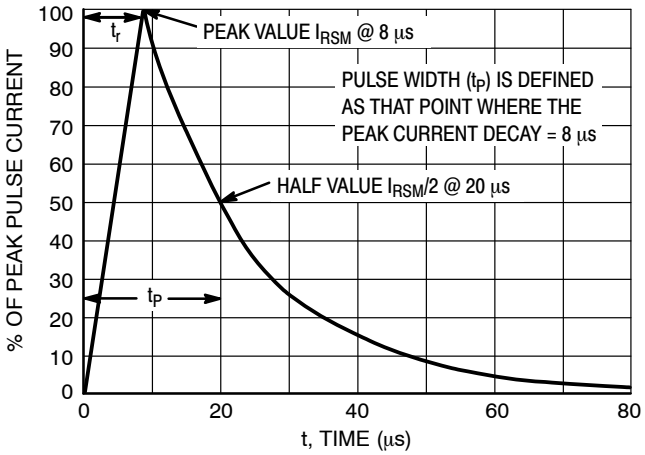

Figure 1. 8 x 20 μs Pulse Waveform

TYPICAL CHARACTERISTICS

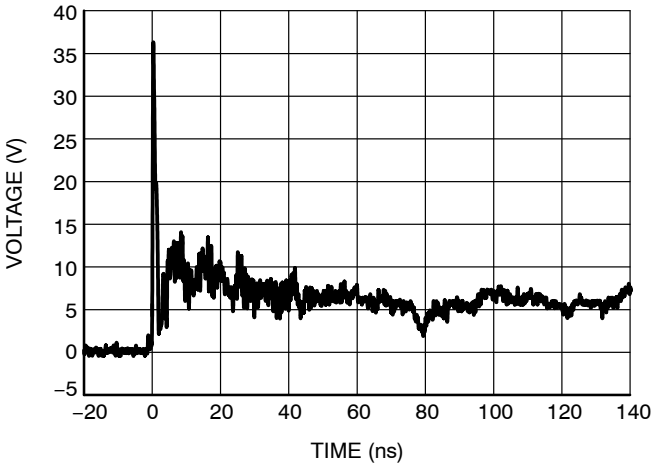

Figure 2. ESD Clamping Voltage Positive 8 kV Contact per IEC61000−4−2

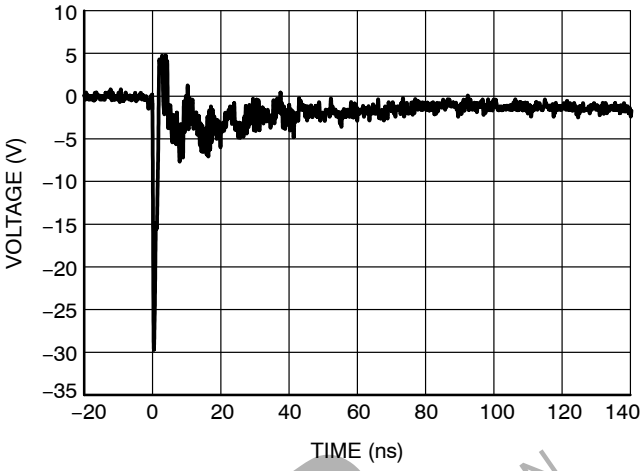

Figure 3. ESD Clamping Voltage Negative 8 kV Contact per IEC61000−4−2

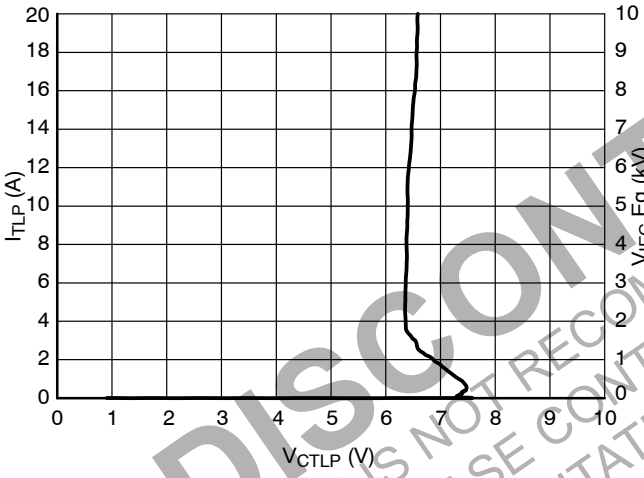

Figure 4. Positive TLP I−V Curve

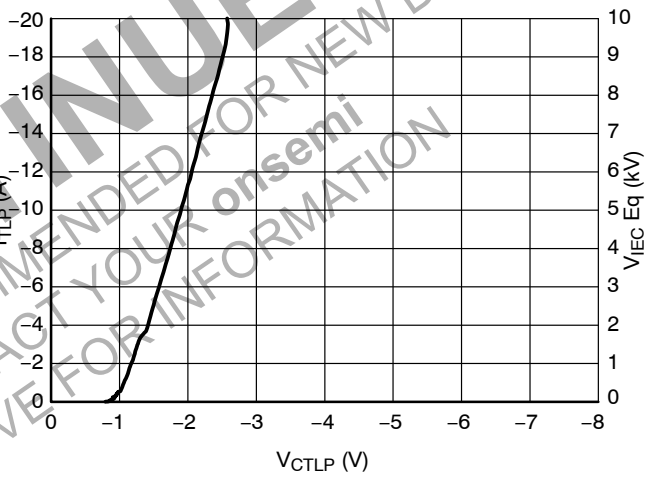

Figure 5. Negative TLP I−V Curve

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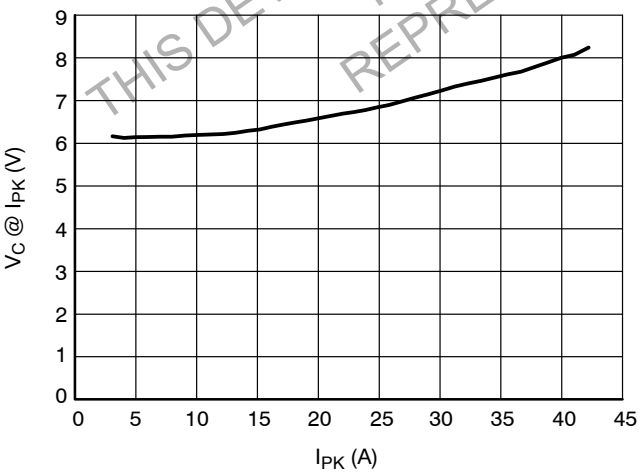

Figure 6. Positive Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

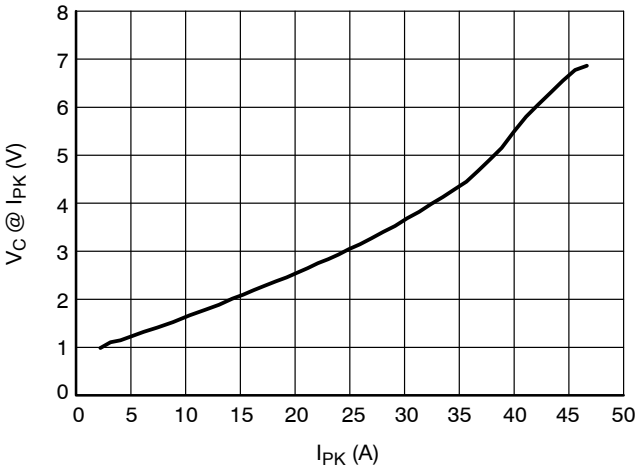

Figure 7. Negative Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

TYPICAL CHARACTERISTICS

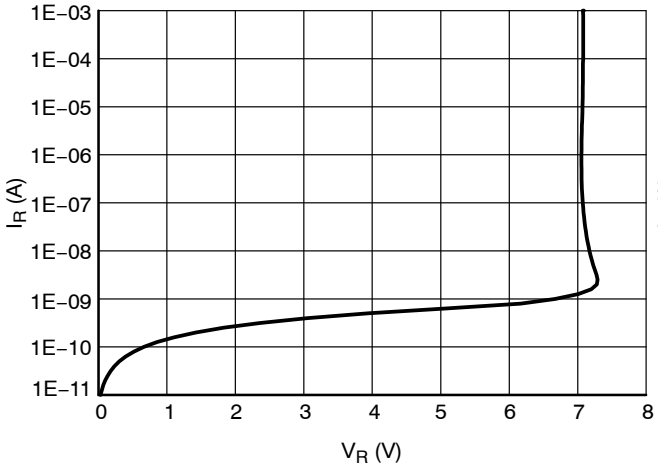

Figure 8. Breakdown Voltage

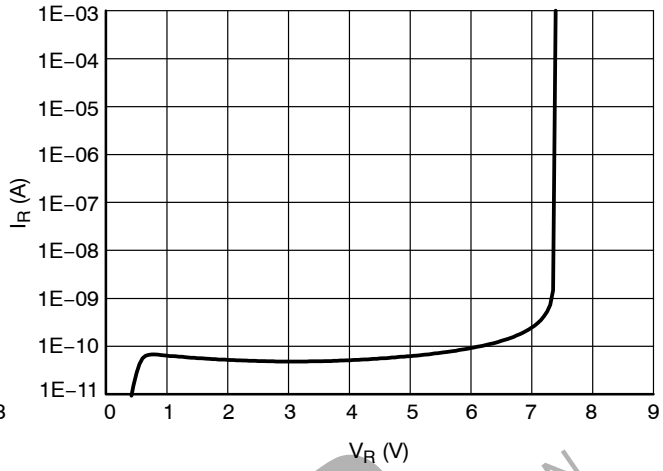

Figure 9. Reverse Leakage Current

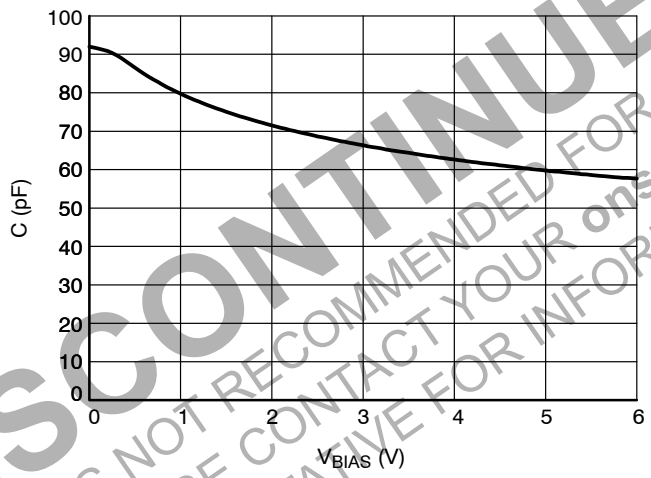

Figure 10. Line Capacitance, *f* = 1 MHz

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Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 11. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 12 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

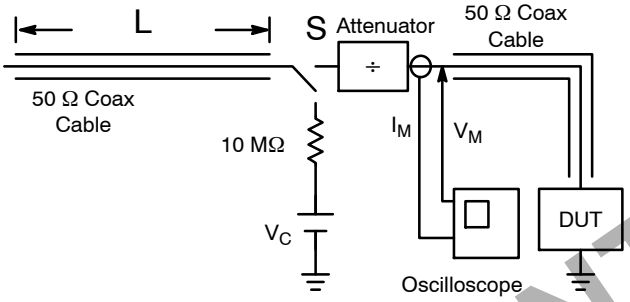

Figure 11. Simplified Schematic of a Typical TLP System

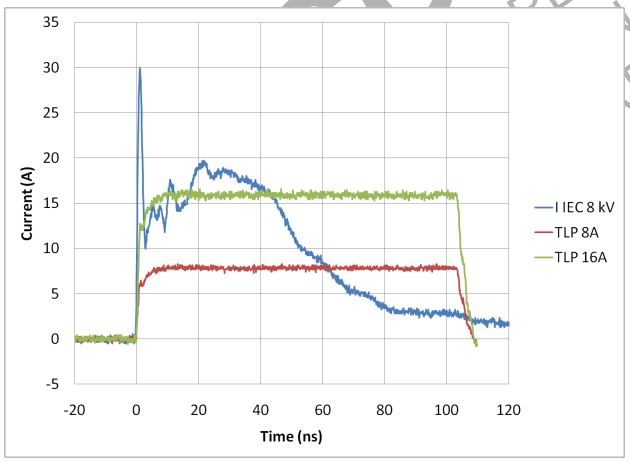

Figure 12. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

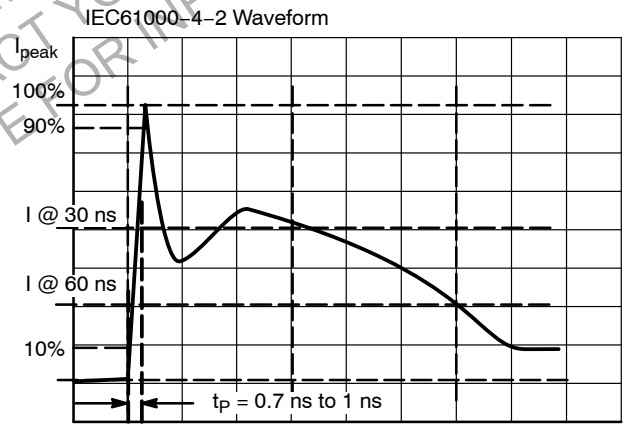

Figure 13. IEC61000−4−2 Spec

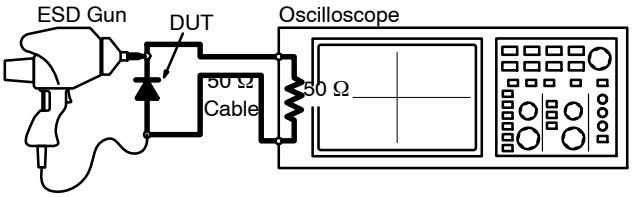

Figure 14. Diagram of ESD Test Setup

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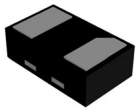
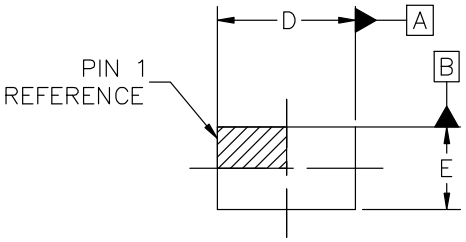
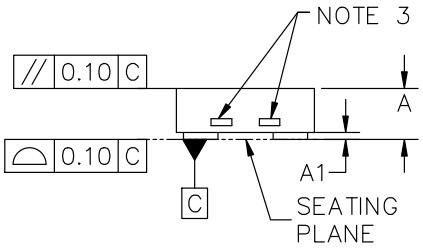


X2DFN2 1.00x0.60x0.37, 0.65P
CASE 714AB
ISSUE C

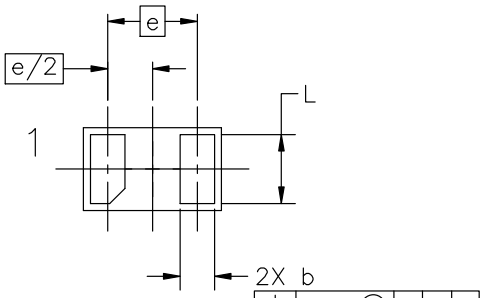
DATE 21 FEB 2024



TOP VIEW



SIDE VIEW

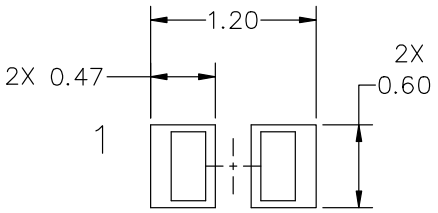


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOW.

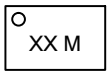
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	−−−	0.03	0.050
b	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.45	0.50	0.55



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	X2DFN2 1.00x0.60x0.37, 0.65P	PAGE 1 OF 1

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