

# NLU1GT86

## Single 2-Input Exclusive OR Gate, TTL Level

### LSTTL-Compatible Inputs

The NLU1GT86 MiniGate™ is an advanced CMOS high-speed 2-input Exclusive OR gate in ultra-small footprint.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing.

The NLU1GT86 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

#### Features

- High Speed:  $t_{PD} = 3.1 \text{ ns}$  (Typ) @  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 1 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- TTL-Compatible Input:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- CMOS-Compatible Output:  
 $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @ Load
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Ultra-Small Packages
- These are Pb-Free Devices

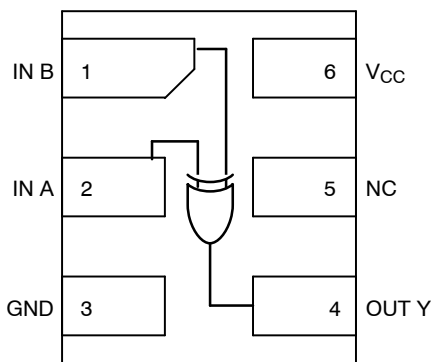


Figure 1. Pinout (Top View)

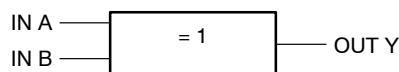


Figure 2. Logic Symbol

#### FUNCTION TABLE

Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

#### PIN ASSIGNMENT

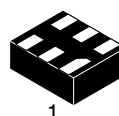
1	IN B
2	IN A
3	GND
4	OUT Y
5	NC
6	$V_{CC}$



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#### MARKING DIAGRAMS



UDFN6  
1.2 x 1.0  
CASE 517AA



6 = Device Marking  
M = Date Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# NLU1GT86

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage	-0.5 to +7.0	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-20	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	±20	mA
$I_O$	DC Output Source/Sink Current	±12.5	mA
$I_{CC}$	DC Supply Current Per Supply Pin	±25	mA
$I_{GND}$	DC Ground Current per Ground Pin	±25	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 150 N/A	V
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	Digital Input Voltage	0	5.5	V
$V_{OUT}$	Output Voltage	0	5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0	100 20	ns/V

# DC ELECTRICAL CHARACTERISTICS

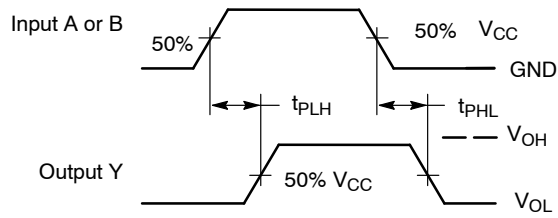
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			T <sub>A</sub> = +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Low-Level Input Voltage		3.0 4.5 to 5.5	1.4 2.0			1.4 2.0		1.4 2.0		V
V <sub>IL</sub>	Low-Level Input Voltage		3.0 4.5 to 5.5			0.53 0.8		0.53 0.8		0.53 0.8	V
V <sub>OH</sub>	High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 µA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 µA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	µA
I <sub>CC</sub>	Quiescent Supply Current	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	5.5			1.0		20		40	µA
I <sub>CC(T)</sub>	Quiescent Supply Current	V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	µA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

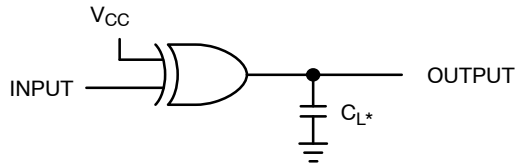
Symbol	Parameter	V <sub>CC</sub> (V)	Test Condition	T <sub>A</sub> = 25 °C			T <sub>A</sub> = +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Input A to Output Y	3.0 to 3.6	C <sub>L</sub> = 15 pF		5.0	11.0		13.0		15.5	ns
			C <sub>L</sub> = 50 pF		6.2	14.5		16.5		19.5	
		4.5 to 5.5	C <sub>L</sub> = 15 pF		3.1	6.8		6.0		10.0	
			C <sub>L</sub> = 50 pF		4.2	8.8		10.0		12.0	
C <sub>IN</sub>	Input Capacitance				5.5	10		10		10.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	5.0			11						pF

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NLU1GT86



**Figure 3. Switching Waveforms**



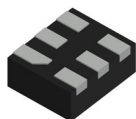
\*Includes all probe and jig capacitance.  
A 1-MHz square input wave is recommended for propagation delay tests.

**Figure 4. Test Circuit**

### ORDERING INFORMATION

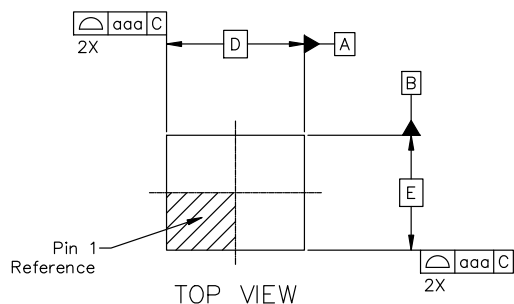
Device	Package	Shipping†
NLU1GT86MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



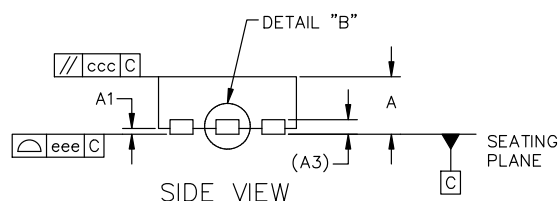
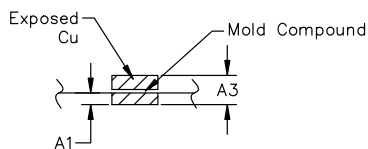
UDFN6, 1.20x1.00x0.50, 0.40P  
CASE 517AA  
ISSUE E

DATE 09 MAY 2025

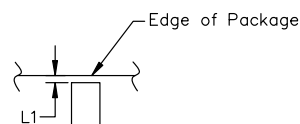


NOTES:

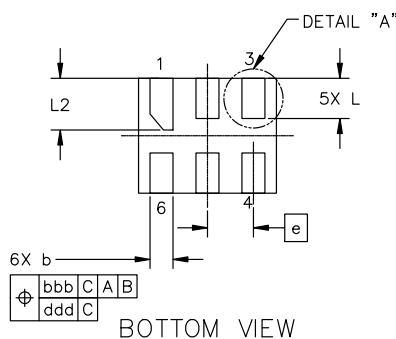
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO TH EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL "B"  
Scale 2:1  
Side View  
(Optional)



DETAIL "A"  
Scale 2:1  
Bottom View  
(Optional)



PIN 1  
Chamfer Dimension

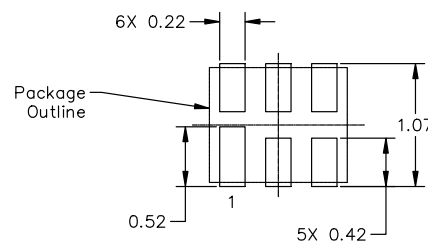
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.127 REF		
b	0.15	0.20	0.25
D	1.20 BSC		
E	1.00 BSC		
e	0.40 BSC		
L	0.30	0.35	0.40
L1	0.00	---	0.15
L2	0.40	0.45	0.50
L3	0.14 REF		
L4	0.116 REF		
TOLERANCE FORM & POSITION			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



### RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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