Intelligent Power Module (IPM)
Inverter, 1200 V, 15 A

Preliminary Document

NFA31512L72D

NFA31512L72D is an advanced IPM module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certification: E209204
- 1200 V / 15 A 3-phase IGBT Inverter with Integral Gate Drivers and Protections
- Built-in Under-Voltage Protection (UVP)
- Built-in Bootstrap Diodes / Resistors
- Separated Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- LVIC Temperature-Sensing Built-In for Temperature Monitoring
- Isolation Rating: 2500 Vrms / 1 min.
- Good Thermal Conductivity with Al2O3 DBC
- This Device is Pb-Free and is RoHS Compliant

Typical Applications

- Industrial Drives, Pumps, Fans, Automations

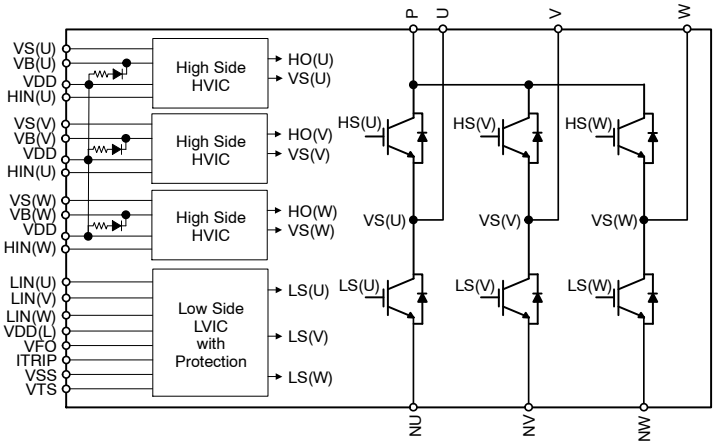
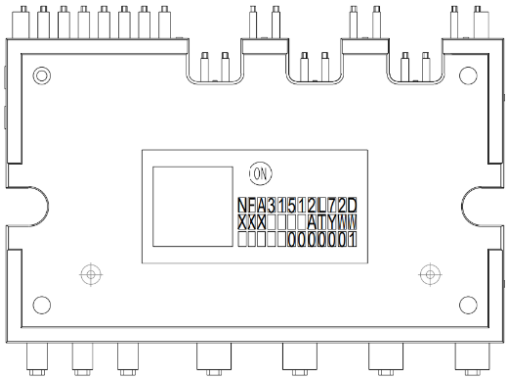


Figure 1. Pin Configuration – Top View

3D Package Drawing
(Click to Active 3D Content)

SPMUA-027 / PDD STD, SPM27-UA, DBC TYPE CASE MODFJ

MARKING DIAGRAM



NFA31512L72D	= Specific Device Code
XXX	= Last 3 Digits of Lot No
AT	= Assembly & Test Site
YWW	= Year and Work Week Code
0000001	= Serial Number

ORDERING INFORMATION

Device	Package	Shipping
NFA31512L72D	SPM27-UA	60 Units / Tube

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

PIN CONFIGURATION

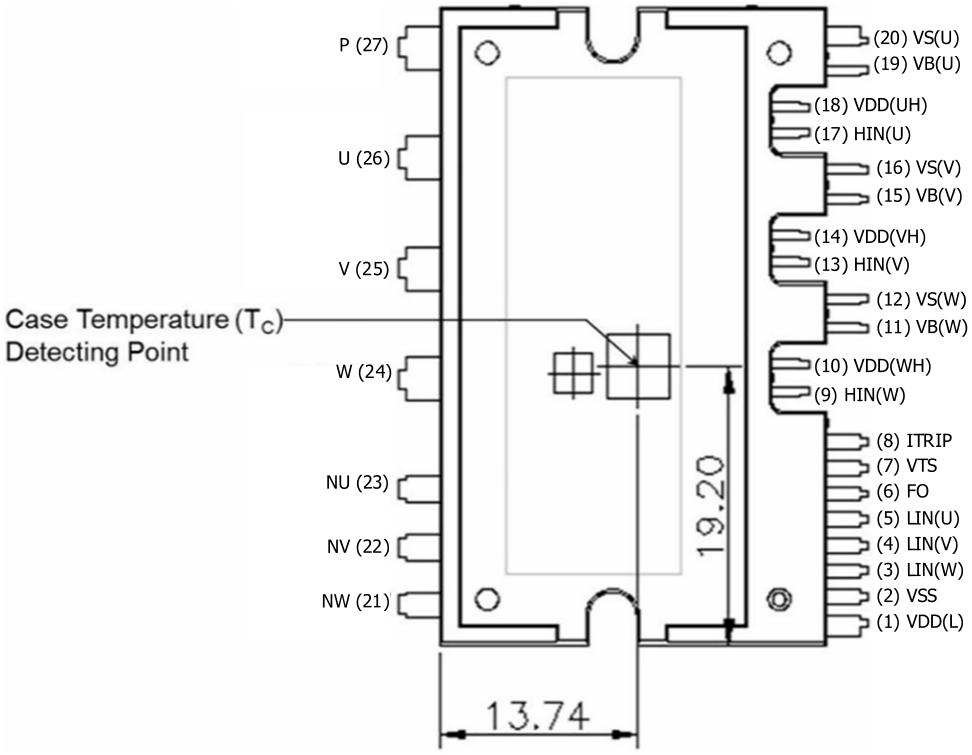


Figure 2. Pin Configuration – Top View

PIN DESCRIPTION

Pin No.	Symbol	Description
1	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
2	VSS	Low-Side Common Supply Ground
3	LIN(W)	Signal Input for Low-Side W-Phase
4	LIN(V)	Signal Input for Low-Side V-Phase
5	LIN(U)	Signal Input for Low-Side U-Phase
6	FO	Fault Output
7	VTS	Output for LVIC Temperature Sensing Voltage Output
8	ITRIP	Shut Down Input for Over Current Detection Input
9	HIN(W)	Signal Input for High-Side W-Phase
10	VDD(WH)	High-Side Bias Voltage for W-Phase IC
11	VB(W)	High-Side Bias Voltage for W-Phase IGBT Driving
12	VS(W)	High-Side Bias Voltage Ground for W-Phase IGBT Driving
13	HIN(V)	Signal Input for High-Side V-Phase
14	VDD(VH)	High-Side Bias Voltage for V-Phase IC
15	VB(V)	High-Side Bias Voltage for V-Phase IGBT Driving
16	VS(V)	High-Side Bias Voltage Ground for V-Phase IGBT Driving
17	HIN(U)	Signal Input for High-Side U-Phase
18	VDD(UH)	High-Side Bias Voltage for U-Phase IC
19	VB(U)	High-Side Bias Voltage for U-Phase IGBT Driving
20	VS(U)	High-Side Bias Voltage Ground for U-Phase IGBT Driving
21	NW	Negative DC-Link Input for W-Phase
22	NV	Negative DC-Link Input for V-Phase
23	NU	Negative DC-Link Input for U-Phase
24	W	Output for W-Phase
25	V	Output for V-Phase
26	U	Output for U-Phase
27	P	Positive DC-Link Input

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS

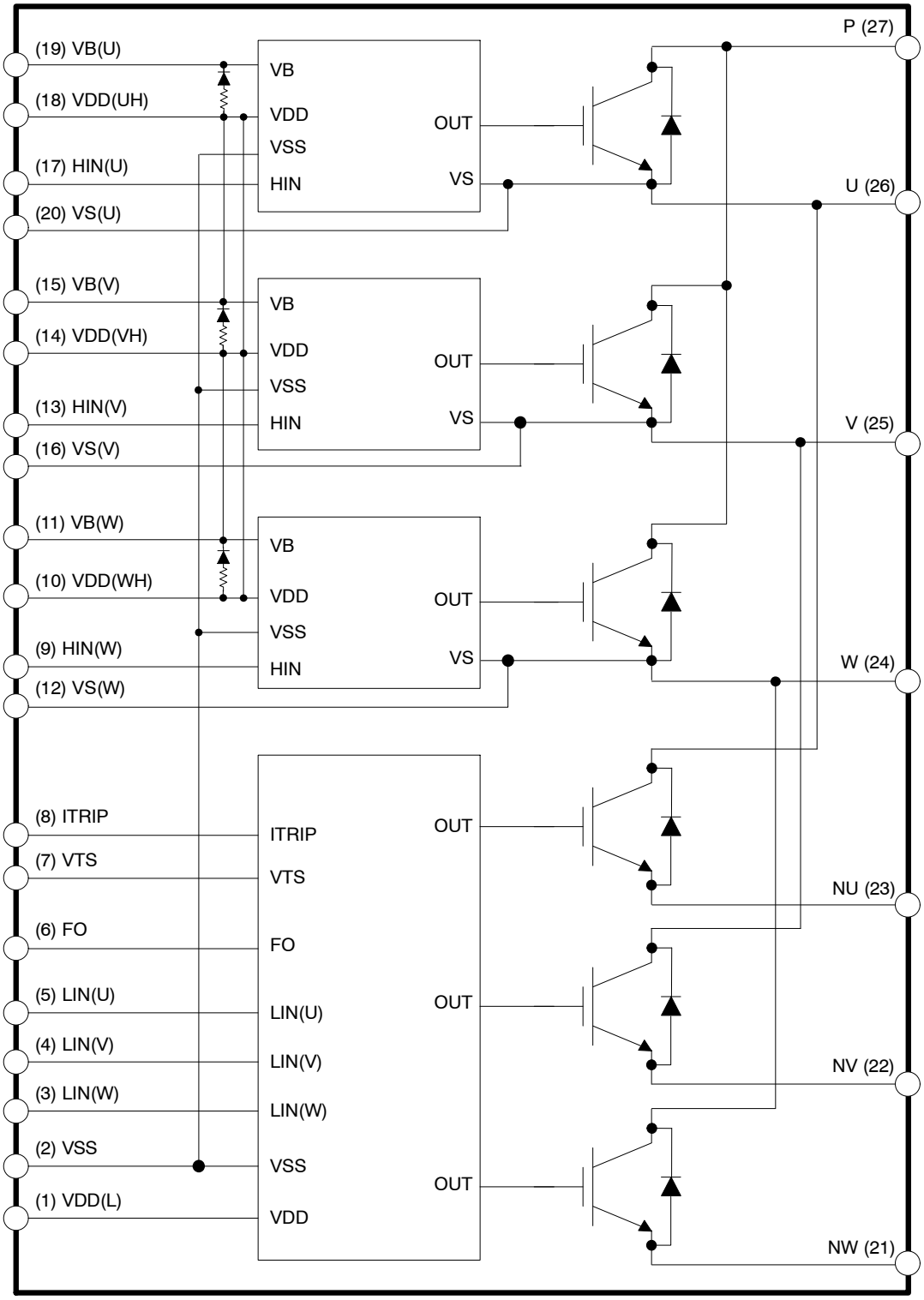


Figure 3. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C, V_{DD} = 15 V, V_{BS} = 15 V, unless otherwise specified)

Symbol	Parameter	Test Condition	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW	900	V
$V_{PN(surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 1)	1000	V
V_{CES}	Collector-Emitter Voltage	P to U, V, W; U to NU, V to NV, W to NW	1200	V
I_C	Output Current	P, NU, NV, NW, U, V, W terminal current	15	A
I_{CP}	Output Peak Current	P, NU, NV, NW, U, V, W terminal current Under 1 ms Pulse Width	30	A
P_D	Power Dissipation	T_C = 25 °C per One Chip (Note 3)	80.7	W
T_J	Operating Junction Temperature	IGBT (Note 4)	−40 ~ 150	°C
CONTROL PART				
V_{DD}	Control Supply Voltage	Applied between VDD(H), VDD(L) – VSS	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	20	V
V_{IN}	Input Signal Voltage	Applied between HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	−0.3 ~ VDD + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between FO – VSS	−0.3 ~ VDD + 0.3	V
I_{FO}	Fault Output Current	Sink Current at FO pin	2	mA
V_{ITRIP}	Current Sensing Input Voltage	Applied between VITRIP – VSS	−0.3 ~ VDD + 0.3	V
TOTAL SYSTEM				
$V_{PN(prot)}$	Self-Protection Supply Voltage Limit (Short Circuit Protection Capability)	V_{DD} = V_{BS} = 13.5 ~ 16.5 V, T_J = 150 °C, Non-repetitive, < 2 μs	800	V
T_C	Case Operation Temperature	See Figure 2	−40 ~ 125	°C
T_{stg}	Storage Temperature		−40 ~ 125	°C
V_{iso}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance (Note 5)	IGBT per 1/6 module			1.55	°C/W
$R_{th(j-c)F}$		FWDi per 1/6 module			2.40	°C/W

1. Surge voltage generated by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
2. This is not for continuous DC voltage, Recommend to use max 960 V (80% of rated voltage) for continuous DC voltage.
3. This is calculated value determined by the design factor values.
4. The allowable maximum junction temperature of power chips is 175 °C, however to ensure safe operation, the average junction temperature is recommended to be limited to $T_{J.Avg} \leq 150$ °C.
5. For the measurement point of case temperature (T_C), please refer to Figure 2.

ELECTRICAL CHARCTERISTICS (T_J = 25 °C, V_{DD} = 15 V, V_{BS} = 15 V, unless otherwise specified)

Symbol		Parameter	Test Condition	Min	Typ	Max	Unit
INVERTER PART							
$V_{CE(sat)}$		Collector-Emitter Saturation Voltage	V_{IN} = 5 V, I_C = 10 A, T_J = 25 °C		1.50	1.90	V
			V_{IN} = 5 V, I_C = 10 A, T_J = 150 °C		1.75		
V_F		FWDi Forward Voltage	V_{IN} = 0 V, I_F = 10 A, T_J = 25 °C		1.70	2.10	V
			V_{IN} = 0 V, I_F = 10 A, T_J = 150 °C		1.65		
HS	t_{on}	High Side Switching Times	V_{PN} = 600 V, I_C = 10 A, T_J = 25 °C V_{IN} = 0 V ↔ 5 V, Inductive Load See Figure 4 (Note 6)			1.10	μs
	$t_{c(on)}$					0.25	
	t_{off}					1.00	
	$t_{c(off)}$					0.35	
	t_{rr}				0.15		
LS	t_{on}	Low Side Switching Times	V_{PN} = 600 V, I_C = 10 A, T_J = 25 °C V_{IN} = 0 V ↔ 5 V, Inductive Load See Figure 4 (Note 6)			0.85	μs
	$t_{c(on)}$					0.25	
	t_{off}					0.95	
	$t_{c(off)}$					0.35	
	t_{rr}				0.20		
I_{CES}		Collector-Emitter Leakage Current	T_J = 25 °C, V_{CE} = V_{CES}			1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

SWITCHING TIME DEFINITION

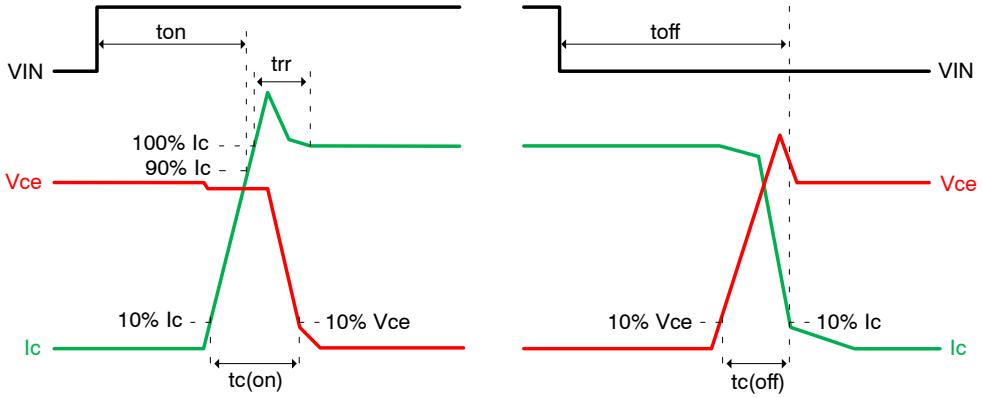


Figure 4. Switching Time Definition

ELECTRICAL CHARCTERISTICS (T_J = 25 °C, V_{DD} = 15 V, V_{BS} = 15 V, unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
CONTROL PART							
I_{QDDH}	Quiescent VDD Supply Current	HIN(U,V,W) = 0 V	VDD(H) – VSS			0.30	mA
I_{QDDL}		LIN(U,V,W) = 0 V	VDD(L) – VSS			5.0	mA
I_{PDDH}	Operating VDD Supply Current	fPWM = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side	VDD(H) – VSS			0.50	mA
I_{PDDL}		fPWM = 20 kHz, duty = 50%, applied to one PWM signal input for Low-Side	VDD(L) – VSS			6.00	mA
I_{QBS}	Quiescent VBS Supply Current	HIN(U, V, W) = 0 V	VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)			0.30	mA
I_{PBS}	Operating VBS Supply Current	fPWM = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side	VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)			2.50	mA
$V_{IN(on)}$	ON Threshold Voltage	HIN(U, V, W) – VSS, LIN(U, V, W) – VSS				2.6	V
$V_{IN(off)}$	OFF Threshold Voltage			0.8			V
$V_{ITRIP(ref)}$	Over Current Trip Level	V_{DD} = 15 V	ITRIP – VSS	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit Under-Voltage Protection	V_{DD} supply undervoltage negative going input threshold		10.3		12.8	V
UV_{DDR}		V_{DD} supply undervoltage positive going input threshold		10.8		13.3	V
UV_{BSD}		V_{BS} supply undervoltage negative going input threshold		9.5		12.0	V
UV_{BSR}		V_{BS} supply undervoltage positive going input threshold		10.0		12.5	V
V_{TS}	LVIC Temperature Sensing Voltage Output	$V_{DD(L)}$ = 15 V, T_{LVIC} = 25 °C (Note 7) See Figure 5		0.88	0.98	1.08	V
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{ITRIP} = 0 V, VFO pin pulled up to 5 V by 10 kΩ Resistor		4.5			V
V_{FOL}		V_{DD} = 15 V, V_{ITRIP} = 1 V, VFO pin pulled up to 5 V by 10 kΩ Resistor				0.5	V
t_{FOD}	Fault Out Pulse Width	VFO – VSS		50			μs
BOOTSTRAP PART							
V_F	Bootstrap Diode Forward Current	I_F = 10 mA (See Figure 7)		0.70	1.05	1.40	V
R_{BOOT}	Built-in Limiting Resistance			16	21	26	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. T_{LVIC} is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown IGBT's automatically. The relationship between VTS voltage output and LVIC temperature is described in Figure 5.

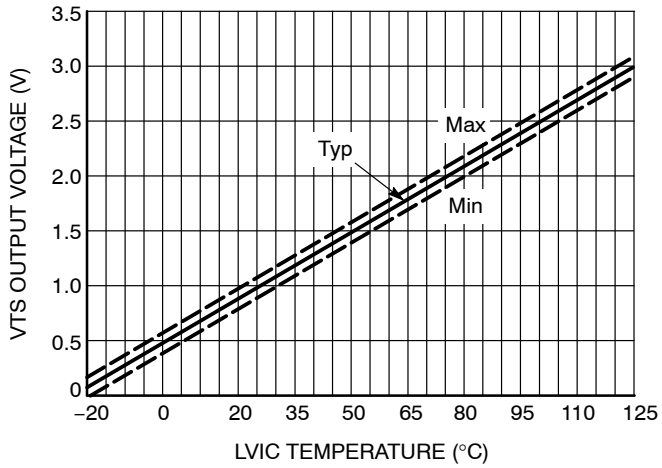


Figure 5. Temperature of LVIC vs. VTS Characteristics

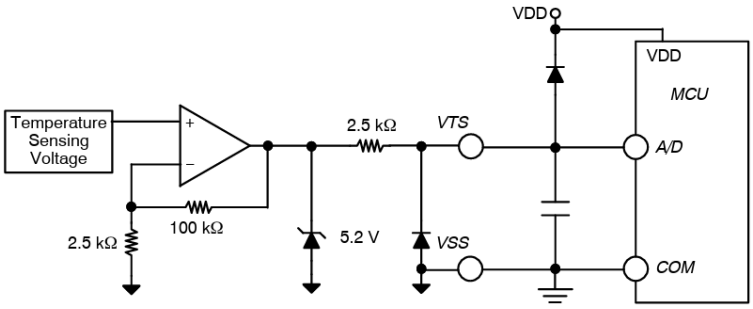


Figure 6. Internal Block Diagram and Interface Circuit of VTS

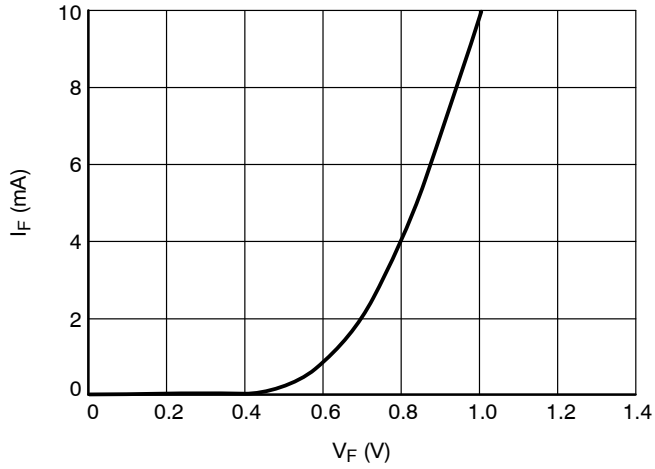


Figure 7. I-V Characteristics of BSDR

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min	Min	Max	Unit
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW		600	800	V
V_{DD}	Control Supply Voltage	Applied between VDD – VSS	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	13.0	15.0	18.5	V
dV_{DD} / dt, dV_{BS} / dt	Control Supply Variation		–1		1	V/μs
t_{dead}	Dead Time	Turn-off to Turn-on (external)	1.5			μs
f_{PWM}	PWM Input Signal	–40 °C ≤ T_C ≤ 125 °C, –40 °C ≤ T_J ≤ 150 °C			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between NU, NV, NW – VSS (Including Surge Voltage)	–5		5	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	V_{DD} = V_{BS} = 15 V, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH (Note 8)	1.5			μs
$PW_{IN(OFF)}$			2.0			

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. This product might not respond if input pulse width is less than the recommended value.

TIME CHARTS OF PROTECTIVE FUNCTION

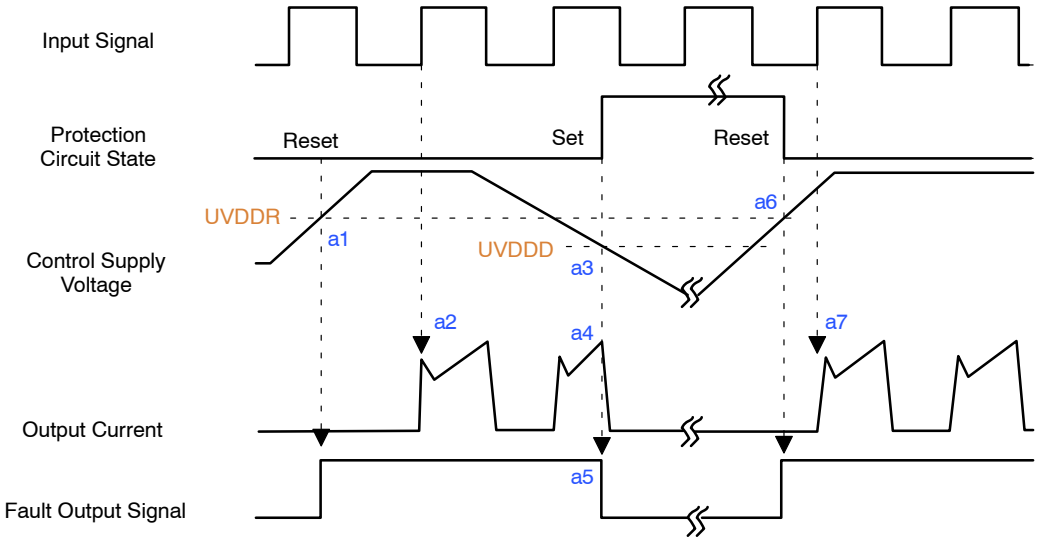


Figure 8. Under-Voltage Protection (Low-Side)

a1: Control supply voltage rises: After the voltage rises UVDDR, the circuits start to operate when next input is applied.
a2: Normal operation: IGBT ON and carrying current.
a3: Under voltage detection (UVDDD).
a4: IGBT OFF in spite of control input condition.
a5: Fault output operation starts with a fixed pulse width.
a6: Under voltage reset (UVDDR).
a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

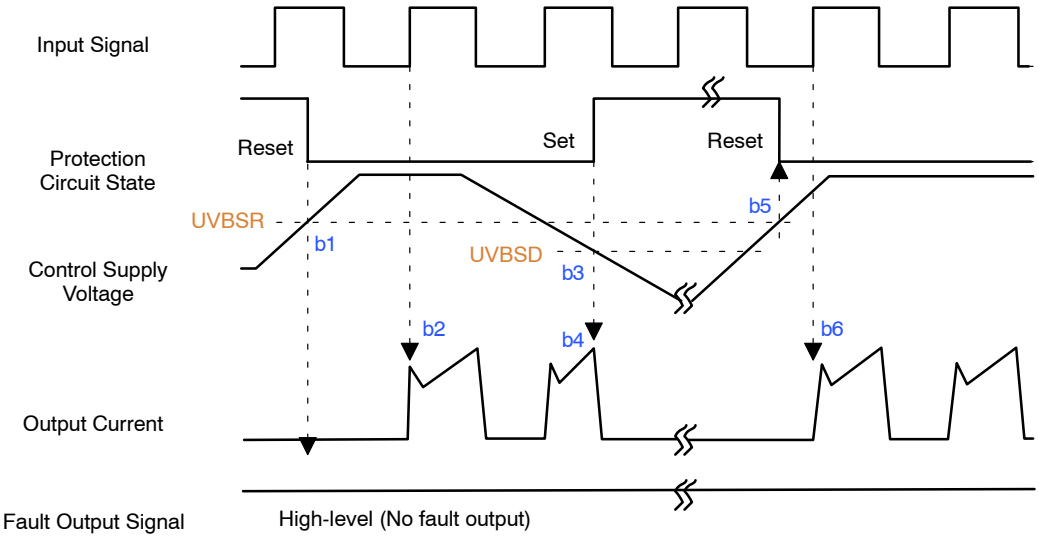


Figure 9. Under-Voltage Protection (High-Side)

b1: Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.
b2: Normal operation: IGBT ON and carrying current.
b3: Under voltage detection (UVBSD).
b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
b5: Under voltage reset (UVBSR).
b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

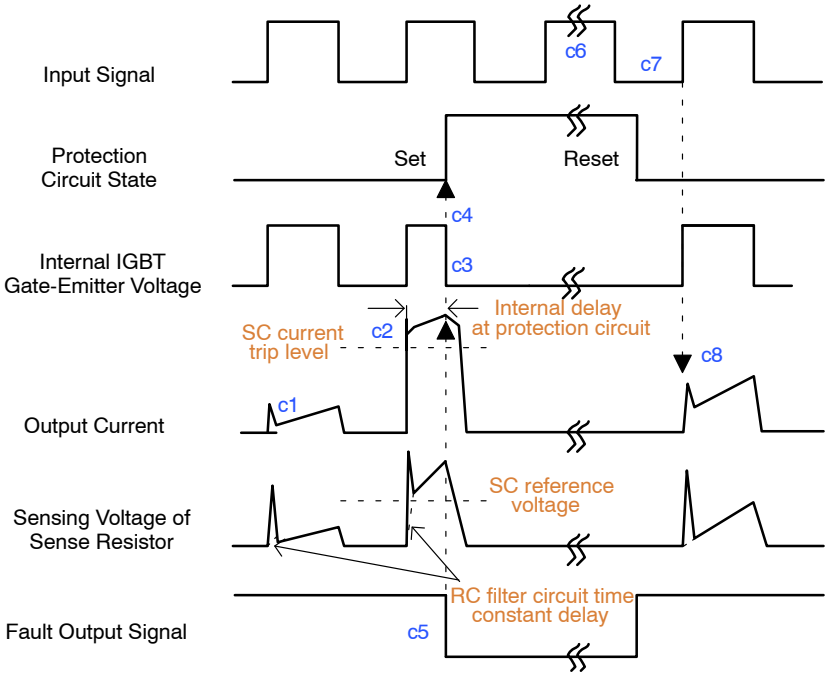


Figure 10. Short-Circuit Current Protection (Low-Side Operation Only)

(with the external sense resistance and RC filter connection)
c1: Normal operation: IGBT ON and carrying current.
c2: Short circuit current detection (SC trigger).
c3: All low-side IGBT's gate are hard interrupted.
c4: All low-side IGBT's turn OFF.
c5: Fault output operation starts with a fixed pulse width.
c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.
c8: Normal operation: IGBT ON and carrying current.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Min	Typ	Max	Unit
Comparative Tracking Index (CTI)			575			V
Device Flatness	See Figure 11		0		+150	μm
Mounting Torque	Mounting Screw: M3 See Figure 12	Recommended 0.7 N • m	0.6	0.7	0.8	N • m
		Recommended 7.1 kgf • cm	6.2	7.1	8.1	kgf • cm
Terminal Pulling Strength	Load 19.6 N		10			s
Terminal Bending Strength	Load 9.8 N, 90 deg. bend		2			times
Weight				15		g
Package Stray Inductance (Lσ)	P to NU, NV, NW (Note 9)			24		nH

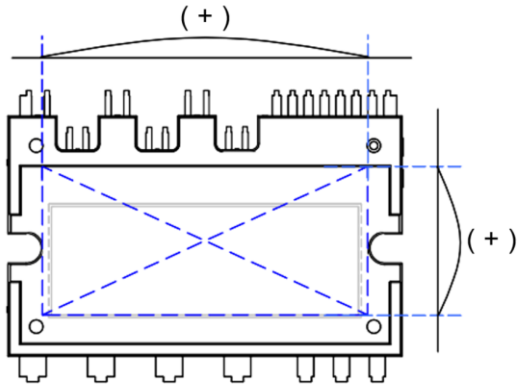


Figure 11. Flatness Measurement Position

MOUNTING SCREWS TORQUE ORDER

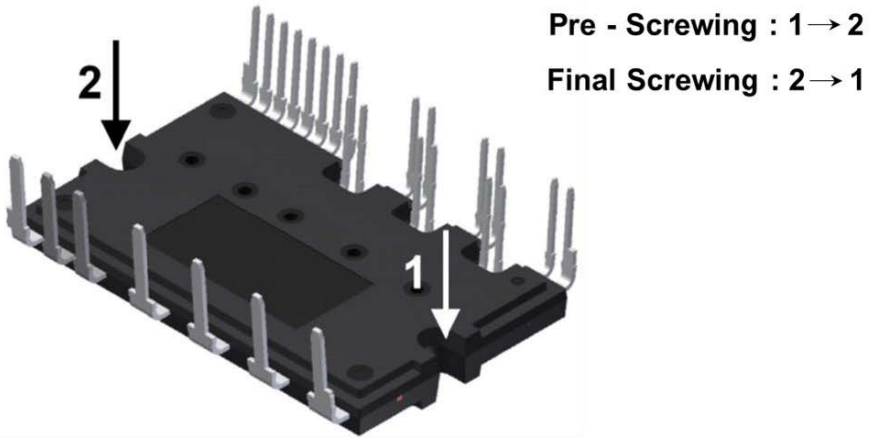


Figure 12. Screw Mounting Sequence

9. Stray Inductance per phase measured per IEC 60747-15.

TYPICAL APPLICATION CIRCUIT

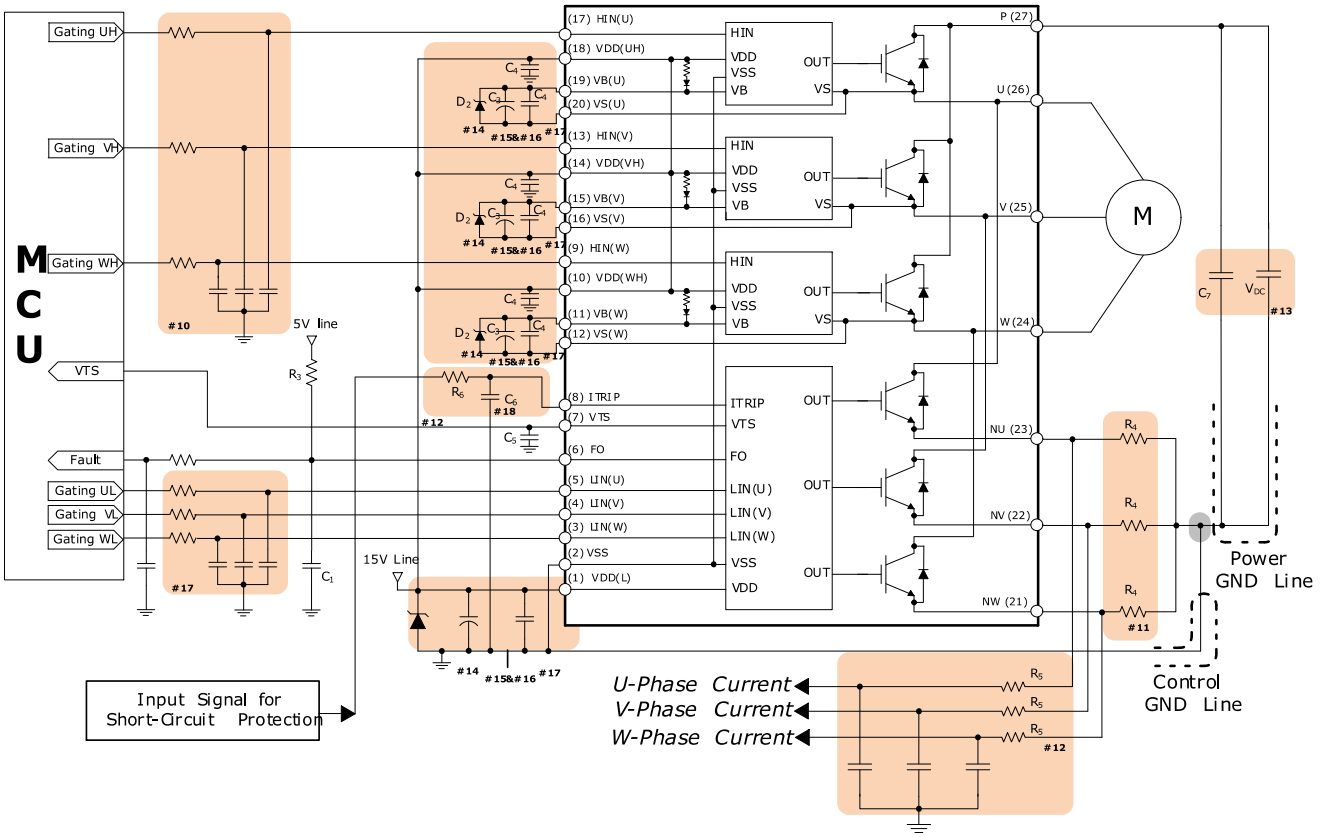


Figure 13. Typical Application Circuit

To avoid malfunction, the wiring of each input should be as short as possible (less than 2–3 cm). Each capacitor should be mounted as close to the pins of the product as possible. FO output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 2 mA.

NOTES:

10. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull down each signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50 ~ 150 ns. (Recommended R = 100 Ω, C = 1 nF)
11. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
12. In the short-circuit protection circuit, please select the RC time constant in the range 1.5 ~ 2 μs. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the RC time constant.
13. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
14. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended Zener diode is 22 V / 1 W, which has the lower Zener impedance characteristic than about 15 Ω).
15. The VDD electrolytic capacitor is recommended to be around 7 times larger than VBS electrolytic bootstrap capacitors.
16. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristics.
17. 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics are recommended.
18. To prevent protection function errors, the ITRIP capacitor should be placed as close to ITRIP and VSS pins as possible.

TYPICAL CHARACTERISTICS

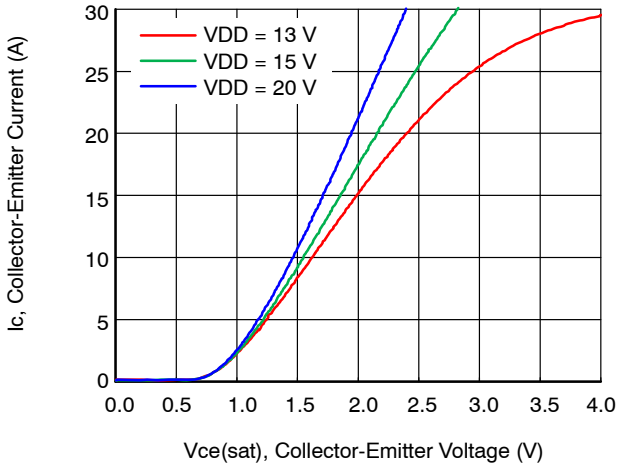


Figure 14. Collector-Emitter Saturation Voltage

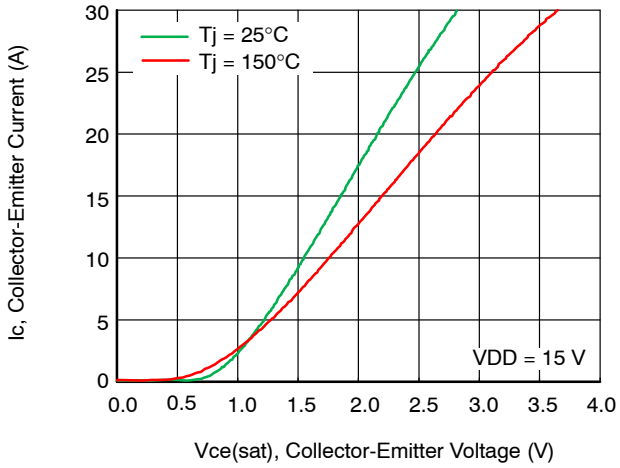


Figure 15. Collector-Emitter Saturation Voltage

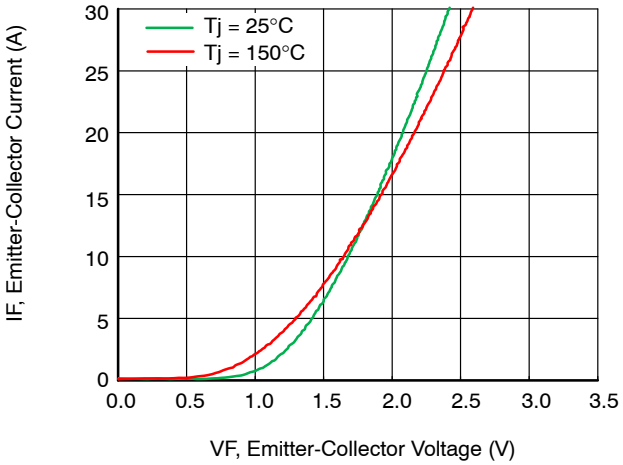


Figure 16. Emitter-Collector Forward Voltage

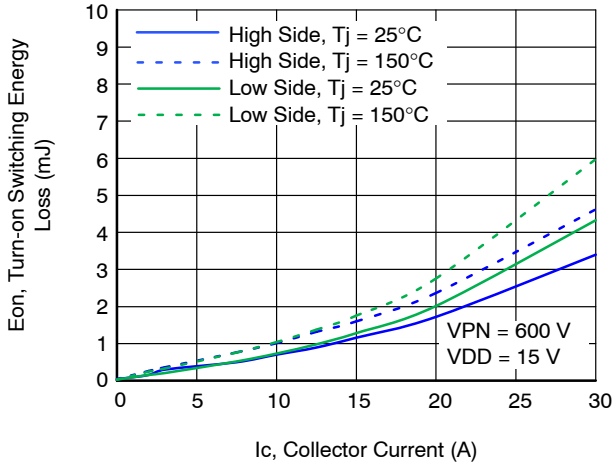


Figure 17. Turn-on Switching Energy Loss

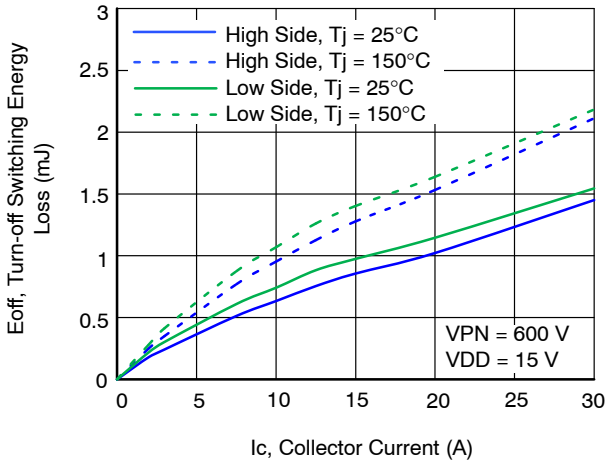


Figure 18. Turn-off Switching Energy Loss

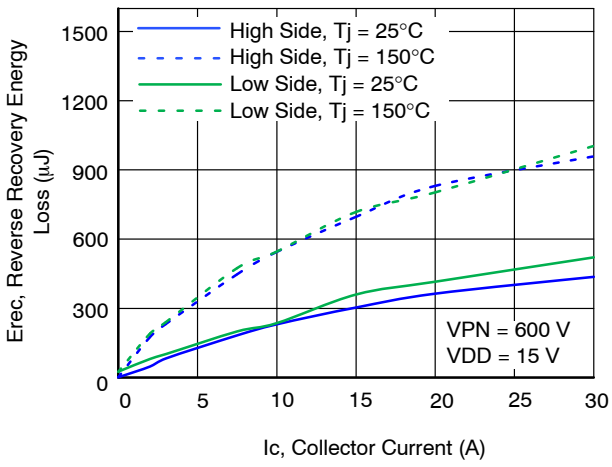


Figure 19. Reverse Recovery Energy Loss

TYPICAL CHARACTERISTICS

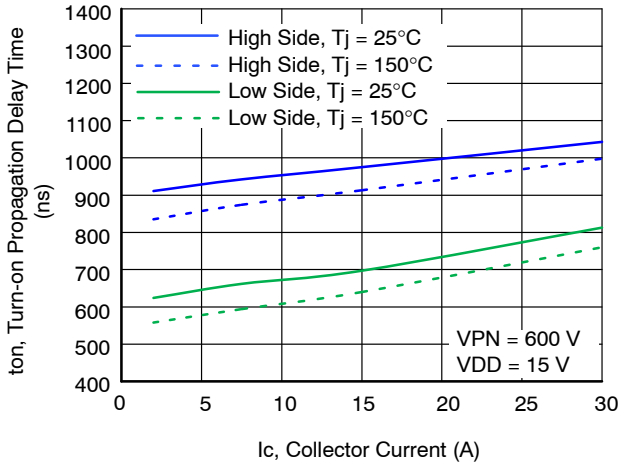


Figure 20. Turn-on Propagation Delay Time

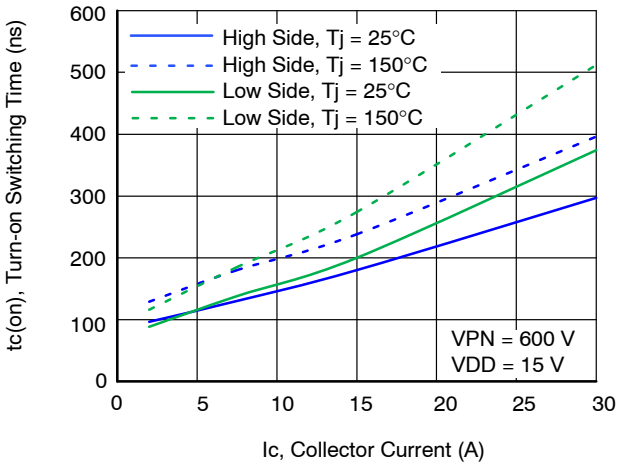


Figure 21. Turn-on Switching Time

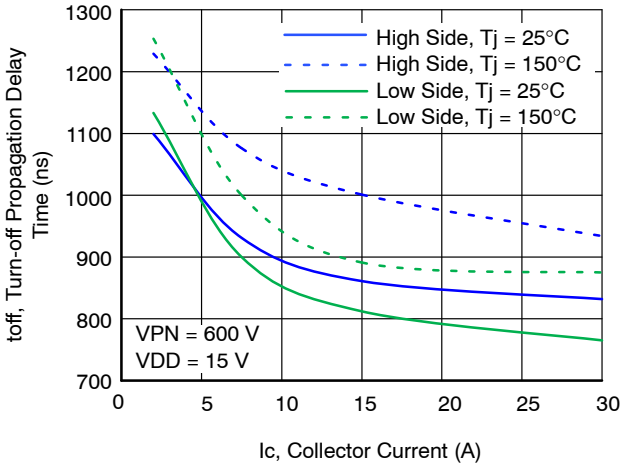


Figure 22. Typ. Turn-off Propagation Delay Time

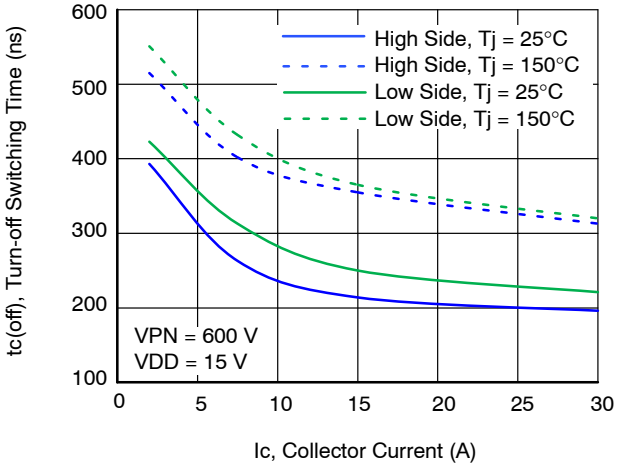


Figure 23. Typ. Turn-off Switching Time

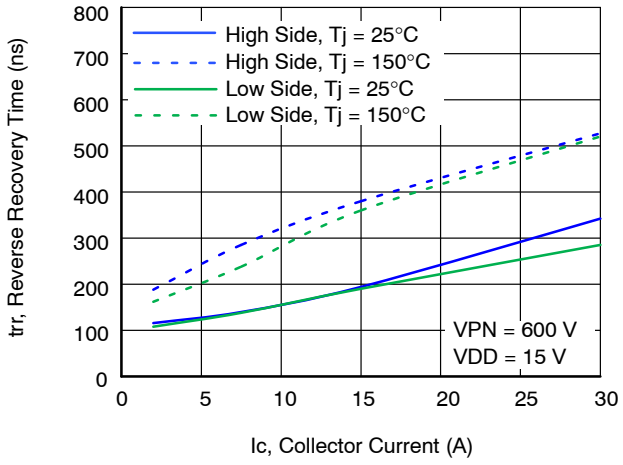


Figure 24. Typ. Reverse Recovery Time

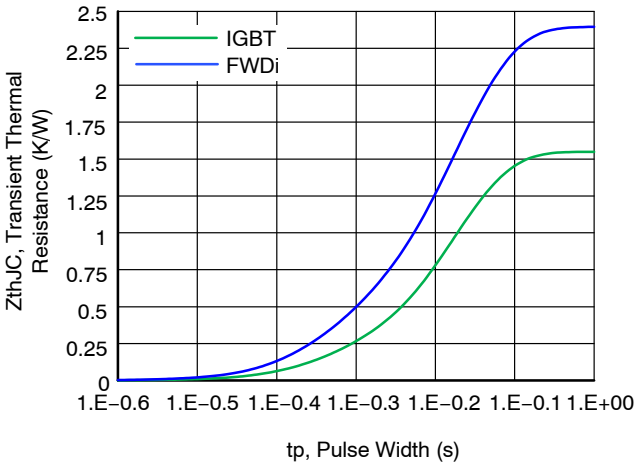


Figure 25. Transient Thermal Resistance

TURN-ON/OFF SWITCHING WAVEFORM

Switching conditions: V_{PN} = 600 V, V_{DD} = 15 V, T_J = 25 °C, I_C = 10 A

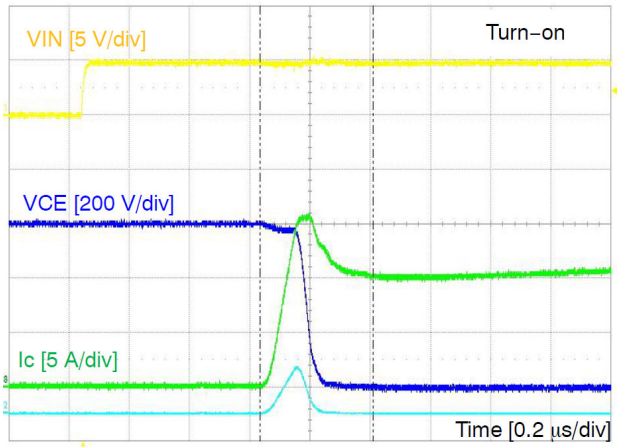


Figure 26. Turn-on Switching Waveform

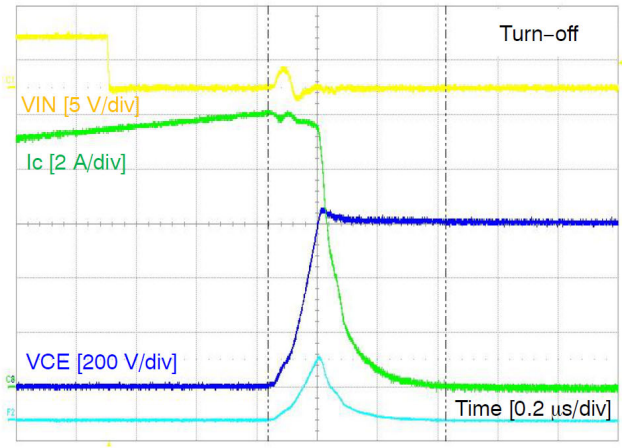


Figure 27. Turn-off Switching Waveform

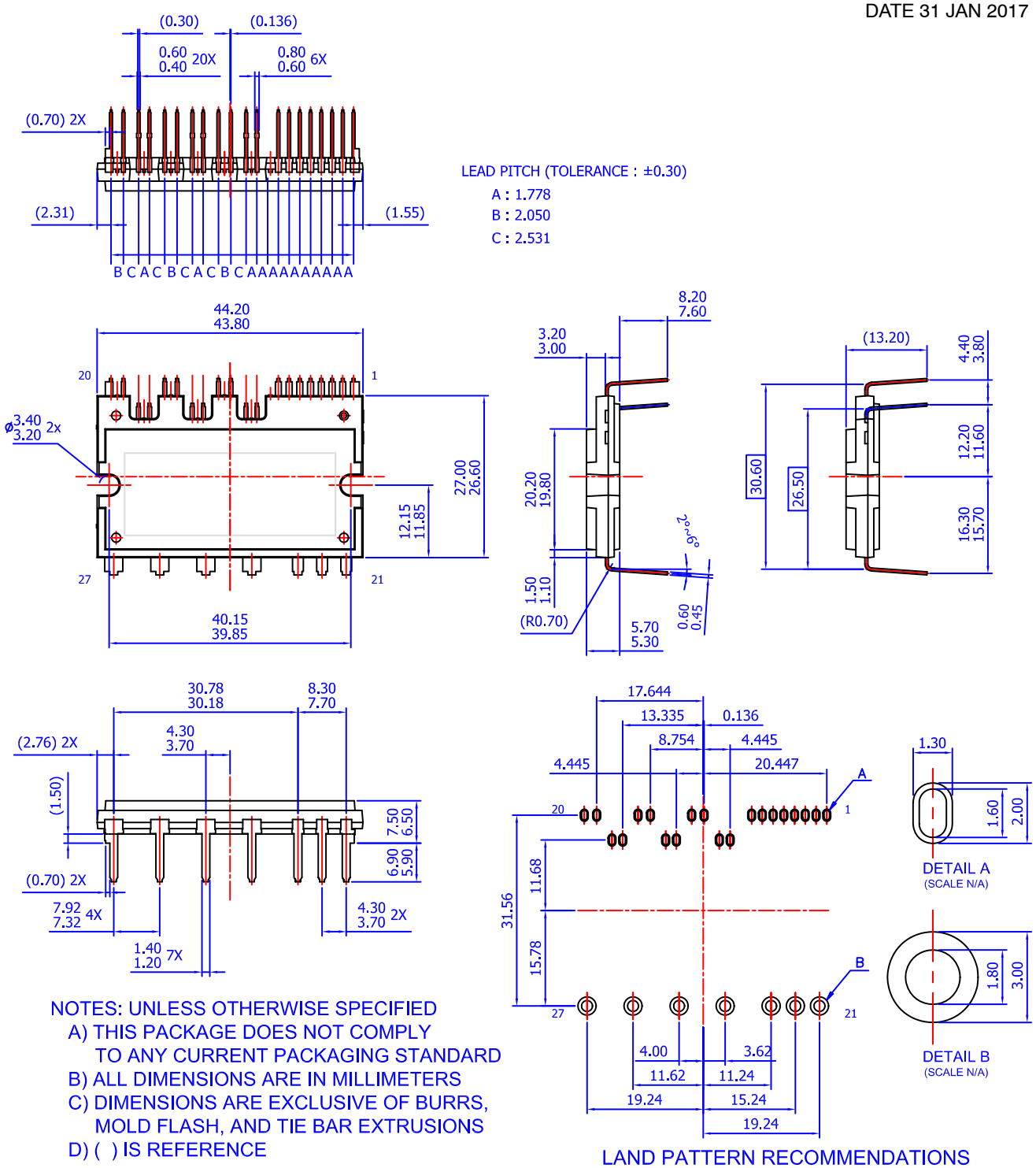
REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial preliminary document release.	9/9/2026

PACKAGE DIMENSIONS

SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE
CASE MODFJ
ISSUE O

DATE 31 JAN 2017



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

LAND PATTERN RECOMMENDATIONS

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