

# Field Effect Transistor - P-Channel, Logic Level, Enhancement Mode

## NDS332P

### General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- -1 A, -20 V
  - ♦  $R_{DS(on)} = 0.41 \Omega @ V_{GS} = -2.7 V$
  - ♦  $R_{DS(on)} = 0.3 \Omega @ V_{GS} = -4.5 V$
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits.  $V_{GS(th)} < 1.0 V$
- Proprietary Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- High Density Cell Design for Extremely Low  $R_{DS(on)}$
- Exceptional On-resistance and Maximum DC Current Capability
- Compact Industry Standard SOT-23 Surface Mount Package
- This Device is Pb-Free and Halide Free

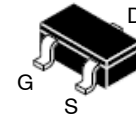
### MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter		Value	Unit
$V_{DSS}$	Drain-Source Voltage		-20	V
$V_{GSS}$	Gate-Source Voltage - Continuous		$\pm 8$	V
$I_D$	Drain Current	Continuous (Note 1a)	-1	A
		Pulsed	-10	
$P_D$	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

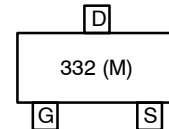
### THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ C/W$



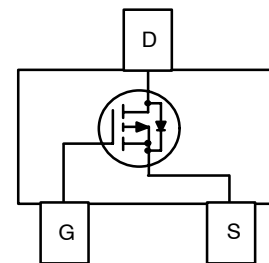
SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9  
CASE 527AG

### MARKING DIAGRAM



332 = Specific device Code  
M = Date Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
NDS332P	SOT-23-3/ SUPERSOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://BRD8011/D).

# NDS332P

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = –250 μA	–20	–	–	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = –16 V, V <sub>GS</sub> = 0 V	–	–	–1	μA
		V <sub>DS</sub> = –16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	–	–	–10	
I <sub>GSS</sub>	Gate–Body Leakage Current	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V	–	–	100	nA
I <sub>GSS</sub>	Gate–Body Leakage Current	V <sub>GS</sub> = –8 V, V <sub>DS</sub> = 0 V	–	–	–100	nA

## ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μA	–0.4	–0.6	–1	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μA, T <sub>J</sub> = 125°C	–0.3	–0.45	–0.8	
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = –2.7 V, I <sub>D</sub> = –1 A	–	0.35	0.41	Ω
		V <sub>GS</sub> = –2.7 V, I <sub>D</sub> = –1 A, T <sub>J</sub> = 125°C	–	0.5	0.74	
		V <sub>GS</sub> = –4.5 V, I <sub>D</sub> = –1.1 A	–	0.26	0.3	
I <sub>D(on)</sub>	On–State Drain Current	V <sub>GS</sub> = –2.7 V, V <sub>DS</sub> = –5 V	–1.5	–	–	A
		V <sub>GS</sub> = –4.5 V, V <sub>DS</sub> = –5 V	–2.5	–	–	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = –5 V, I <sub>D</sub> = –1 A	–	2.2	–	S

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = –10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	–	195	–	pF
C <sub>oss</sub>	Output Capacitance		–	105	–	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	40	–	pF

## SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn–On Delay Time	V <sub>DD</sub> = –6 V, I <sub>D</sub> = –1 A, V <sub>GS</sub> = –4.5 V, R <sub>GEN</sub> = 6 Ω	–	8	15	ns
t <sub>r</sub>	Turn–On Rise Time		–	30	45	ns
t <sub>d(off)</sub>	Turn–Off Delay Time		–	25	45	ns
t <sub>f</sub>	Turn–Off Fall Time		–	27	45	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = –5 V, I <sub>D</sub> = –1 A, V <sub>GS</sub> = –4.5 V	–	3.7	5	nC
Q <sub>gs</sub>	Gate–Source Charge		–	0.5	–	nC
Q <sub>gd</sub>	Gate–Drain Charge		–	0.9	–	nC

## DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Source Current		–	–	–0.42	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –0.42 A (Note 2)	–	–0.75	–1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R<sub>θJA</sub> is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5" x 5" FR–4 PCB in a still air environment:



a) 250°C/W when mounted on a 0.02 in² pad of 2oz copper.



b) 270°C/W when mounted on a 0.001 in² pad of 2oz copper.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

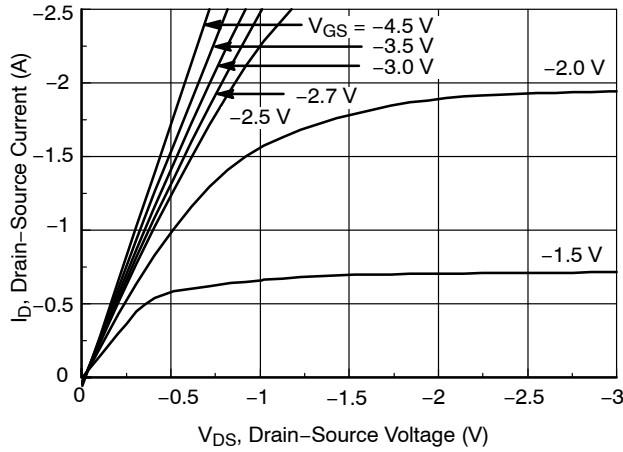


Figure 1. On-Region Characteristics

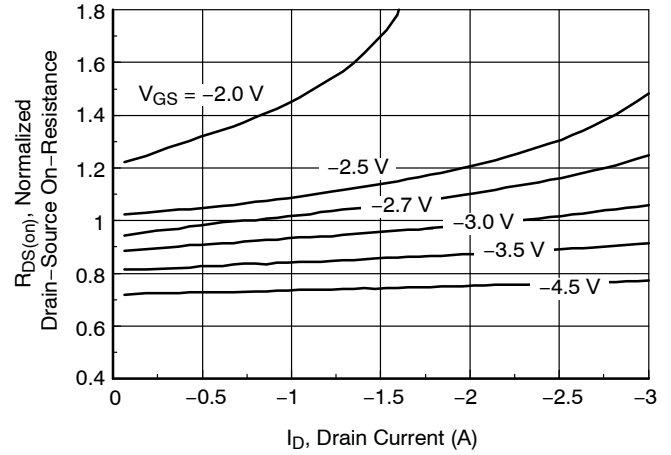


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

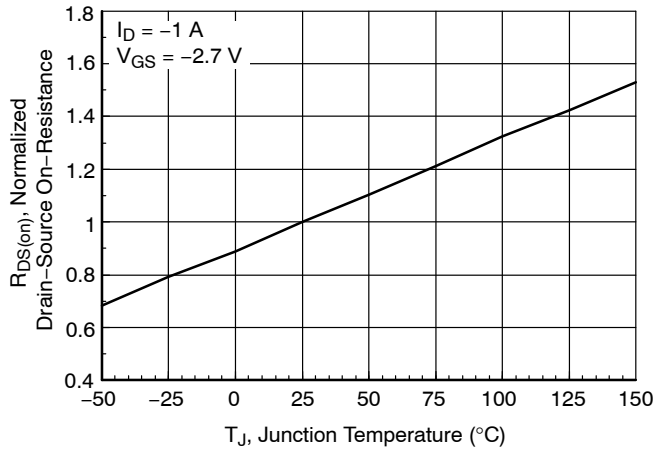


Figure 3. On-Resistance Variation with Temperature

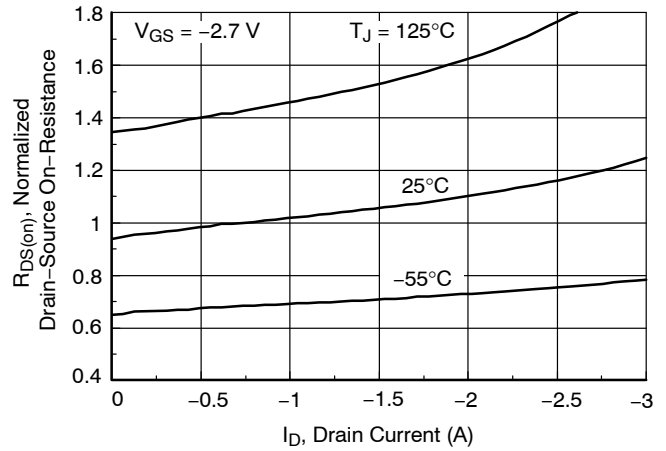


Figure 4. On-Resistance Variation with Drain Current and Temperature

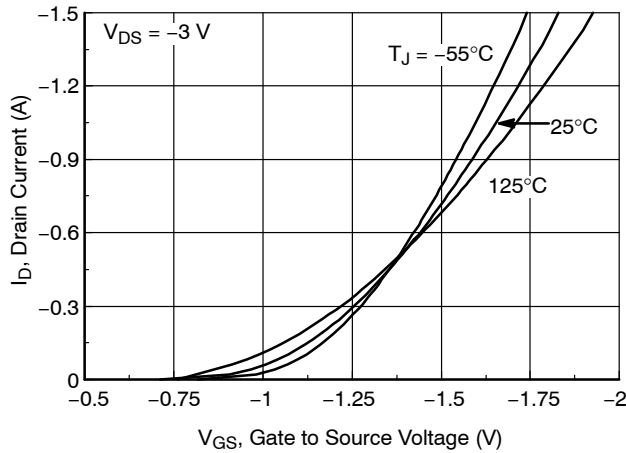


Figure 5. Transfer Characteristics

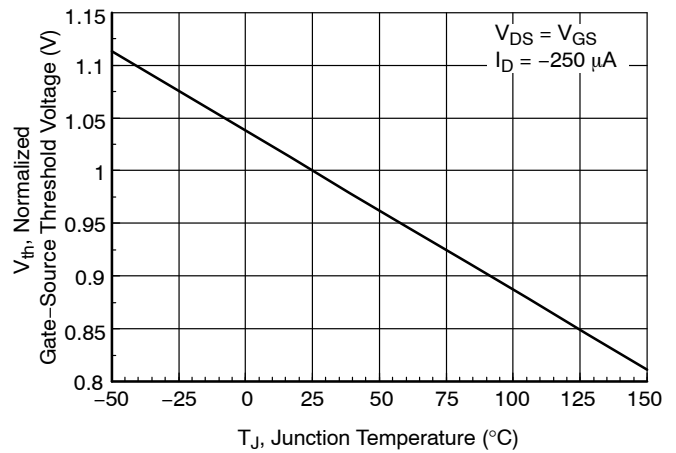


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

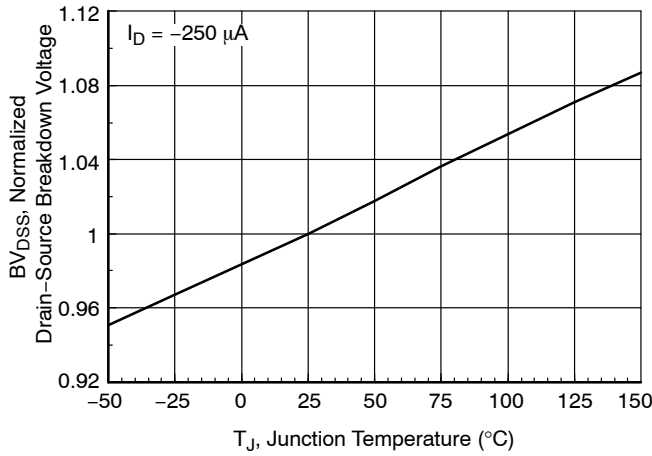


Figure 7. Breakdown Voltage Variation with Temperature

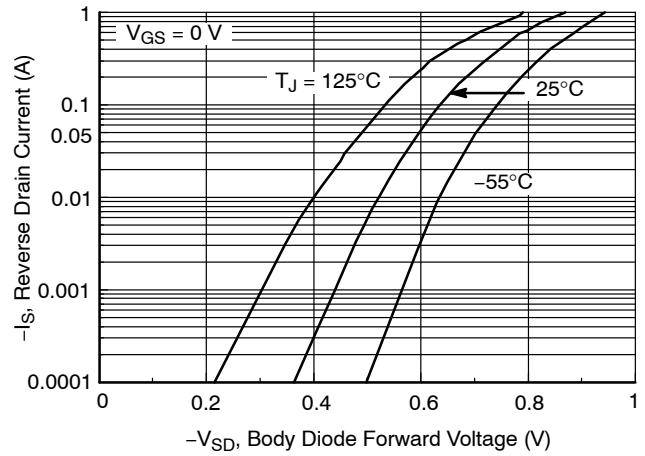


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

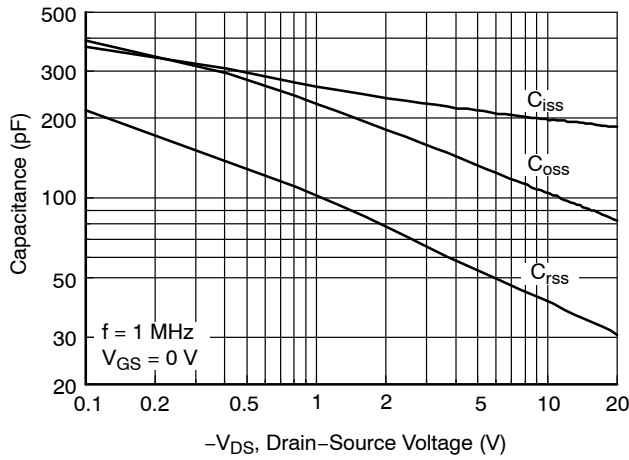


Figure 9. Capacitance Characteristics

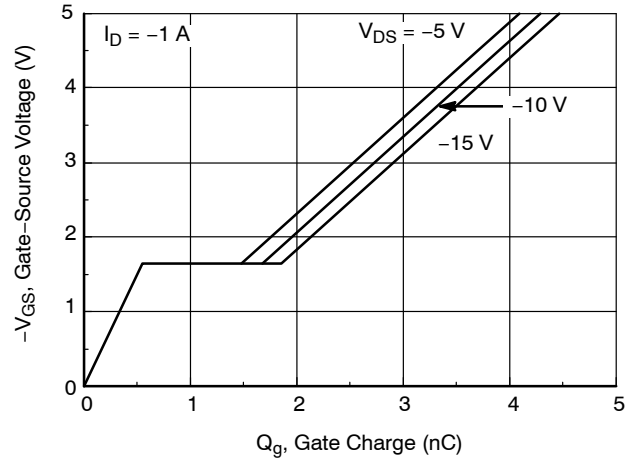


Figure 10. Gate Charge Characteristics

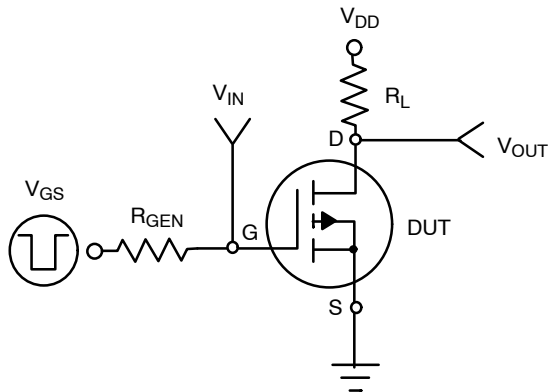


Figure 11. Switching Test Circuit

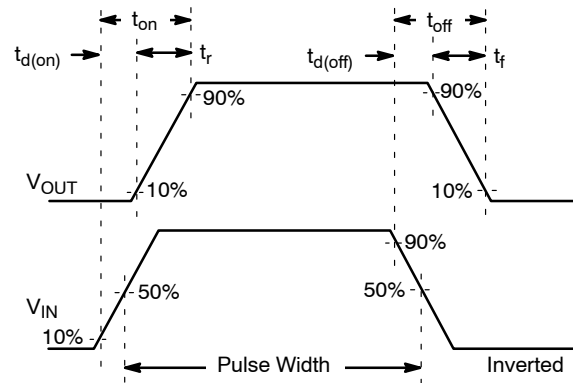


Figure 12. Switching Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

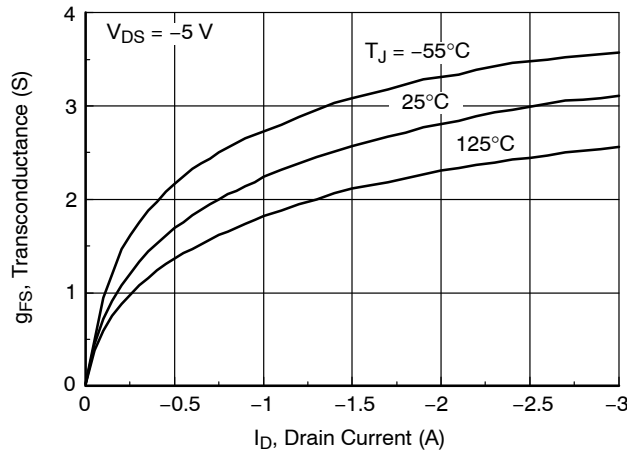


Figure 13. Transconductance Variation with Drain Current and Temperature

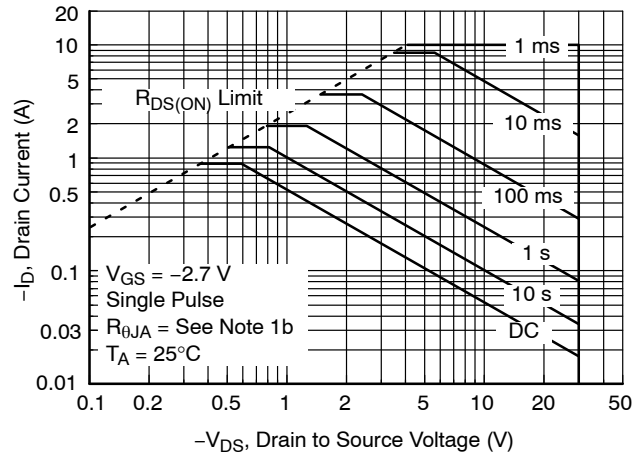


Figure 14. Maximum Safe Operating Area

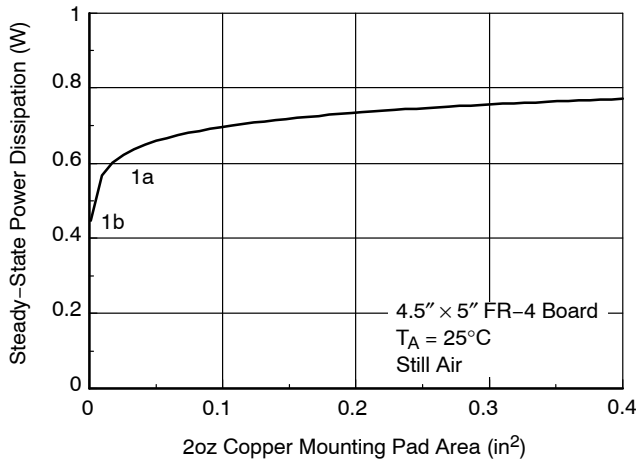


Figure 15. SUPERSOT™ -3 Maximum Steady-State Power Dissipation vs. Copper Mounting Pad Area

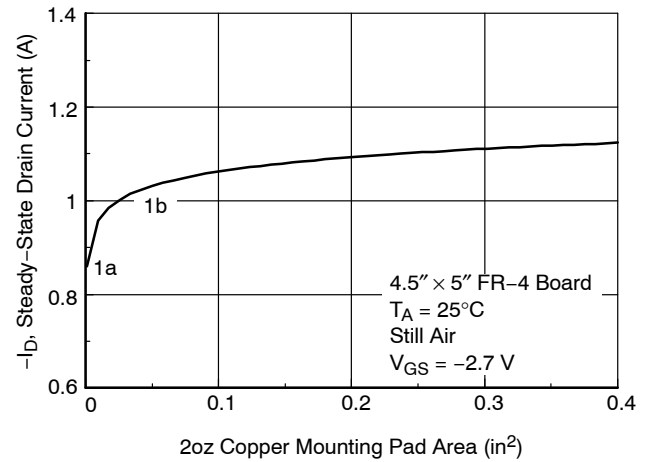


Figure 16. Maximum Steady-State Drain Current vs. Copper Mounting Pad Area

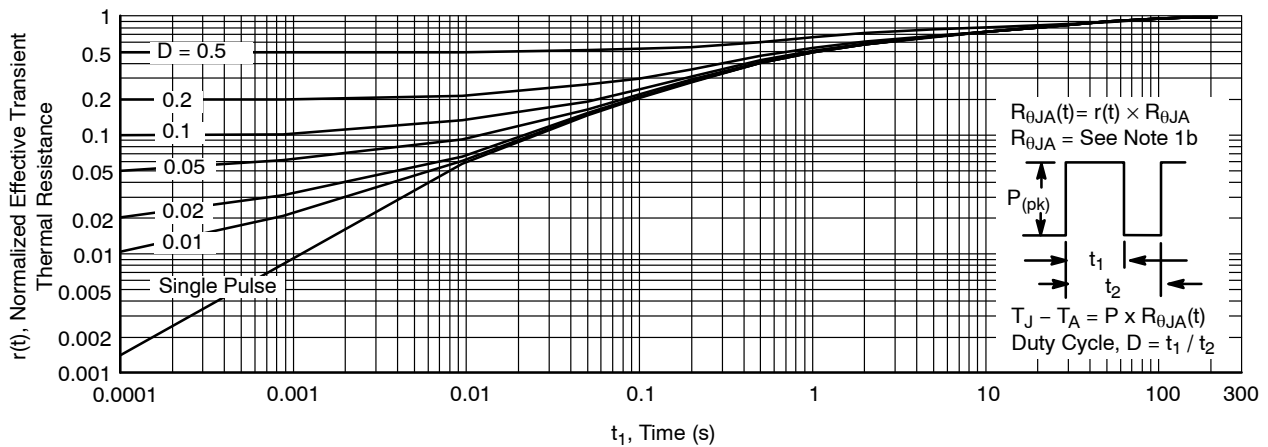
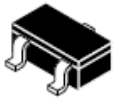


Figure 17. Transient Thermal Response Curve

Note: Characterization performed using the conditions described in note 1b.  
Transient thermal response will change depending on the circuit board design.

SUPERSOT is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.



### SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9

#### CASE 527AG

#### ISSUE A

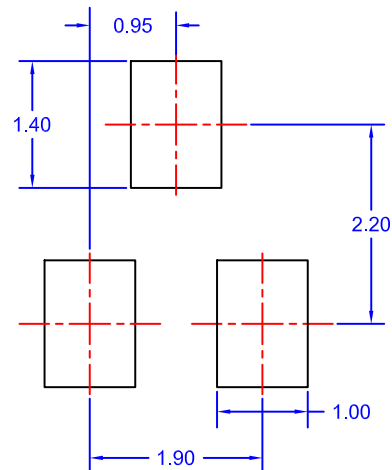
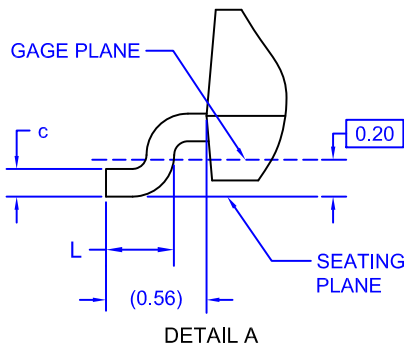
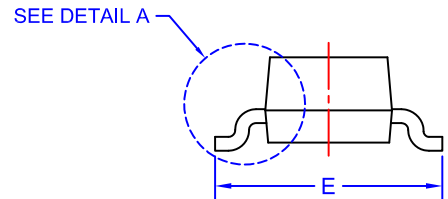
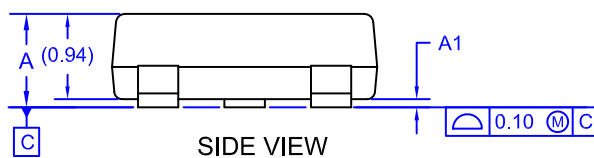
DATE 09 DEC 2019



NOTES: UNLESS OTHERWISE SPECIFIED

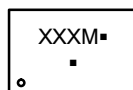
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43



\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Month Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON34319E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)