

# P-Channel Enhancement Mode Field Effect Transistor

## NDS0610

### General Description

This P-Channel Enhancement Mode Field Effect Transistors are Produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 120 mA DC and can deliver current up to 1 A.

This product is particularly suited to low voltage applications requiring a low current high side switch.

### Features

- -0.12 A, -60 V
  - ♦  $R_{DS(on)} = 10 \Omega$  @  $V_{GS} = -10 V$
  - ♦  $R_{DS(on)} = 20 \Omega$  @  $V_{GS} = -4.5 V$
- Voltage Controlled P-Channel Small Signal Switch
- High Density Cell design for Low  $R_{DS(on)}$
- High Saturation Current

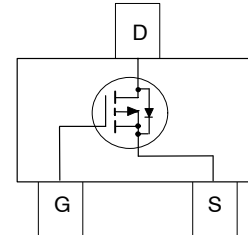
### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	-60	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1) - Pulsed	-0.12 -1	A
$P_D$	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above $25^\circ C$	2.9	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	$^\circ C$

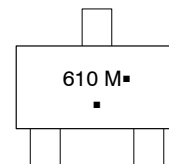
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOT-23  
CASE 318-08



### MARKING DIAGRAM



610 = Device Code  
M = Date Code\*  
■ = Pb-Free Package

(NOTE: Microdot may be in either location)

\*Date Code orientation and/or location may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NDS0610	SOT-23 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://BRD8011/D).

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	350	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS  $T_A = 25^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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## Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -10\text{ }\mu\text{A}$	-60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -10\text{ }\mu\text{A}$ , Referenced to $25^{\circ}\text{C}$	-	-53	-	$\text{mV}/^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$	-	-	-200	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 10$	nA

## On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -1\text{ mA}$	-1	-1.7	-3.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -1\text{ mA}$ , Referenced to $25^{\circ}\text{C}$	-	-3	-	$\text{mV}/^{\circ}\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.25\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}, T_J = 125^{\circ}\text{C}$	-	1.0 1.3 1.7	10 20 16	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -10\text{ V}$	-0.6	-	-	A
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -0.1\text{ A}$	70	430	-	mS

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	79	-	pF
$C_{oss}$	Output Capacitance		-	10	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	4	-	pF
$R_G$	Gate Resistance	$V_{DS} = -15\text{ mV}, f = 1.0\text{ MHz}$	-	10	-	$\Omega$

## Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -25\text{ V}, I_D = -0.12\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	-	2.5	5	ns
$t_r$	Turn-On Rise Time		-	6.3	12.6	ns
$t_{d(off)}$	Turn-Off Delay Time		-	10	15	ns
$t_f$	Turn-Off Fall Time		-	7.5	15	ns
$Q_g$	Total Gate Change	$V_{DS} = -48\text{ V}, I_D = -0.5\text{ A},$ $V_{GS} = -10\text{ V}$	-	1.8	2.5	nC
$Q_{gs}$	Gate-Source Change		-	0.3	-	nC
$Q_{gd}$	Gate-Drain Change		-	0.4	-	nC

## Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.24	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –0.24 A (Note 2)	–	–0.8	–1.5	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = –0.5 A, d <sub>iF</sub> /d <sub>t</sub> = 100 A/μs (Note 2)	–	17	–	ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge		–	15	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NOTES:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $350\text{ }^{\circ}\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

TYPICAL CHARACTERISTICS

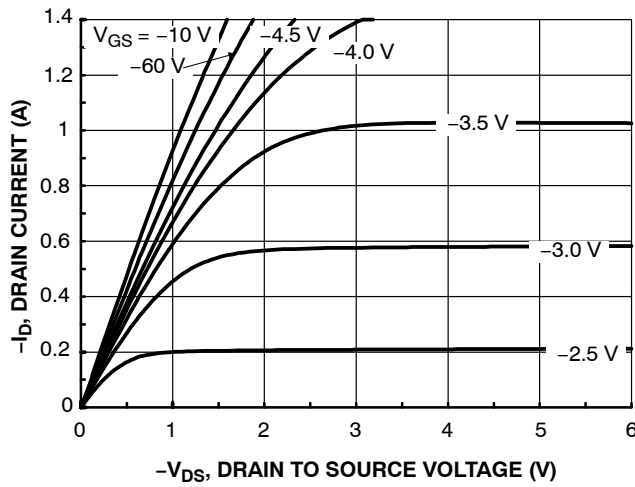


Figure 1. On-Region Characteristics

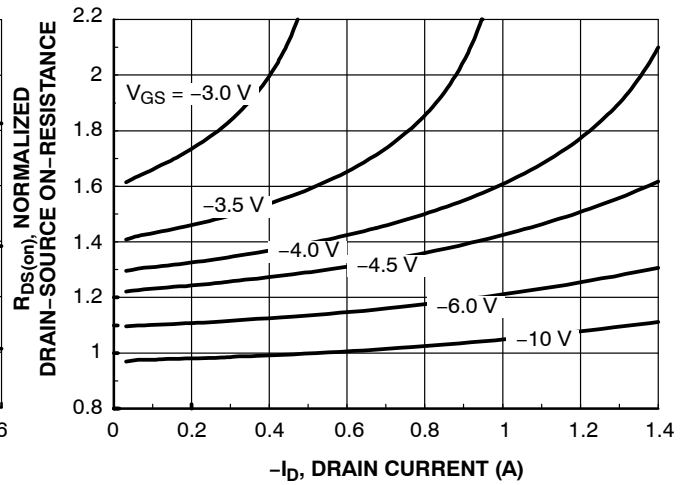


Figure 2. On-Resistance Variation With Drain Current and Gate Voltage

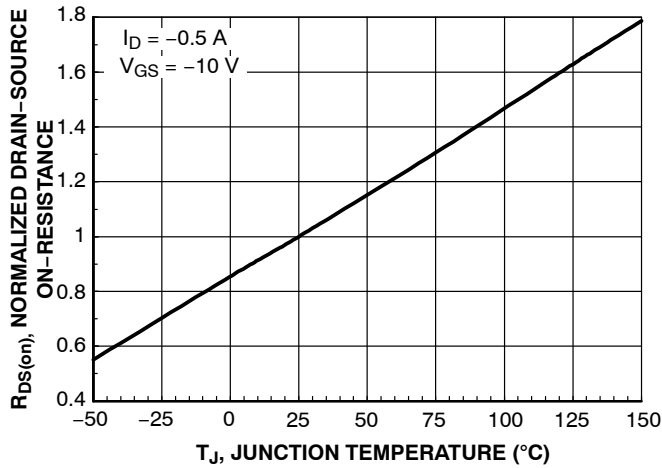


Figure 3. On-Resistance Variation with Temperature

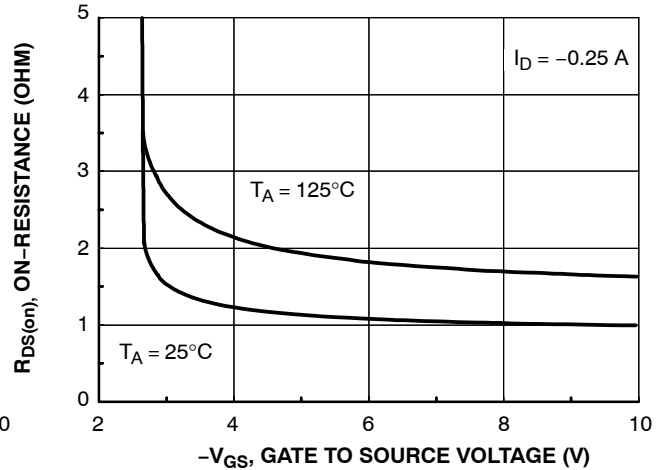


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

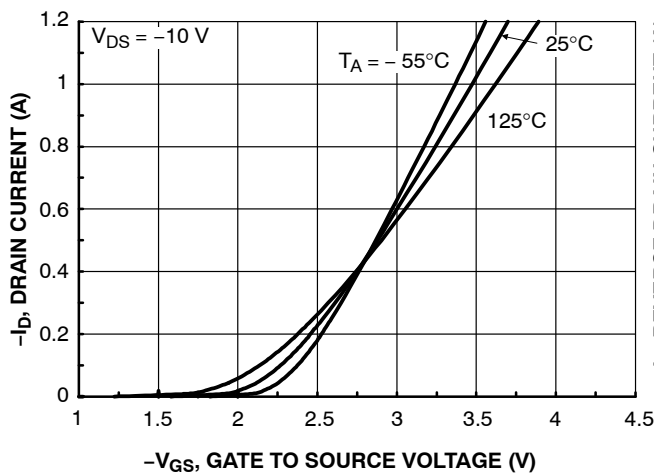


Figure 5. Transfer Characteristics

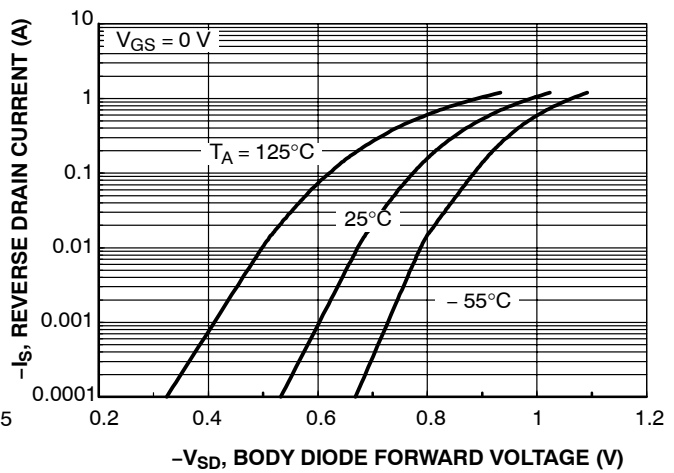


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

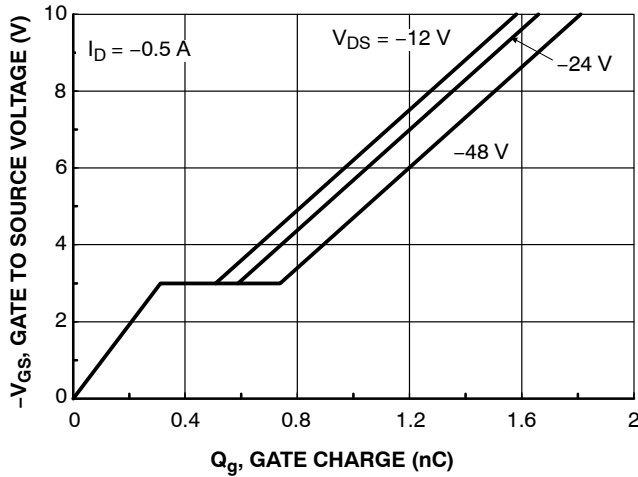


Figure 7. Gate Charge Characteristics

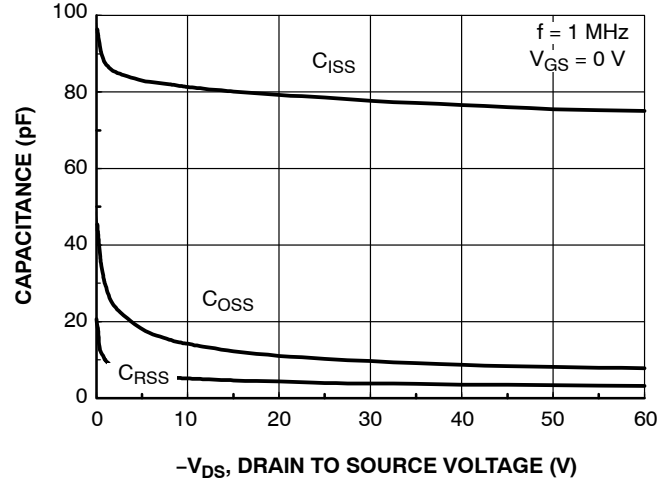


Figure 8. Capacitance Characteristics

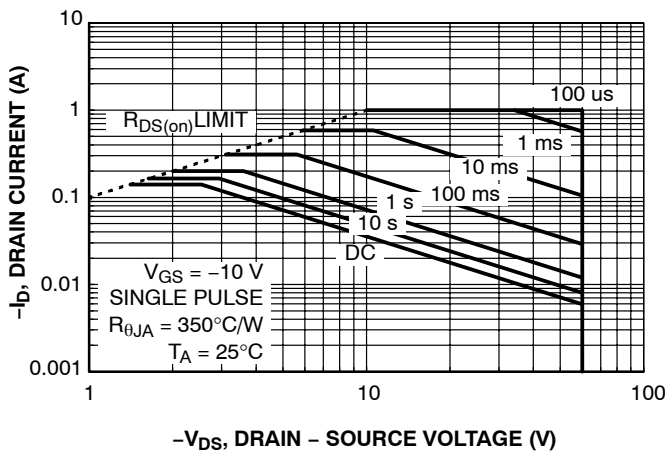


Figure 9. Maximum Safe Operating Area

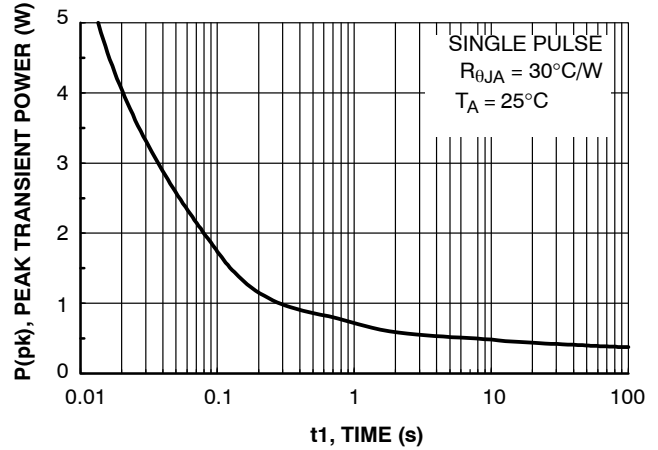


Figure 10. Single Pulse Maximum Power Dissipation

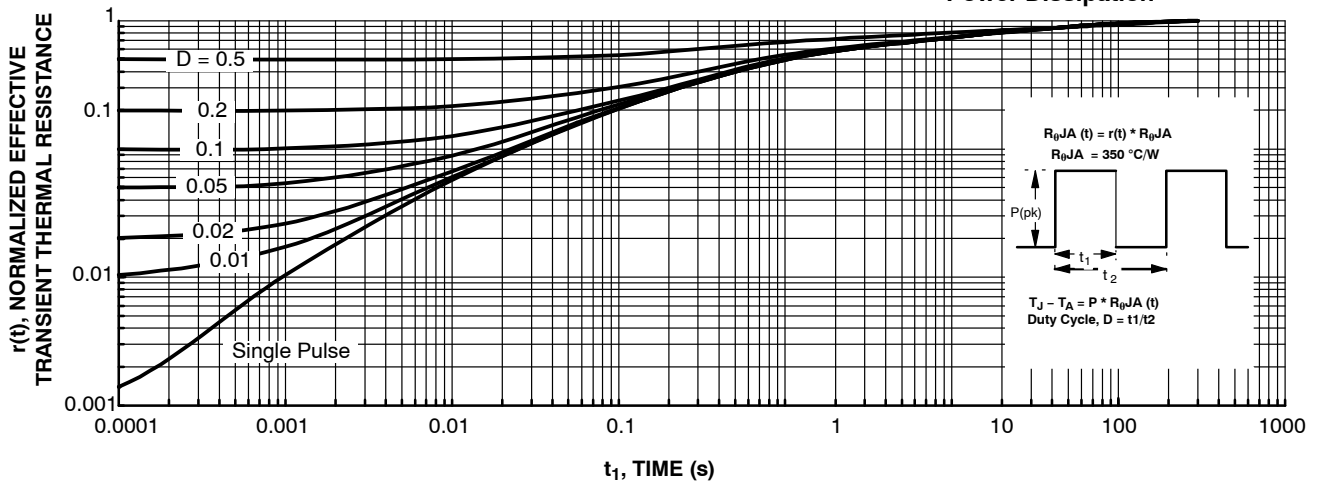


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a.  
Transient thermal response will change depending on the circuit board design.



SCALE 4:1

**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**  
CASE 318  
ISSUE AU

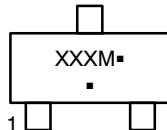
DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

**GENERIC MARKING DIAGRAM\***


XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.


**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**ISSUE AU**

DATE 14 AUG 2024

STYLE 1 THRU 5:  
CANCELLED

STYLE 6:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 7:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 8:  
PIN 1. ANODE  
2. NO CONNECTION  
3. CATHODE

STYLE 9:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 10:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE

STYLE 11:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 12:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 13:  
PIN 1. SOURCE  
2. DRAIN  
3. GATE

STYLE 14:  
PIN 1. CATHODE  
2. GATE  
3. ANODE

STYLE 15:  
PIN 1. GATE  
2. CATHODE  
3. ANODE

STYLE 16:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE

STYLE 17:  
PIN 1. NO CONNECTION  
2. ANODE  
3. CATHODE

STYLE 18:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. ANODE

STYLE 19:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE-ANODE

STYLE 20:  
PIN 1. CATHODE  
2. ANODE  
3. GATE

STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 22:  
PIN 1. RETURN  
2. OUTPUT  
3. INPUT

STYLE 23:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 24:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE

STYLE 25:  
PIN 1. ANODE  
2. CATHODE  
3. GATE

STYLE 26:  
PIN 1. CATHODE  
2. ANODE  
3. NO CONNECTION

STYLE 27:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

STYLE 28:  
PIN 1. ANODE  
2. ANODE  
3. ANODE

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