

# NDD60N745U1

## N-Channel Power MOSFET 600 V, 745 mΩ

### Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter  |                         |                             | Symbol         | Value       | Unit               |
|--|-------------------------|-----------------------------|----------------|-------------|--------------------|
| Drain-to-Source Voltage  |                         |                             | $V_{DSS}$      | 600         | V                  |
| Gate-to-Source Voltage   |                         |                             | $V_{GS}$       | $\pm 25$    | V                  |
| Continuous Drain Current $R_{\theta JC}$                               | Steady State            | $T_C = 25^{\circ}\text{C}$  | $I_D$          | 6.6         | A                  |
|  |                         | $T_C = 100^{\circ}\text{C}$ |                | 4.2         |                    |
| Power Dissipation – $R_{\theta JC}$                                    | Steady State            | $T_C = 25^{\circ}\text{C}$  | $P_D$          | 84          | W                  |
| Pulsed Drain Current   | $t_p = 10\ \mu\text{s}$ |                             | $I_{DM}$       | 27          | A                  |
| Operating Junction and Storage Temperature                             |                         |                             | $T_J, T_{STG}$ | -55 to +150 | $^{\circ}\text{C}$ |
| Source Current (Body Diode)  |                         |                             | $I_S$          | 6.6         | A                  |
| Single Pulse Drain-to-Source Avalanche Energy ( $I_D = 2.5\text{ A}$ ) |                         |                             | EAS            | 38          | mJ                 |
| Peak Diode Recovery (Note 1)   |                         |                             | $dv/dt$        | 15          | V/ns               |
| Lead Temperature for Soldering Leads                                   |                         |                             | $T_L$          | 260         | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $I_{SD} < 6.6 \text{ A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ,  $V_{DS \text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

### THERMAL RESISTANCE

| Parameter   | Symbol          | Value | Unit                      |
|---|-----------------|-------|---------------------------|
| Junction-to-Case (Drain) NDD60N745U1                  | $R_{\theta JC}$ | 1.5   | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient Steady State (Note 3) NDD60N745U1 | $R_{\theta JA}$ | 47    | $^\circ\text{C}/\text{W}$ |
| (Note 2) NDD60N745U1-1                                |                 | 98    |                           |
| (Note 2) NDD60N745U1-35                               |                 | 95    |                           |

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

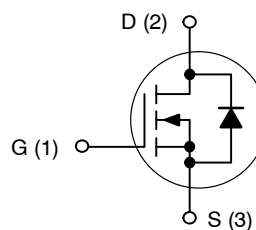


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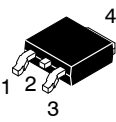
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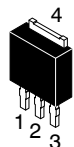
|               |                          |
|---------------|--------------------------|
| $V_{(BR)DSS}$ | $R_{DS(ON) \text{ MAX}}$ |
| 600 V         | 745 mΩ @ 10 V            |

### N-Channel MOSFET



  
IPAK  
CASE 369D  
STYLE 2

  
DPAK  
CASE 369C  
STYLE 2

  
IPAK  
CASE 369AD  
STYLE 2

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# NDD60N745U1

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------|--------|-----------------|-----|-----|-----|------|
|----------------|--------|-----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|   |                                      |  |                        |     |      |       |
|---|--------------------------------------|--|------------------------|-----|------|-------|
| Drain-to-Source Breakdown Voltage                         | V <sub>(BR)DSS</sub>                 | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA   | 600                    |     |      | V     |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V <sub>(BR)DSS</sub> /T <sub>J</sub> |  |                        | 540 |      | mV/°C |
| Drain-to-Source Leakage Current                           | I <sub>DSS</sub>                     | V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V | T <sub>J</sub> = 25°C  |     | 1    | μA    |
|   |                                      |  | T <sub>J</sub> = 125°C |     | 100  |       |
| Gate-to-Source Leakage Current                            | I <sub>GSS</sub>                     | V <sub>GS</sub> = ±20 V                        |                        |     | ±100 | nA    |

### ON CHARACTERISTICS (Note 4)

|  |                                     |   |   |     |     |       |
|--|-------------------------------------|---|---|-----|-----|-------|
| Gate Threshold Voltage                     | V <sub>GS(TH)</sub>                 | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA | 2 | 3.2 | 4   | V     |
| Negative Threshold Temperature Coefficient | V <sub>GS(TH)</sub> /T <sub>J</sub> | Reference to 25°C, I <sub>D</sub> = 250 μA                  |   | 7.6 |     | mV/°C |
| Static Drain-to-Source On Resistance       | R <sub>DS(on)</sub>                 | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.25 A             |   | 610 | 745 | mΩ    |
| Forward Transconductance                   | g <sub>FS</sub>                     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.25 A             |   | 5.6 |     | S     |

### DYNAMIC CHARACTERISTICS

|   |                    |  |  |     |  |    |
|---|--------------------|--|--|-----|--|----|
| Input Capacitance                                     | C <sub>iss</sub>   | V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz                       |  | 440 |  | pF |
| Output Capacitance                                    | C <sub>oss</sub>   |  |  | 27  |  |    |
| Reverse Transfer Capacitance                          | C <sub>rss</sub>   |  |  | 1.5 |  |    |
| Effective output capacitance, energy related (Note 6) | C <sub>o(er)</sub> | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V                            |  | 21  |  |    |
| Effective output capacitance, time related (Note 7)   | C <sub>o(tr)</sub> | I <sub>D</sub> = constant, V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V |  | 71  |  |    |
| Total Gate Charge                                     | Q <sub>g</sub>     | V <sub>DS</sub> = 300 V, I <sub>D</sub> = 6.8 A, V <sub>GS</sub> = 10 V        |  | 15  |  | nC |
| Gate-to-Source Charge                                 | Q <sub>gs</sub>    |  |  | 2.9 |  |    |
| Gate-to-Drain Charge                                  | Q <sub>gd</sub>    |  |  | 7.3 |  |    |
| Plateau Voltage                                       | V <sub>GP</sub>    |  |  | 5.3 |  | V  |
| Gate Resistance                                       | R <sub>g</sub>     |  |  | 4.4 |  | Ω  |

### RESISTIVE SWITCHING CHARACTERISTICS (Note 5)

|                     |                     |   |  |    |  |    |
|---------------------|---------------------|---|--|----|--|----|
| Turn-on Delay Time  | t <sub>d(on)</sub>  | V <sub>DD</sub> = 300 V, I <sub>D</sub> = 6.8 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω |  | 8  |  | ns |
| Rise Time           | t <sub>r</sub>      |   |  | 10 |  |    |
| Turn-off Delay Time | t <sub>d(off)</sub> |   |  | 19 |  |    |
| Fall Time           | t <sub>f</sub>      |   |  | 7  |  |    |

### SOURCE-DRAIN DIODE CHARACTERISTICS

|                         |                 |   |                        |     |      |     |    |
|-------------------------|-----------------|---|------------------------|-----|------|-----|----|
| Diode Forward Voltage   | V <sub>SD</sub> | I <sub>S</sub> = 6.6 A, V <sub>GS</sub> = 0 V   | T <sub>J</sub> = 25°C  |     | 0.90 | 1.6 | V  |
|                         |                 |   | T <sub>J</sub> = 100°C |     | 0.82 |     |    |
| Reverse Recovery Time   | t <sub>rr</sub> | V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V, I <sub>S</sub> = 6.8 A, dI/dt = 100 A/μs |                        | 260 |      |     | ns |
| Charge Time             | t <sub>a</sub>  |   |                        | 130 |      |     |    |
| Discharge Time          | t <sub>b</sub>  |   |                        | 130 |      |     |    |
| Reverse Recovery Charge | Q <sub>rr</sub> |   |                        | 2.1 |      |     |    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

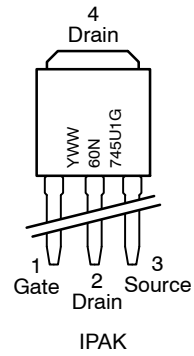
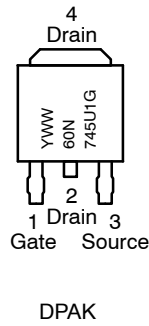
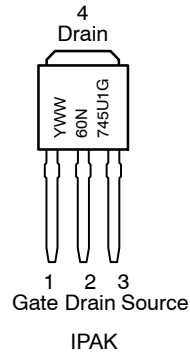
5. Switching characteristics are independent of operating junction temperatures.

6. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

7. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

# NDD60N745U1

## MARKING DIAGRAMS



Y = Year  
WW = Work Week  
G = Pb-Free Package

## ORDERING INFORMATION

| Device          | Package                         | Shipping <sup>†</sup> |
|-----------------|---------------------------------|-----------------------|
| NDD60N745U1-1G  | IPAK<br>(Pb-Free, Halogen-Free) | 75 Units / Rail       |
| NDD60N745U1-35G | IPAK<br>(Pb-Free, Halogen-Free) | 75 Units / Rail       |
| NDD60N745U1T4G  | DPAK<br>(Pb-Free, Halogen-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

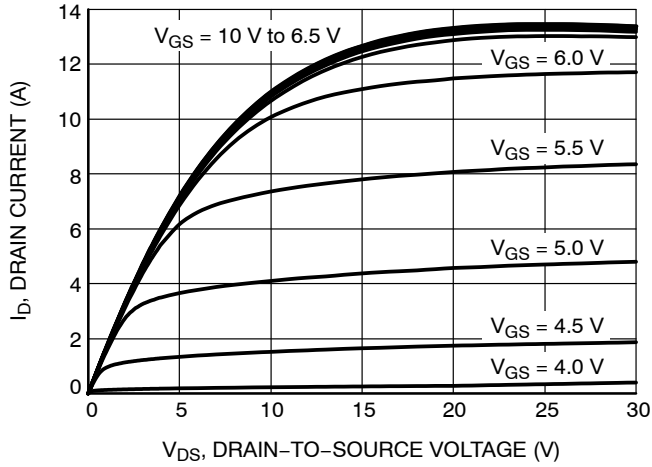


Figure 1. On-Region Characteristics

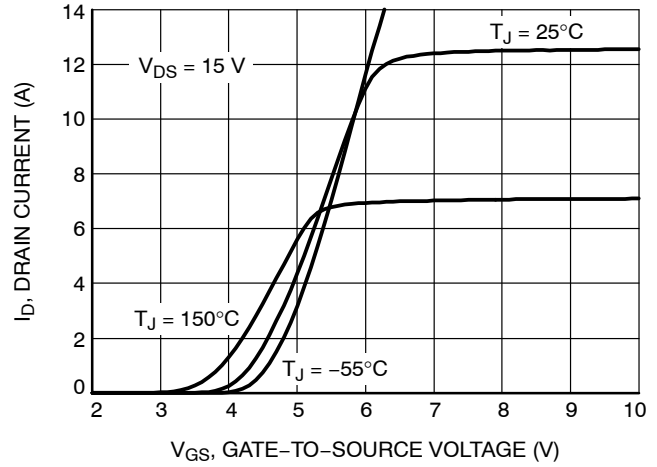


Figure 2. Transfer Characteristics

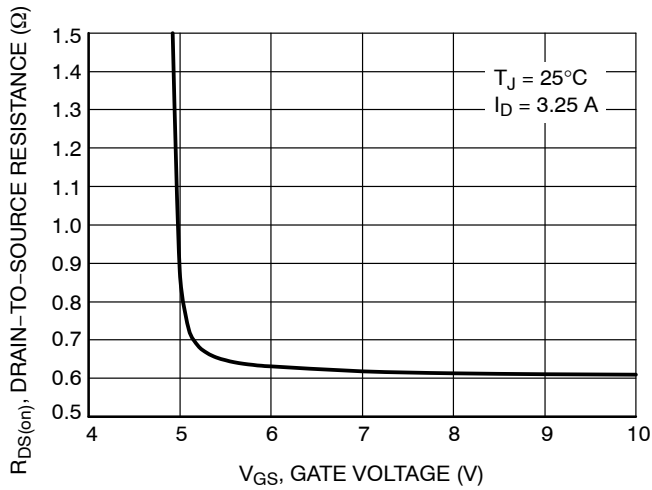


Figure 3. On-Resistance vs. Gate-to-Source Voltage

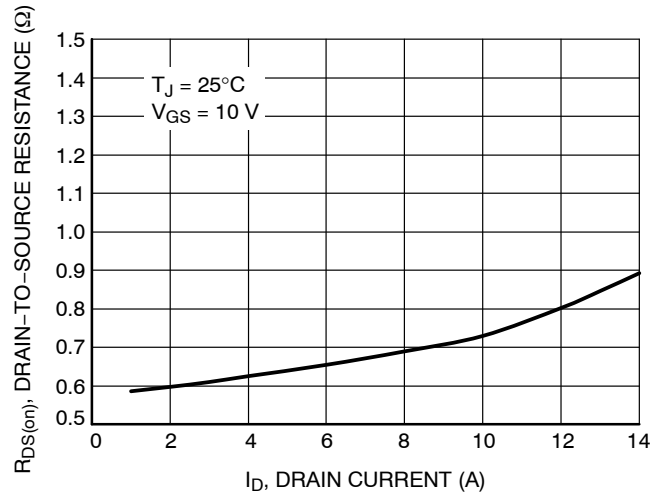


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

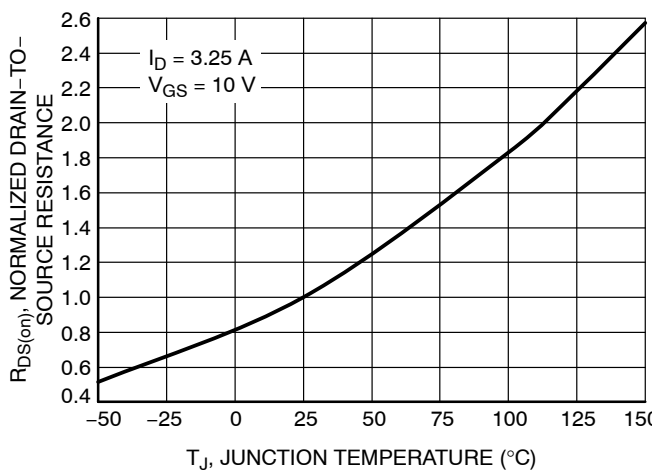


Figure 5. On-Resistance Variation with Temperature

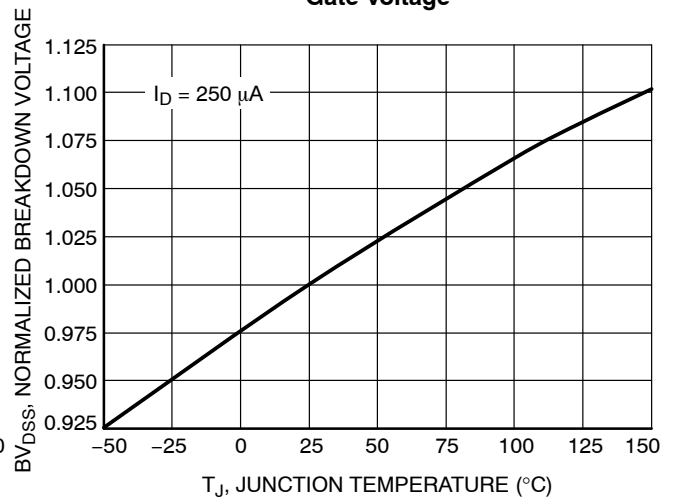


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

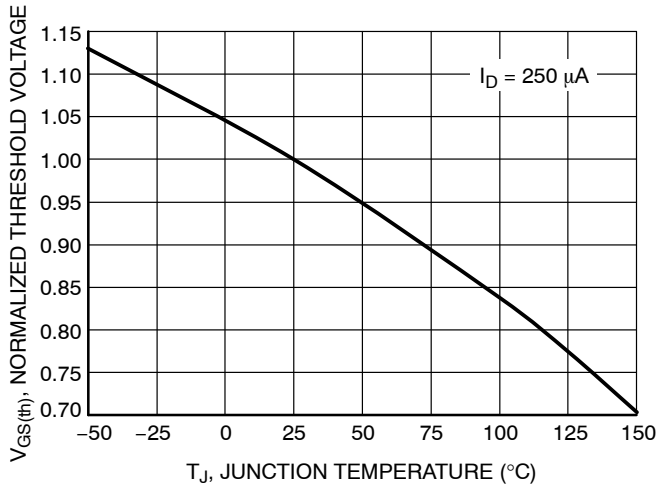


Figure 7. Threshold Voltage Variation with Temperature

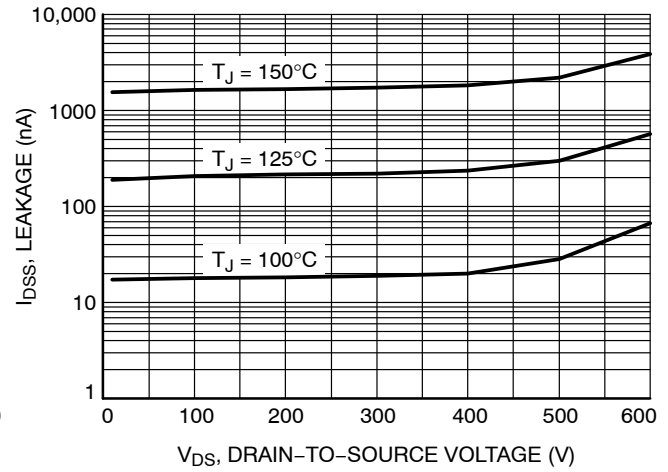


Figure 8. Drain-to-Source Leakage Current vs. Voltage

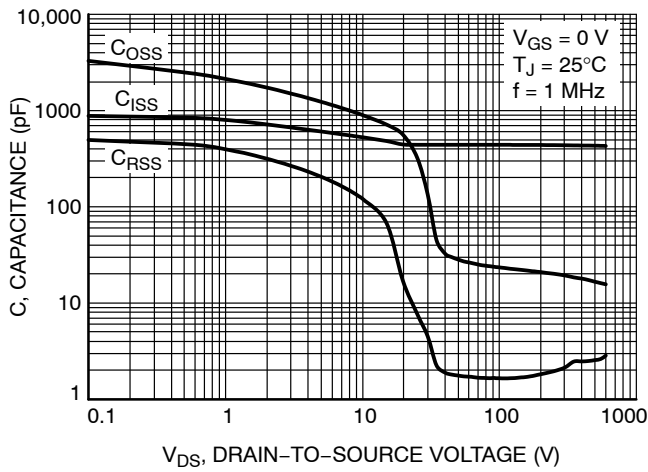


Figure 9. Capacitance Variation

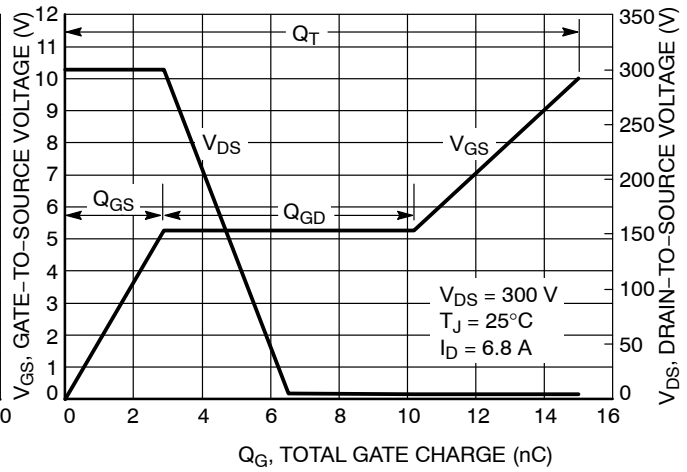


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

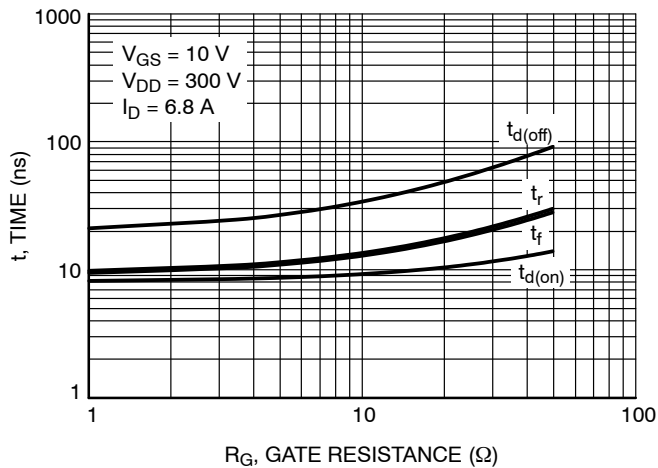


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

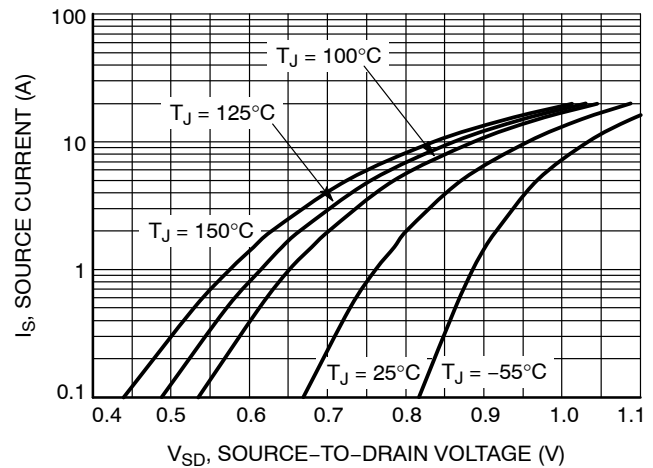


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

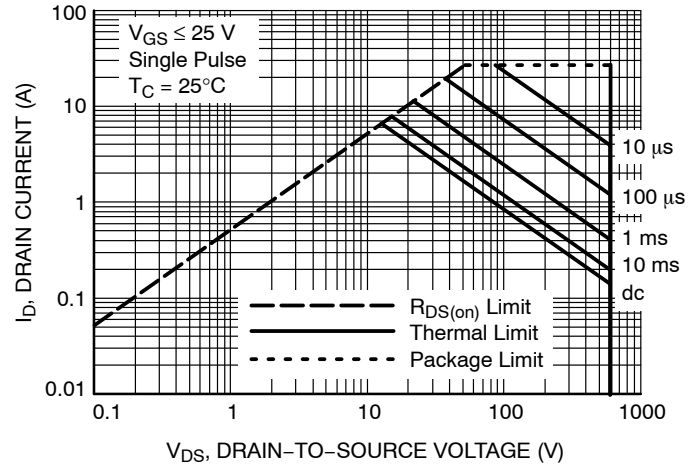


Figure 13. Maximum Rated Forward Biased Safe Operating Area

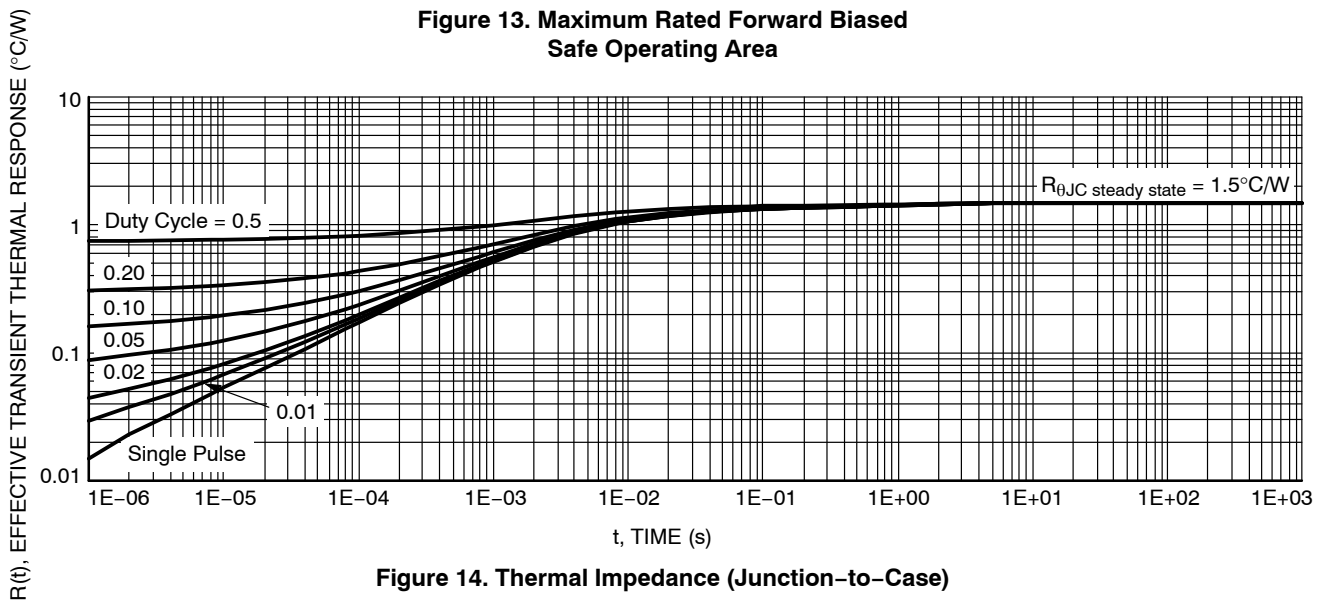
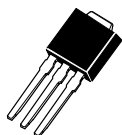


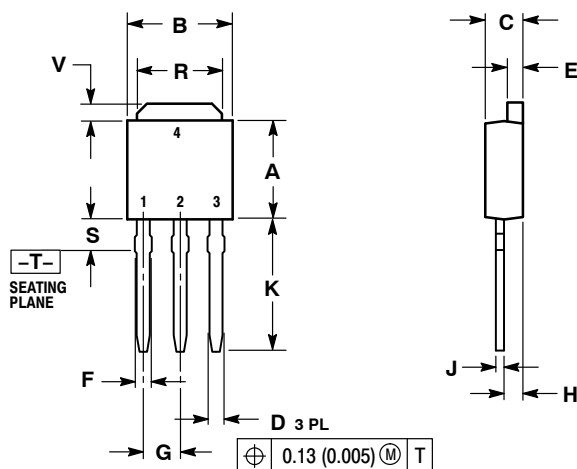
Figure 14. Thermal Impedance (Junction-to-Case)



DPAK INSERTION MOUNT  
CASE 369  
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.235     | 0.250 | 5.97        | 6.35 |
| B   | 0.250     | 0.265 | 6.35        | 6.73 |
| C   | 0.086     | 0.094 | 2.19        | 2.38 |
| D   | 0.027     | 0.035 | 0.69        | 0.88 |
| E   | 0.033     | 0.040 | 0.84        | 1.01 |
| F   | 0.037     | 0.047 | 0.94        | 1.19 |
| G   | 0.090 BSC |       | 2.29 BSC    |      |
| H   | 0.034     | 0.040 | 0.87        | 1.01 |
| J   | 0.018     | 0.023 | 0.46        | 0.58 |
| K   | 0.350     | 0.380 | 8.89        | 9.65 |
| R   | 0.175     | 0.215 | 4.45        | 5.46 |
| S   | 0.050     | 0.090 | 1.27        | 2.28 |
| V   | 0.030     | 0.050 | 0.77        | 1.27 |

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

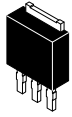
STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2

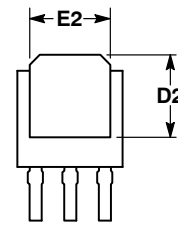
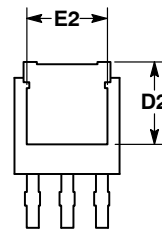
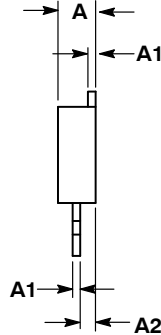
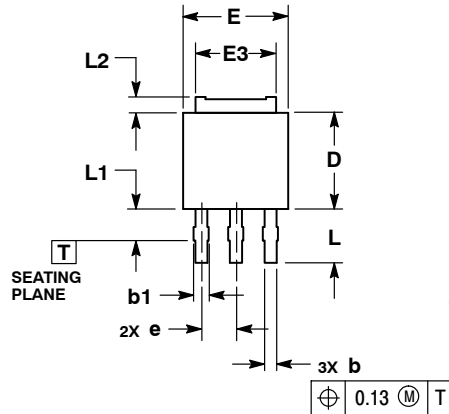
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| DESCRIPTION:     | DPAK INSERTION MOUNT | PAGE 1 OF 1   |

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**3.5 MM IPAK, STRAIGHT LEAD**  
**CASE 369AD**  
**ISSUE B**

DATE 18 APR 2013

SCALE 1:1


**OPTIONAL  
CONSTRUCTION**
**NOTES:**

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 2.19     | 2.38 |
| A1          | 0.46     | 0.60 |
| A2          | 0.87     | 1.10 |
| b           | 0.69     | 0.89 |
| b1          | 0.77     | 1.10 |
| D           | 5.97     | 6.22 |
| D2          | 4.80     | ---  |
| E           | 6.35     | 6.73 |
| E2          | 4.57     | 5.45 |
| E3          | 4.45     | 5.46 |
| e           | 2.28 BSC |      |
| L           | 3.40     | 3.60 |
| L1          | ---      | 2.10 |
| L2          | 0.89     | 1.27 |

**GENERIC MARKING  
DIAGRAMS\***
**STYLE 1:**  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

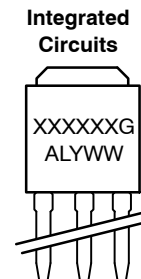
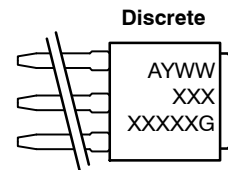
**STYLE 2:**  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

**STYLE 3:**  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

**STYLE 4:**  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

**STYLE 5:**  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE

**STYLE 6:**  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2

**STYLE 7:**  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**DOCUMENT NUMBER:** 98AON23319D

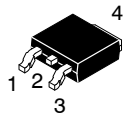
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**DESCRIPTION:** 3.5 MM IPAK, STRAIGHT LEAD

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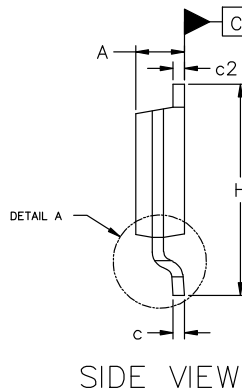
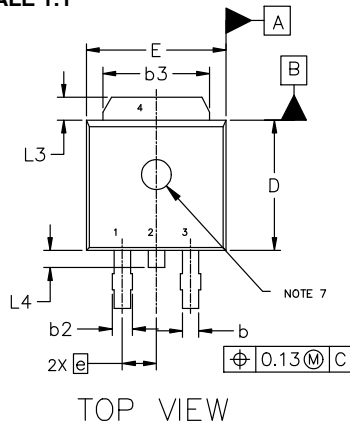




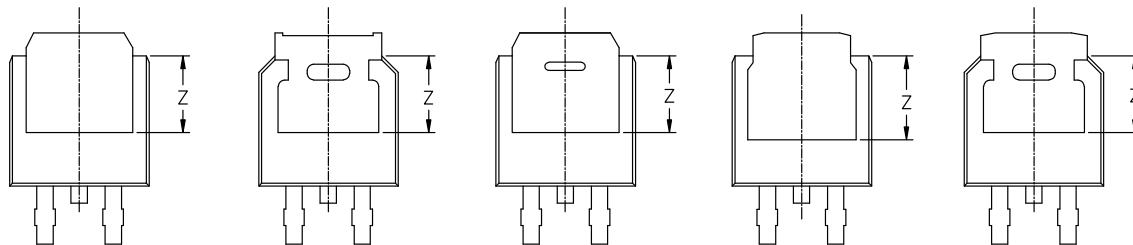
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CASE 369C  
ISSUE J

DATE 12 AUG 2025

SCALE 1:1

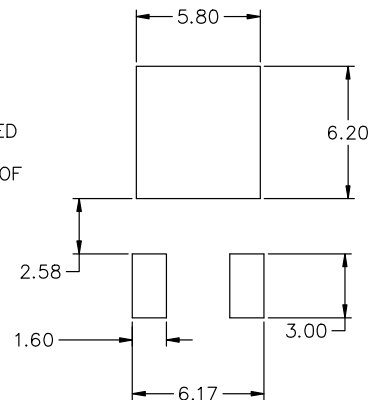
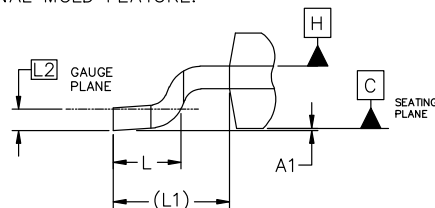


| MILLIMETERS |          |      |       |
|-------------|----------|------|-------|
| DIM         | MIN      | NOM  | MAX   |
| A           | 2.18     | 2.28 | 2.38  |
| A1          | 0.00     | ---  | 0.13  |
| b           | 0.63     | 0.76 | 0.89  |
| b2          | 0.72     | 0.93 | 1.14  |
| b3          | 4.57     | 5.02 | 5.46  |
| c           | 0.46     | 0.54 | 0.61  |
| c2          | 0.46     | 0.54 | 0.61  |
| D           | 5.97     | 6.10 | 6.22  |
| E           | 6.35     | 6.54 | 6.73  |
| e           | 2.29 BSC |      |       |
| H           | 9.40     | 9.91 | 10.41 |
| L           | 1.40     | 1.59 | 1.78  |
| L1          | 2.90 REF |      |       |
| L2          | 0.51 BSC |      |       |
| L3          | 0.89     | ---  | 1.27  |
| L4          | ---      | ---  | 1.01  |
| Z           | 3.93     | ---  | ---   |



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

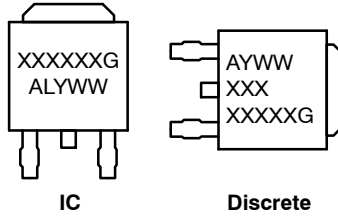
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| DESCRIPTION:     | DPAK3 6.10x6.54x2.28, 2.29P | PAGE 1 OF 2  |

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DPAK3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|   |   |  |  |   |
|---|---|--|--|---|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | STYLE 5:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| STYLE 6:<br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | STYLE 7:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 8:<br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |

|                  |                             |   |
|------------------|-----------------------------|---|
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