High Voltage Linear Regulator

85 V, 100 mA

Preliminary Document

NCV8740

The NCV8740 is a high-voltage tolerant linear regulator that offers the benefits of thermally enhanced MSOP8 EP and DFNW8 3x3 (on request) packages and is able to withstand continuous DC or transient input voltages up to 85 V with Ultra-low Quiescent Current below 5 μA. The device is stable with small 1 μF Ceramic Output Capacitors which allows smaller PCB design. The devices features enable pin compatible with standard CMOS logic, internal power good circuit with a user programmable delay via external capacitor. The active high output of power good has open drain with internal current limitation.

Features

- Wide Input Voltage Range: 3 V to 85 V
- Output Voltage Versions:
  - Fixed: 3.3 V (other versions on request)
  - Adjustable: from 1.2 V up to 20.0 V
- ±0.5% Accuracy at T_J = 25 °C
- Very Low Quiescent Current: 5 μA typ.
- Standby Current: 0.5 μA typ.
- Stable with 1 μF Ceramic Output Capacitor
- Power Good with Programmable Delay
- Thermal Shutdown and Current Limit Protection
- Built-in Soft Start Circuit to Suppress Inrush Current
- Available in Thermally Enhanced MSOP8 EP and DFNW8 3x3 (on request) Packages
- Output Active Discharge Functions
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

- Body Control and Sensor Modules
- On Board Charger
- Infotainment and Audio Systems
- General Purpose Automotive

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.
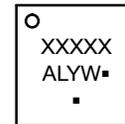
MARKING DIAGRAMS

MSOP8 EP 3x3
(DN SUFFIX)
CASE 846AT

XXXXXX
AYWZZ

XXXX = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
ZZ   = Assembly Lot Code

On Request

DFNW8 3x3
(ML SUFFIX)
CASE 507AD

XXXXX
ALYW∎

XXXXX = Specific Device Marking
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
∎   = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.
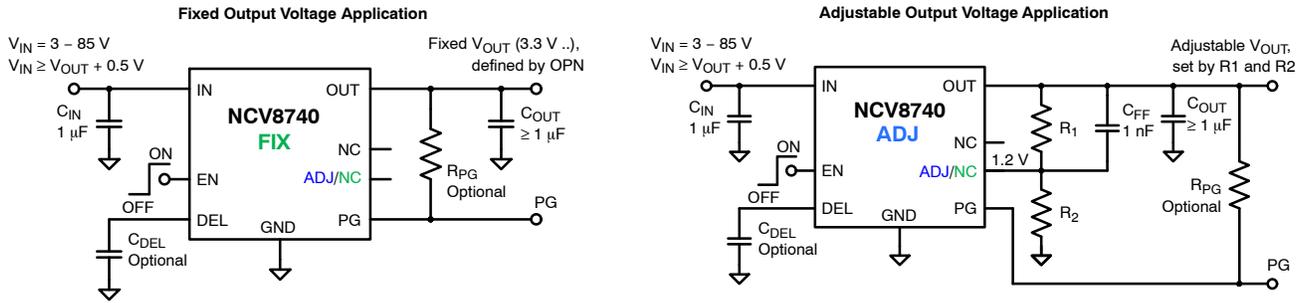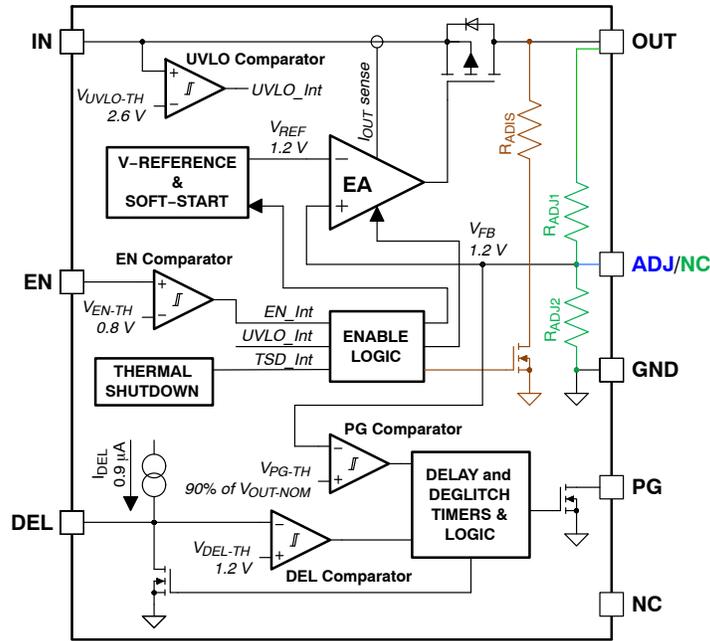
NCV8740

Fixed Output Voltage Application

$V_{IN} = 3 - 85\ V$
$V_{IN} \geq V_{OUT} + 0.5\ V$

Fixed V_{OUT} (3.3 V ..),
defined by OPN

NCV8740
FIX

IN   OUT
NC
ADJ/NC
EN
DEL   GND   PG

C_{IN} 1 µF
C_{DEL} Optional
ON
OFF

R_{PG} Optional
C_{OUT} ≥ 1 µF
PG

Adjustable Output Voltage Application

$V_{IN} = 3 - 85\ V$
$V_{IN} \geq V_{OUT} + 0.5\ V$

Adjustable V_{OUT},
set by R1 and R2

NCV8740
ADJ

IN   OUT
NC
ADJ/NC
EN
DEL   GND   PG

C_{IN} 1 µF
C_{DEL} Optional
ON
OFF

R_1
R_2
1.2 V
C_{FF} 1 nF
C_{OUT} ≥ 1 µF
R_{PG} Optional
PG

Figure 1. Typical Application Schematics

MSOP−8 EP

OUT	1		8	IN
ADJ/NC	2	EP (GND)	7	DEL
PG	3		6	NC
GND	4		5	EN

DFNW−8 3x3

OUT	1		8	IN
ADJ/NC	2	EP (GND)	7	DEL
PG	3		6	NC
GND	4		5	EN

Figure 2. Pin Connections (Top view)

IN

UVLO Comparator
$V_{UVLO-TH}$ 2.6 V
UVLO_Int

$I_{OUT\ sense}$

OUT

R_{ADIS}
R_{ADJ1}
R_{ADJ2}

V−REFERENCE & SOFT−START
V_{REF} 1.2 V
EA

EN

EN Comparator
V_{EN-TH} 0.8 V

V_{FB} 1.2 V

ADJ/NC

EN_Int
UVLO_Int
TSD_Int

ENABLE LOGIC

THERMAL SHUTDOWN

GND

I_{DEL} 0.9 µA

PG Comparator
V_{PG-TH}
90% of $V_{OUT-NOM}$

DELAY and DEGLITCH TIMERS & LOGIC

PG

DEL

V_{DEL-TH} 1.2 V
DEL Comparator

NC

NOTES:
Blue objects are valid for ADJ version only.
Green objects are valid for FIX version only.
Brown objects are valid for active output discharge version only.
Black objects are common to all versions.

Figure 3. Internal Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

Pin No. WDFNW8 3x3	Pin No. MSOP8-EP	Pin Name	Description
1	1	OUT	Regulator output pin. A capacitor $\geq 1\ \mu F$ (effective) must be connected from this pin to GND to assure stability.
2	2	ADJ/NC	This pin is used for adjustable version to set the output voltage by external resistor divider. For fixed voltage versions leave this pin floating.
3	3	PG	Power good output pin. High-Z level for power ok, low level for fail. If not used, could be left unconnected or shorted to GND.
4	4	GND	Power supply ground pin.
5	5	ENA	Chip enable pin (active "H"). Do not leave this pin floating.
6	6	NC	Not connected pin. Leave this pin floating or connect to GND.
7	7	DEL	PG delay pin. Connect a capacitor to GND to adjust the PG delay time. Leave this pin floating if the function is not used.
8	8	IN	Power supply input pin.
EP	EP	EP	Exposed pad. Must be connected to GND potential.

Table 2. ABSOLUTE MAXIMUM RATING

Ratings		Symbol	Value	Unit
IN Pin Voltage Range (Note 1)		V_{IN}	−0.3 to 90	V
OUT Pin Voltage Range	ADJ Version	V_{OUT}	−0.3 to [$(V_{IN} + 0.3)$ or 90; whichever is lower]	V
	FIX Versions		−0.3 to [$(V_{IN} + 0.3)$ or $(3 \times V_{OUT\text{-}NOM})$; whichever is lower]	
OUT Pin Current (forced into the pin) (Note 4)		$I_{OUT\text{-}F}$	1	mA
EN Pin Voltage Range		V_{ENA}	−0.3 to $(Vin + 0.3)$	V
ADJ Pin Voltage Range		V_{ADJ}	−0.3 to 3.6	V
DEL Pin Voltage Range		V_{DEL}	−0.3 to 3.6	V
PG Pin Voltage Range		V_{PG}	−0.3 to $(V_{in} + 0.3)$	V
PG Pin Current		I_{PG}	5	mA
DEL Pin Current		I_{DEL}	5	μA
Maximum Junction Temperature		$T_{J(max)}$	150	°C
Storage Temperature Range		T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1	kV
Moisture Sensitivity Level		MSL	TBD	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)		T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
NOTE: Pin voltages are related to GND pin.
1. Refer to ELECTRICAL CHARACTERISTIC and APPLICATION INFORMATION for Safe operating Area
2. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
    ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002, EIA/JESD22-C101 (AEC Q100-011D)
    Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
4. Continuous current forced into OUT pin must be limited at both cases: when $V_{OUT\text{-}FORCED} > V_{IN}$ and when $V_{OUT\text{-}FOCED} > 0$ V if LDO is disabled by EN pin (applicable to AD version only). Active discharge function is designed just to discharge output capacitor, not to continuously sink current.

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Table 3. THERMAL CHARACTERISTICS (Note 5)

Characteristic	Symbol	MSOP-8	DFNW-8 3x3	Unit
Thermal Resistance, Junction-to-Air	R_{thJA}	38.7	35.4	°C/W
Thermal Resistance, Junction-to-Case (top)	R_{thJCt}	102.0	87.3	°C/W
Thermal Resistance, Junction-to-Case (bottom)	R_{thJCb}	14.7	10.3	°C/W
Thermal Resistance, Junction-to-Board (top)	R_{thJBt}	15.2	10.1	°C/W
Thermal Characterization Parameter, Junction-to-Case (top)	Psi_{JCt}	10.3	7.4	°C/W
Thermal Characterization Parameter, Junction-to-Board [FEM]	Psi_{JB}	15.5	10.2	°C/W

5. Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 645 mm^2, no airflow). Detailed description of the board can be found in JESD51-7.

Table 4. ELECTRICAL CHARACTERISTICS $-40\ °C \le T_J \le 150\ °C$; $V_{IN} = V_{OUTNOM} + 1.0\ V$ or $3.0\ V$ (whichever is greater), $I_{OUT} = 10\ \mu A$, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ (Note 6), ADJ pin connected to V_{OUT} pin, unless otherwise noted. Typical values are at $T_A = +25\ °C$. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT						
Operating Input Voltage		V_{IN}	3		85	V
Input Voltage UVLO Threshold	V_{IN} rising	$V_{UVLO-TH}$	1.7	2.6	3.0	V
Input Voltage UVLO Hysteresis	V_{IN} falling	$V_{UVLO-HY}$	0.01	0.3	0.5	V
OUTPUT						
Output Voltage Accuracy (Note 8)	$T_J = 25\ °C$	V_{OUT}	−0.5	V_{NOM25}	0.5	%
	$T_J = -40\ °C$ to $125\ °C$		−1.5		1.5	
	$T_J = -40\ °C$ to $150\ °C$		−2		1.5	
ADJ Reference Voltage	ADJ version only	V_{ADJ}		1.2		V
ADJ Input Current	ADJ version only, $V_{ADJ} = 1.2\ V$	I_{ADJ}	−100	10	100	nA
Output Voltage Range	ADJ version only	$V_{OUT-ADJ}$	V_{ADJ}		20	V
Line Regulation	$V_{IN} = (V_{OUT-NOM} + 1.0\ V)$ to $85\ V$, $V_{IN} \ge 3.0\ V$	$\Delta V_O/\Delta V_I$		0.01	0.2	%V_{OUT}
Load Regulation	$I_{OUT} = 10\ \mu A$ to $100\ mA$	$\Delta V_O/\Delta I_O$		0.1	0.4	%V_{OUT}
Dropout Voltage	$I_{OUT} = 100\ mA$, all $V_{OUT-NOM}$ versions	V_{DO}		400	830	mV
Output Current Limit	$V_{OUT-FORCED} = V_{OUT-NOM} - 100\ mV$	I_{OLIM}	110	200	300	mA
Short Circuit Current	$V_{OUT} = 0\ V$	I_{OSC}	110	200	300	
Active Discharge Resistance	$V_{EN} = 0V$	R_{ADIS}		50		Ω
CURRENT CONSUMPTION						
Disable Current	$V_{EN} = 0\ V$, $V_{IN} = (V_{OUT-NOM} + 1.0\ V)$ to $85\ V$, $V_{IN} \ge 3.0\ V$	I_{DIS}		0.5	5	μA
Quiescent Current	$I_{OUT} = 0\ mA$, $V_{IN} = (V_{OUT-NOM} + 1.0\ V)$ to $85\ V$, $V_{IN} \ge 3.0\ V$	I_Q		5	15	μA
Ground Current	$I_{OUT} = 100\ mA$	I_{GND}		300	500	μA
ENABLE THRESHOLDS						
Enable Voltage Threshold	V_{EN} rising	V_{EN-TH}	0.3	0.8	1.2	V
Enable Voltage Hysteresis	V_{EN} falling	V_{EN-HY}	0.01	0.1	0.3	V
Enable pin current	$V_{EN} \le 85\ V$	I_{EN}		0.1	1	μA

Table 4. ELECTRICAL CHARACTERISTICS $-40\ °C \le T_J \le 150\ °C$; $V_{IN} = V_{OUTNOM} + 1.0\ V$ or $3.0\ V$ (whichever is greater), $I_{OUT} = 10\ \mu A$, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ (Note 6), ADJ pin connected to V_{OUT} pin, unless otherwise noted. Typical values are at $T_A = +25\ °C$. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PSRR AND NOISE						
Power Supply Ripple Rejection	$V_{OUT} = 3.3\ V$ (ADJ), $C_{FF} = 10\ nF$, $C_{OUT} = 2.2\ \mu F$, $I_{OUT} = 100\ mA$ f = 100 Hz, 0.1 V_{p-p} f = 1 kHz, 0.1 V_{p-p} f = 100 kHz, 0.1 V_{p-p}	PSRR		 TBD TBD TBD		dB
Output Noise Voltage	$V_{OUT} = 3.3\ V$ (ADJ), $C_{FF} = 10\ nF$, $C_{OUT} = 2.2\ \mu F$, $I_{OUT} = 100\ mA$ f = 10 Hz to 100 kHz f = 10 Hz to 1 MHz	V_{NOISE}		 83 130		μV_{rms}
POWER GOOD, DELAY						
Power Good V_{OUT} Threshold	V_{OUT} rising	V_{PG-THR}	85%	90%	95%	V_{OUTNOM}
	V_{OUT} falling	V_{PG-THF}	83%	88%	93%	V_{OUTNOM}
Power Good V_{OUT} Hysteresis		V_{PG-HY}		2.5%	4%	V_{OUTNOM}
Power Good Voltage Low	$V_{OUT} = 80\%\ V_{OUT-NOM}$, $I_{PG} = 1\ mA$	V_{PG-LO}		0.05	0.25	V
Power Good Leakage Current	$V_{PG} = V_{OUT-NOM}$	I_{PG}		0.02	1	μA
Delay pin Current	$V_{DEL} = 0\ V$	I_{DEL}	0.3	0.9	2	μA
Delay pin Threshold Voltage	V_{DEL} rising	V_{DEL-TH}	1.1	1.2	1.3	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}		170		°C
Thermal Shutdown Hysteresis		T_{SH}		15		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A = 25\ °C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Typical value of output voltage at 25 °C is set during testing to value $V_{NOM25} = V_{NOM} * 1.003$ (what means +0.3% above V_{NOM}) to have symmetrical deviation of V_{OUT} to V_{NOM} over the whole temperature range. Note that V_{OUT} at 25 °C is at it's maximum. See V_{OUT} vs. Temperature chart below for details.
9. Dropout voltage is measured when the output voltage falls 100 mV below the nominal output voltage. A_{DJ} version is measured with A_{DJ} pin connected to resistor divider which sets V_{OUT} to 3.3 V. Limits are valid for all voltage versions.

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APPLICATIONS INFORMATION

The NCV8740 is high input voltage regulator with internal thermal shutdown and internal current limit. Typical application circuits are shown in Figures TBD to TBD.

Input Decoupling (C$_{in}$)

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected as close as possible to the input pin of NCV8740 regulator. Higher capacitance and lower ESR will improve the overall line and load transient response. Larger values help improve Line Transient response and minimize the impact of long input traces at the PCB path.

Output Decoupling (C$_{out}$)

The NCV8740 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling effective value is 0.9 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors up to 100 μF. The larger values improve noise rejection and load regulation transient response.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. The turn-on/turn-off transient voltage being supplied to the enable pin should exceed a slew rate of TBD mV/μs to ensure correct operation. If the enable function is not to be used then the pin should be connected to VIN pin.

Output Voltage Adjust

The output voltage can be adjusted from 1.2 V to 20.0 V using resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{out} = V_{ADJ}\left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \quad \text{(eq. 1)}$$

$$R_2 \cong R_1 \frac{1}{\dfrac{V_{out}}{V_{ADJ}} - 1} \quad \text{(eq. 2)}$$

Input bias current I$_{ADJ}$ is typically less than TBD nA. Choose R$_1$ arbitrarily to minimize errors due to the bias current and to minimize noise contribution to the output voltage. Use Equation 2. in order to find the required value for R$_2$.

Thermal Considerations

As power in the NCV8740 regulator increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8740 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8740 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 3)}$$

See the chart in Typical Characteristic chapter for R$_{thJA}$ versus PCB area relation. The power dissipated by the NCV8740 device can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_{GND}@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 4)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_{GND}} \quad \text{(eq. 5)}$$

Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5-V or lower rail through an external pull-up resistor. When C$_{DELAY}$ is not used, the PG output is high-impedance when V$_{OUT}$ is greater than the PG threshold. If V$_{OUT}$ falls below PG threshold, the open-drain output turns on and pulls the PG pin to ground. The Current through PG pin is internally limited in order to avoid device damage by flowing a high current through this pin. If the output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

Power Good Delay

The power-good delay time (t$_{DELAY}$) is defined as the time period from when VOUT exceeds the PG trip threshold voltage to point when the PG output is high. This power-good delay time could be set by an external capacitor (C$_{DEL}$) connected from the DEL pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I$_{DEL}$) once VOUT exceeds the PG threshold .

When C$_{DELAY}$ is used, the PG output is high-impedance when V$_{OUT}$ exceeds PG threshold, and V$_{DELAY}$ exceeds V$_{REF}$.

The Power Good Delay time can be calculated using: t$_{DELAY}$ = (C$_{DEL}$ * V$_{REF}$) / I$_{DEL}$.

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8740, and make traces as short as possible.

NCV8740

ORDERING INFORMATION (Note 10)

Device pn.	Output Voltage	OUT Active Discharge	Marking	Package	Shipping†
NCV8740ADN330R2G	3.3 V	Yes	V74A33	MSOP8 EP 3x3 Pb-Free	4000 / Tape & Reel
NCV8740ADN500R2G	5 V	Yes	V74A50		
NCV8740ADNADJR2G	ADJ	Yes	V74AAD		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. To order DFNW8 3x3 package, other FIX voltage version, A$_{DJ}$ version or non output active discharge version, please contact your **onsemi** sales representative.

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REVISION HISTORY

Revision	Description of Changes	Date
P1	Application schematic, pinout diagrams and internal block diagram updated by higher quality pictures. Added "OUT pin current" line to absolute max. rating table. Updated "Thermal characteristics" table. Updated "Electrical char." table – added "Input UVLO threshold and hysteresis" parameters, low limit of "Output current limit" and "Short Circuit Current" both respecified from 100 to 110 mA, reworded "EN threshold and hysteresis" parameters. Updated equations 1 and 2 – TBD replaced by VADJ. Table "Ordering information" – removed NCV8740ADNADJR2G part, added marking for all other parts and changed shipping quantity from 3000 to 4000.	6/20/2025
P2	Updated DFNW Thermal Characteristics values.	9/19/2025
P3	Device NCV8740ADNADJR2G added to the Ordering Information table.	3/2/2026

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MSOP8 EP 3x3
CASE 846AT
ISSUE O

DATE 01 OCT 2020

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

TOP VIEW

SIDE VIEW

END VIEW

DETAIL A

BOTTOM VIEW

NOTE 3

DETAIL A

RECOMMENDED
MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°

✳ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***

XXXXXX
AYWZZ

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON25934H		
DESCRIPTION:	MSOP8 EP 3x3		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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