

Protected Power MOSFET

2.6 A, 52 V, N-Channel, Logic Level,
Clamped MOSFET w/ ESD Protection

NCV8440, NCV8440A

Features

- Diode Clamp Between Gate and Source
- ESD Protection – Human Body Model 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance
- These are Pb-Free Devices

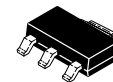
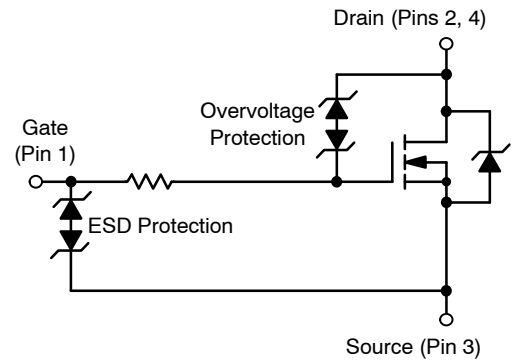
Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

Applications

- Automotive and Industrial Markets:
Solenoid Drivers, Lamp Drivers, Small Motor Drivers
- NCV Prefix for Automotive and Other Applications Requiring
Unique Site and Control Change Requirements; AEC-Q100
Qualified and PPAP Capable

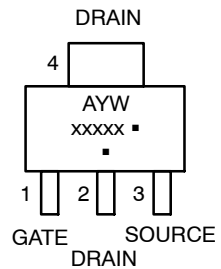
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX
52 V	95 mΩ @ 10 V	2.6 A



**SOT-223
CASE 318E
STYLE 3**

1 = Gate
2 = Drain
3 = Source

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
xxxxx = V8440 or 8440A
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NCV8440, NCV8440A

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V _{DSS}	52-59	V
Gate-to-Source Voltage – Continuous	V _{GS}	±15	V
Drain Current – Continuous @ T _A = 25°C – Single Pulse (t _p = 10 μs) (Note 1)	I _D I _{DM}	2.6 10	A
Total Power Dissipation @ T _A = 25°C (Note 1)	P _D	1.69	W
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 50 V, I _{D(pk)} = 1.17 A, V _{GS} = 10 V, L = 160 mH, R _G = 25 Ω)	E _{AS}	110	mJ
Load Dump Voltage (V _{GS} = 0 and 10 V, R _I = 2.0 Ω, R _L = 9.0 Ω, t _d = 400 ms)	V _{LD}	60	V
Thermal Resistance, Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R _{θJA} R _{θJA}	74 169	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in²).
2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in²).

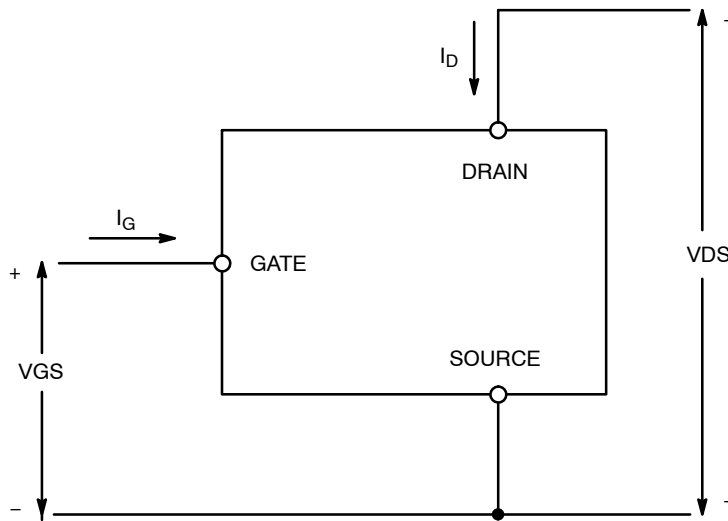


Figure 1. Voltage and Current Convention

NCV8440, NCV8440A

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ V}$, $I_D = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$) ($V_{GS} = 0\text{ V}$, $I_D = 1.0\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C) (Note 4) Temperature Coefficient (Negative)	$V_{(BR)DSS}$	52 50.8	55 54 -9.3	59 59.5	V V mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$) (Note 4)	I_{DSS}			10 25	μA
Gate-Body Leakage Current ($V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$) ($V_{GS} = \pm 14\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}		± 35	± 10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.1	1.5 -4.1	1.9	V mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 3.5\text{ V}$, $I_D = 0.6\text{ A}$) ($V_{GS} = 4.0\text{ V}$, $I_D = 1.5\text{ A}$) ($V_{GS} = 10\text{ V}$, $I_D = 2.6\text{ A}$)	$R_{DS(on)}$		150 135 95	180 160 110	m Ω
Forward Transconductance (Note 3) ($V_{DS} = 15\text{ V}$, $I_D = 2.6\text{ A}$)	g_{FS}		3.8		Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 35\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$	C_{iss}		155		pF
Output Capacitance		C_{oss}		60		
Transfer Capacitance		C_{rss}		25		
Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$	C_{iss}		170		pF
Output Capacitance		C_{oss}		70		
Transfer Capacitance		C_{rss}		30		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Not subject to production testing.
- Switching characteristics are independent of operating junction temperatures.



NCV8440, NCV8440A

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 5)					
Turn-On Delay Time	$t_{d(on)}$		375		ns
Rise Time	t_r		1525		
Turn-Off Delay Time	$t_{d(off)}$		1530		
Fall Time	t_f		1160		
Turn-On Delay Time	$t_{d(on)}$		325		ns
Rise Time	t_r		1275		
Turn-Off Delay Time	$t_{d(off)}$		1860		
Fall Time	t_f		1150		
Turn-On Delay Time	$t_{d(on)}$		190		ns
Rise Time	t_r		710		
Turn-Off Delay Time	$t_{d(off)}$		2220		
Fall Time	t_f		1180		
Gate Charge	Q_T		4.5		nC
	Q_1		0.9		
	Q_2		2.6		
Gate Charge	Q_T		3.9		nC
	Q_1		1.0		
	Q_2		1.7		

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$I_S = 2.6\text{ A}$, $V_{GS} = 0\text{ V}$ (Note 3) $I_S = 2.6\text{ A}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$	V_{SD}		0.81 0.66	1.5	V
Reverse Recovery Time	$I_S = 1.5\text{ A}$, $V_{GS} = 0\text{ V}$, $di_S/dt = 100\text{ A}/\mu\text{s}$ (Note 3)	t_{rr}		730		ns
		t_a		200		
		t_b		530		
Reverse Recovery Stored Charge		Q_{RR}		6.3		μC

ESD CHARACTERISTICS (Note 4)

Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	5000			V
	Machine Model (MM)		500			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Not subject to production testing.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

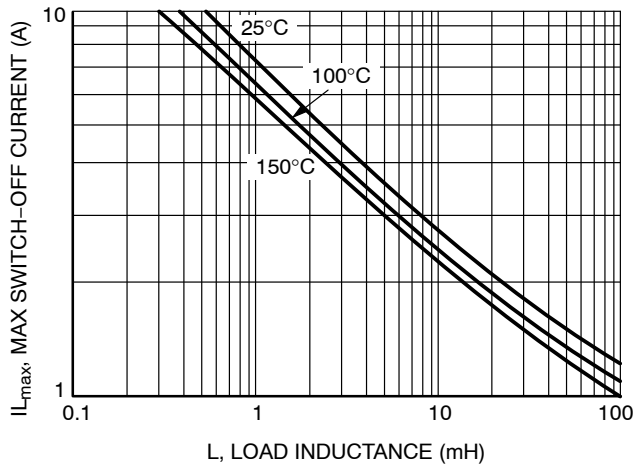


Figure 1. Single Pulse Maximum Switch-off Current vs. Load Inductance

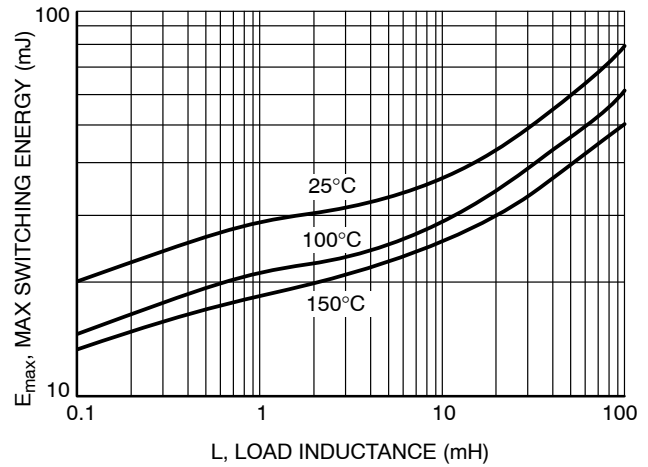


Figure 2. Single Pulse Maximum Switching Energy vs. Load Inductance

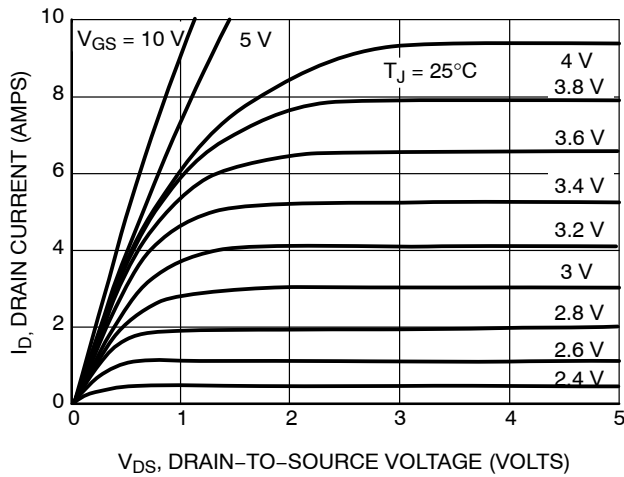


Figure 3. On-State Output Characteristics

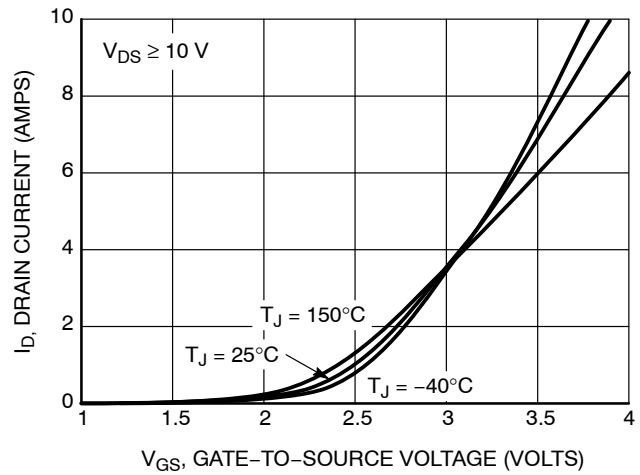


Figure 4. Transfer Characteristics

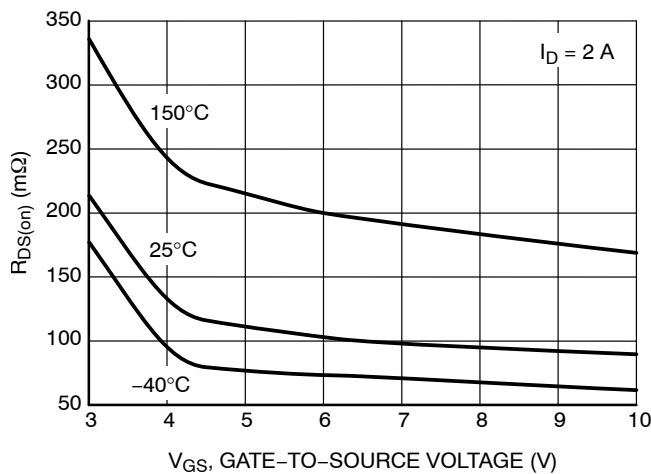


Figure 5. $R_{DS(on)}$ vs. Gate-Source Voltage

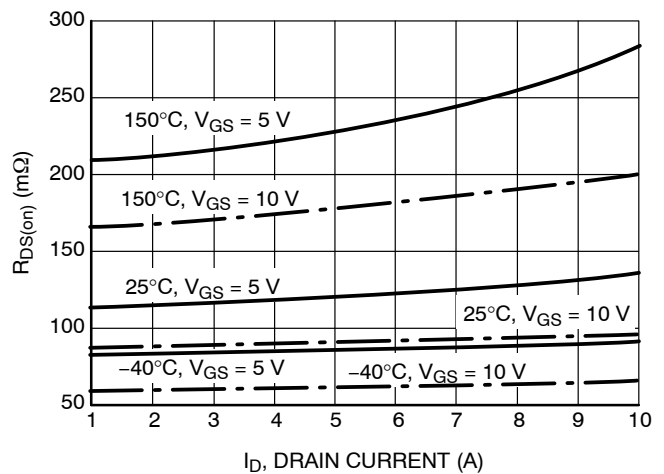


Figure 6. $R_{DS(on)}$ vs. Drain Current

TYPICAL PERFORMANCE CURVES

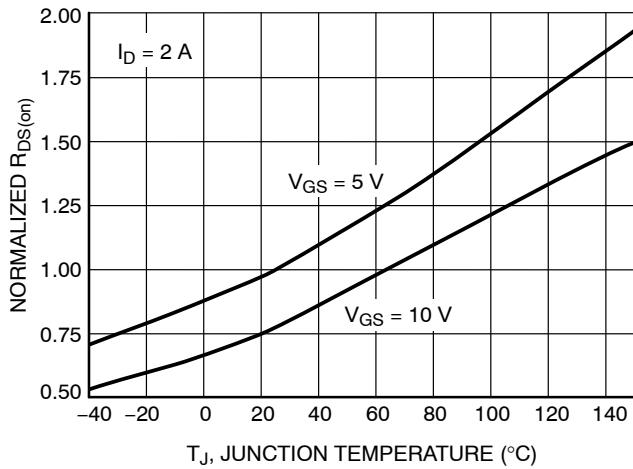


Figure 7. Normalized $R_{DS(on)}$ vs. Temperature

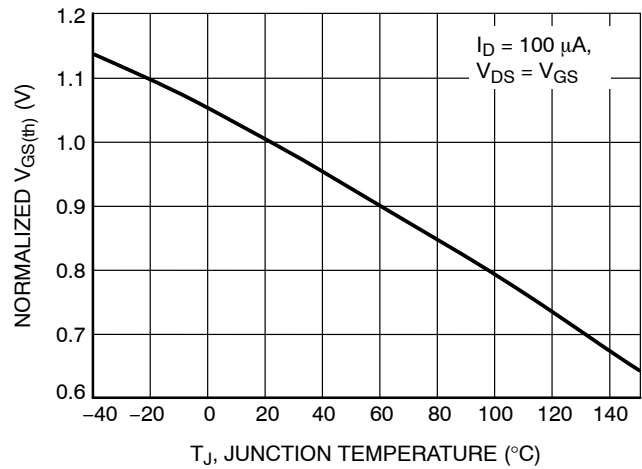


Figure 8. Normalized Threshold Voltage vs. Temperature

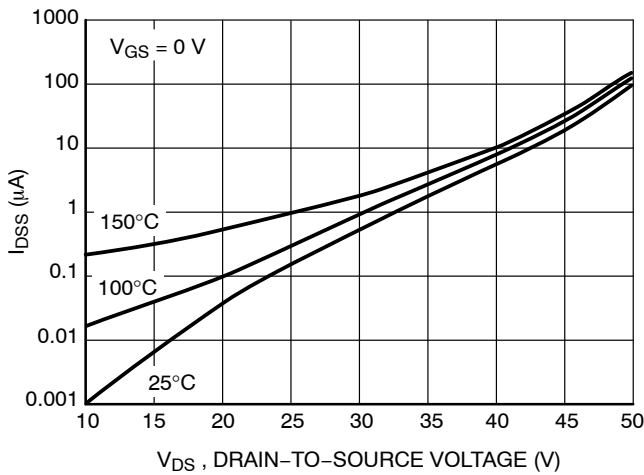


Figure 9. Drain-to-Source Leakage Current

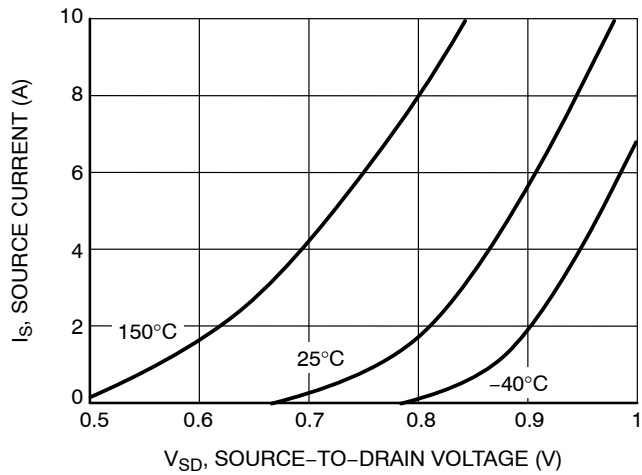


Figure 10. Source-Drain Diode Forward Characteristics

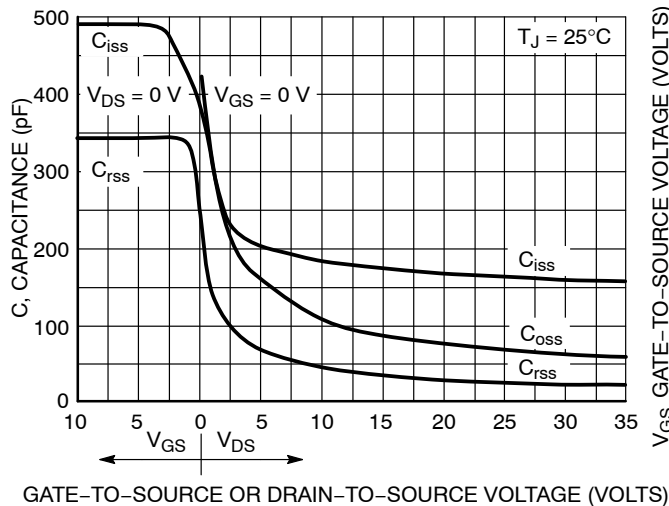


Figure 11. Capacitance Variation

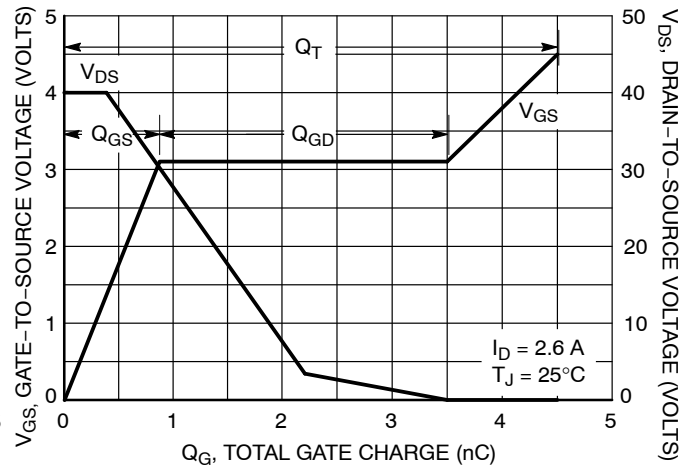


Figure 12. Gate-to-Source Voltage vs. Total Gate Charge

TYPICAL PERFORMANCE CURVES

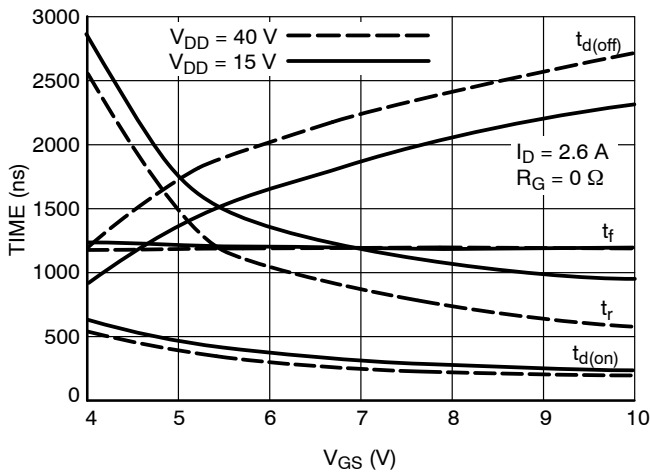


Figure 13. Resistive Load Switching Time vs. Gate-Source Voltage

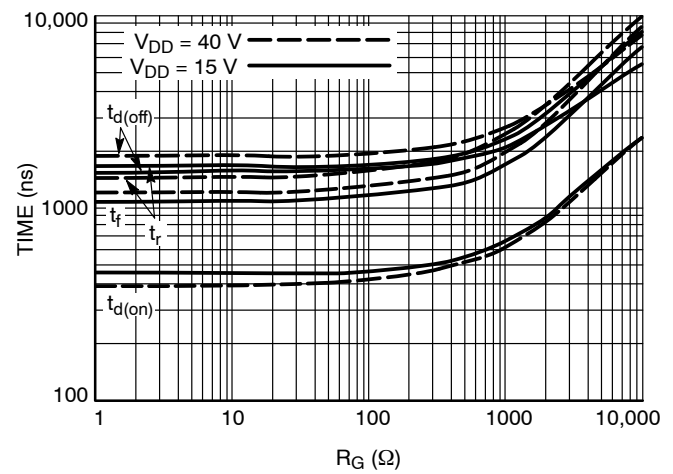


Figure 14. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 5\text{ V}$, $I_D = 2.6\text{ A}$)

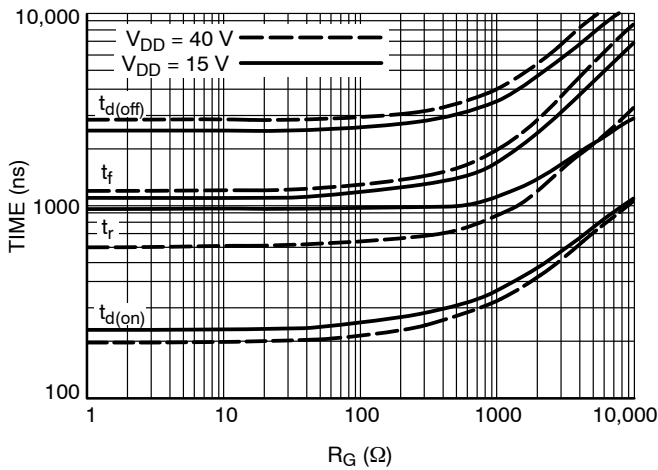


Figure 15. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 10\text{ V}$, $I_D = 2.6\text{ A}$)

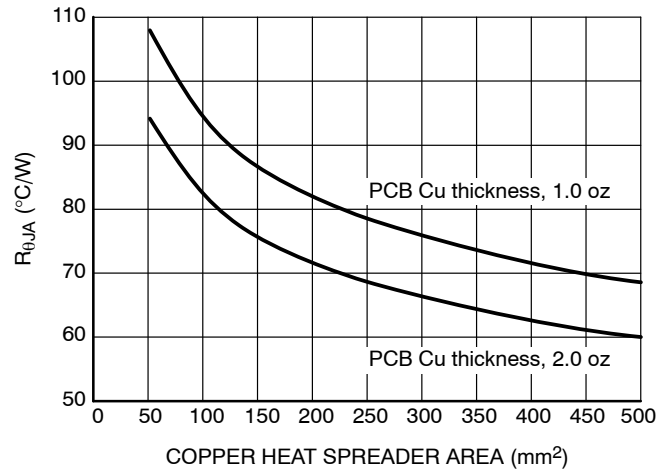


Figure 16. $R_{\theta JA}$ vs. Copper Area

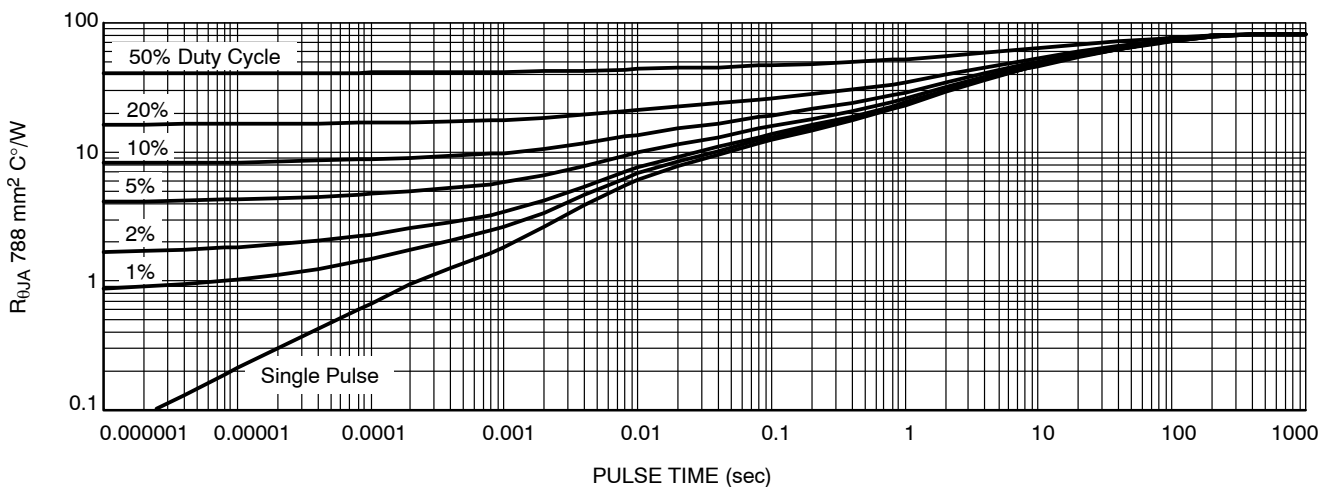


Figure 17. Transient Thermal Resistance

NCV8440, NCV8440A

ORDERING INFORMATION

Device	Package	Shipping†
NCV8440STT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8440ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8440STT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8440ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel

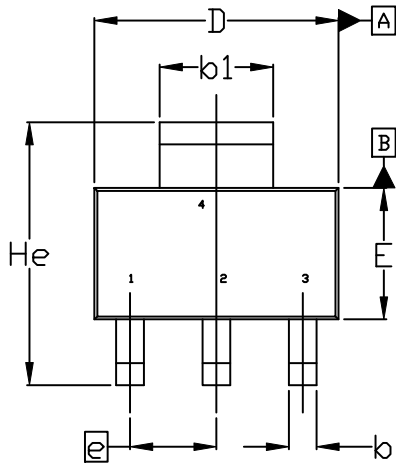
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



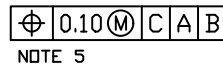
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

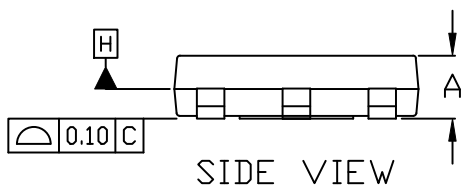
DATE 02 OCT 2018



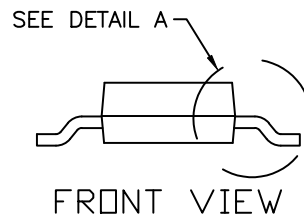
TOP VIEW



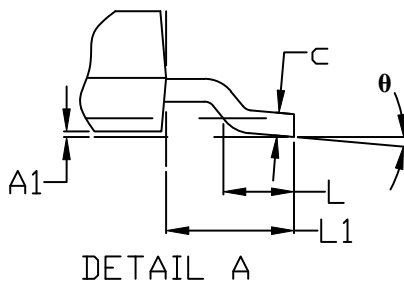
NOTE 5



SIDE VIEW



FRONT VIEW

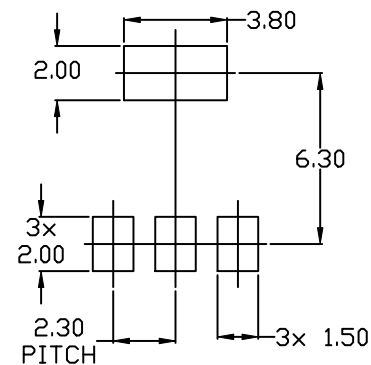


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°


RECOMMENDED MOUNTING
FOOTPRINT

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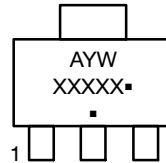
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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