

# Self Protected Very Low Iq High Side Driver with Analog Current Sense

## NCV84120

The NCV84120 is a fully protected single channel high side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids, and other actuators. The device incorporates advanced protection features such as active inrush current management, over-temperature shutdown with automatic restart and an overvoltage active clamp. A dedicated Current Sense pin provides precision analog current monitoring of the output as well as fault indication of short to  $V_D$ , short circuit to ground and OFF state open load detection. An active high Current Sense Enable pin allows all diagnostic and current sense features to be enabled.

### Features

- Short Circuit Protection with Inrush Current Management
- CMOS (3 V / 5 V) Compatible Control Input
- Very Low Standby Current
- Very Low Current Sense Leakage
- Proportional Load Current Sense
- Current Sense Enable
- Off State Open Load Detection
- Output Short to  $V_D$  Detection
- Overload and Short to Ground Indication
- Thermal Shutdown with Automatic Restart
- Undervoltage Shutdown
- Integrated Clamp for Inductive Switching
- Loss of Ground and Loss of  $V_D$  Protection
- ESD Protection
- Reverse Battery Protection
- AEC-Q100 Qualified
- This is a Pb-Free Device

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

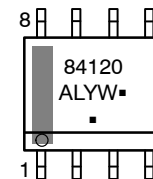
### FEATURE SUMMARY

|   |              |         |               |
|---|--------------|---------|---------------|
| Max Supply Voltage                              | $V_D$        | 41      | V             |
| Operating Voltage Range                         | $V_D$        | 4 to 28 | V             |
| $R_{DS(on)}$ (typical) $T_J = 25^\circ\text{C}$ | $R_{ON}$     | 120     | m $\Omega$    |
| Output Current Limit (typical)                  | $I_{lim}$    | 18      | A             |
| OFF-state Supply Current (max)                  | $I_{D(off)}$ | 0.5     | $\mu\text{A}$ |



SOIC-8  
CASE 751-07  
STYLE 11

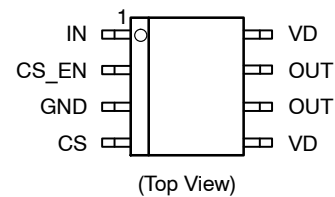
### MARKING DIAGRAM



84120 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

| Device       | Package             | Shipping <sup>†</sup> |
|--------------|---------------------|-----------------------|
| NCV84120DR2G | SOIC-8<br>(Pb-Free) | 2500 / Tape &<br>Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM & PIN CONFIGURATION

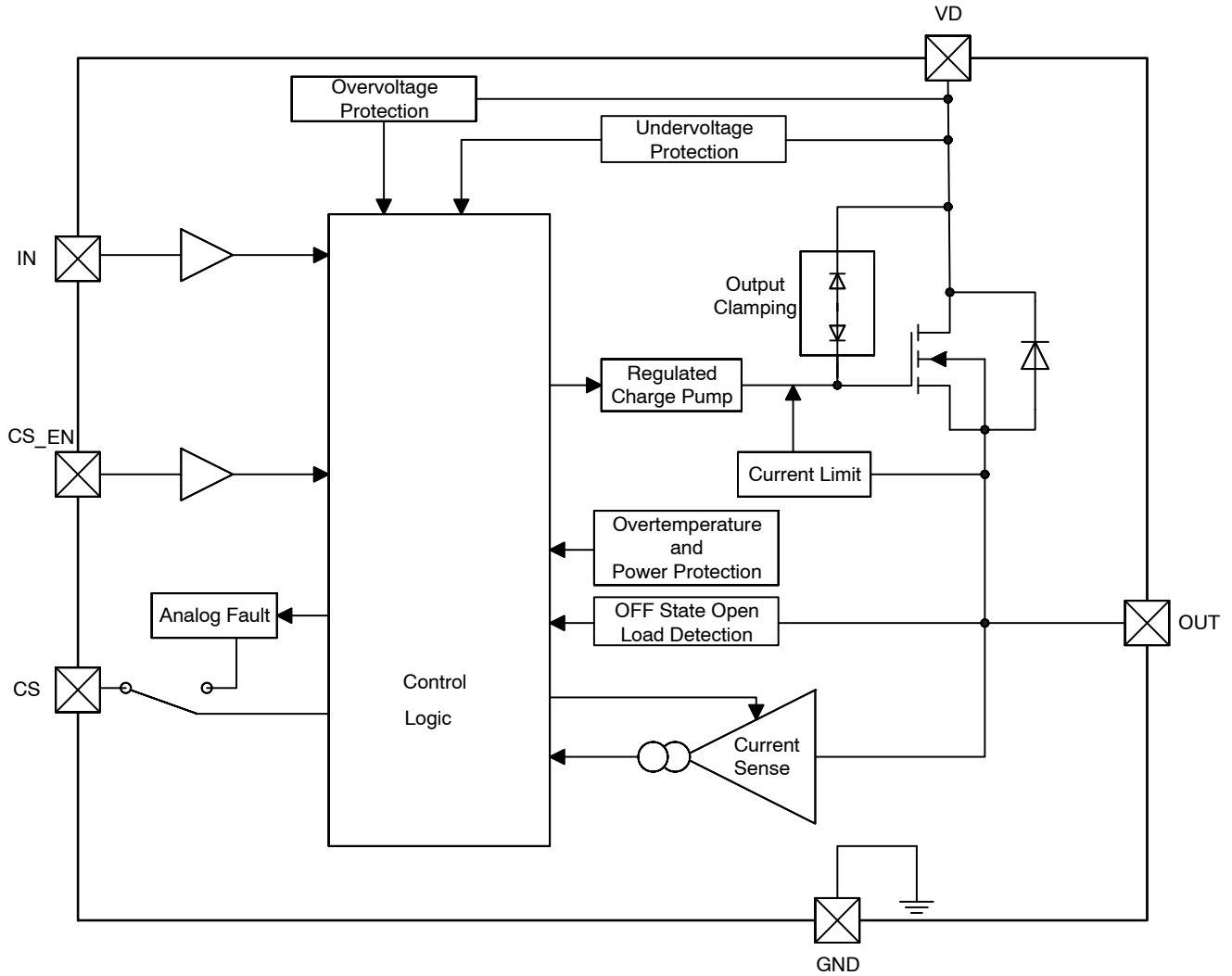


Figure 1. Block Diagram

Table 1. SO8 PACKAGE PIN DESCRIPTION

| Pin # | Symbol | Description                 |
|-------|--------|-----------------------------|
| 1     | IN     | Logic Level Input           |
| 2     | CS_EN  | Current Sense Enable        |
| 3     | GND    | Ground                      |
| 4     | CS     | Analog Current Sense Output |
| 5     | VD     | Supply Voltage              |
| 6     | OUT    | Output                      |
| 7     | OUT    | Output                      |
| 8     | VD     | Supply Voltage              |

# NCV84120

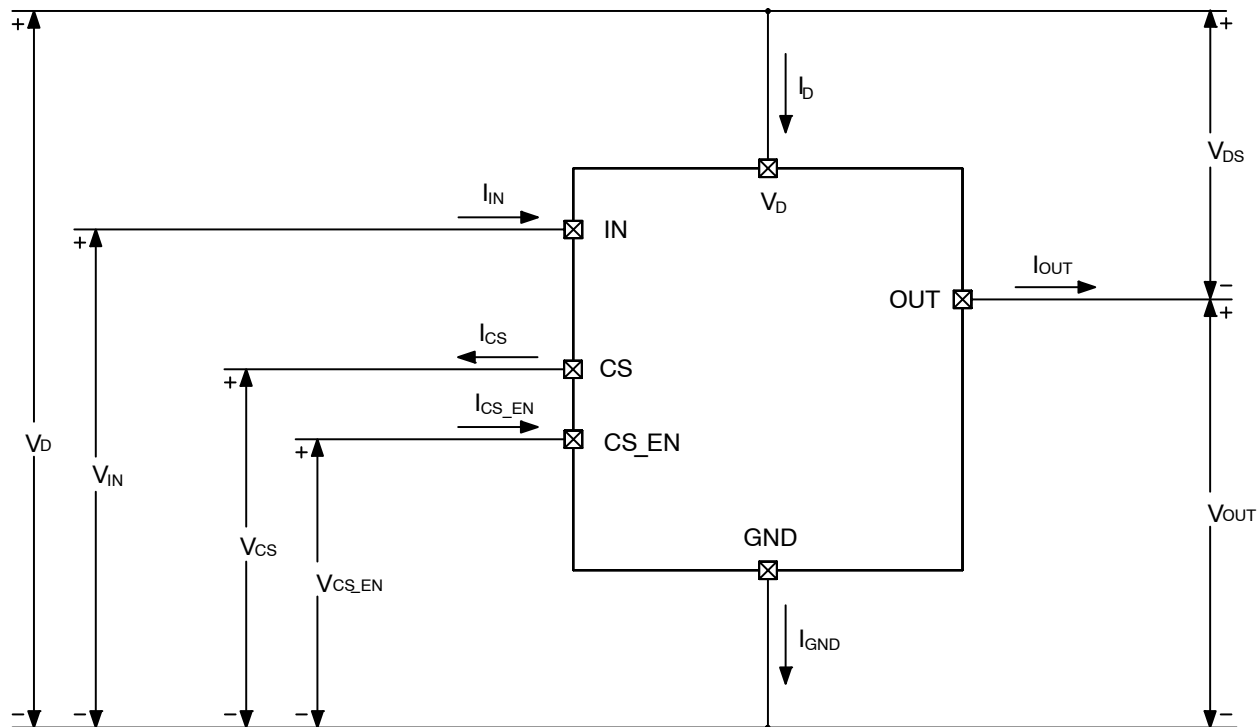


Figure 2. Voltage and Current Conventions

Table 2. Connection suggestions for unused and or unconnected pins

| Connection | Input                  | Output      | Current Sense         | Current Sense Enable   |
|------------|------------------------|-------------|-----------------------|------------------------|
| Floating   | X                      | X           | Not Allowed           | X                      |
| To Ground  | Through 10 kΩ resistor | Not Allowed | Through 1 kΩ Resistor | Through 10 kΩ resistor |

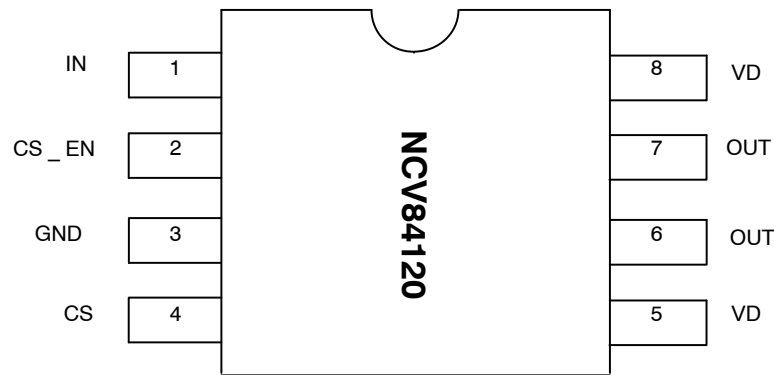


Figure 3. Pin Configuration (Top View)

# ELECTRICAL SPECIFICATIONS

**Table 3. MAXIMUM RATINGS**

| Rating  | Symbol        | Value      |                    | Unit             |
|---|---------------|------------|--------------------|------------------|
| DC Supply Voltage   | $V_D$         | -0.3       | 41                 | V                |
| Max Transient Supply Voltage (Note 1)<br>Load Dump – Suppresses   | $V_{PEAK}$    | –          | 45                 | V                |
| Input Voltage   | $V_{IN}$      | -10        | 10                 | V                |
| Input Current   | $I_{IN}$      | -5         | 5                  | mA               |
| Reverse Ground Pin Current  | $I_{GND}$     | –          | -200               | mA               |
| Output Current (Note 2)   | $I_{OUT}$     | -6         | Internally Limited | A                |
| Reverse CS Current  | $I_{CS}$      | –          | -200               | mA               |
| CS Voltage  | $V_{CS}$      | $V_D - 41$ | $V_D$              | V                |
| CS_EN Voltage   | $V_{CS\_EN}$  | -10        | 10                 | V                |
| CS_EN Current   | $I_{CS\_EN}$  | -5         | 5                  | mA               |
| Power Dissipation $T_c = 25^\circ\text{C}$ (Note 6)   | $P_{tot}$     | 1.95       |                    | W                |
| Electrostatic Discharge (Note 3)<br>(HBM Model 100 pF / 1500 $\Omega$ )   | $V_{ESD}$     |            |                    | DC               |
| Input   |               | 4          | –                  | kV               |
| Current Sense   |               | 4          | –                  | kV               |
| Current Sense Enable  |               | 4          | –                  | kV               |
| Output  |               | 4          | –                  | kV               |
| $V_D$   |               | 4          | –                  | kV               |
| Charged Device Model<br>CDM-AEC-Q100-011  |               | 750        | –                  | V                |
| Single Pulse Inductive Load Switching Energy<br>( $L = 5\text{ mH}$ , $V_D = 13.5\text{ V}$ , $I_L = 4\text{ A}$ , $T_{Jstart} = 150^\circ\text{C}$ (Note 4)) | $E_{AS}$      | 56         | –                  | mJ               |
| Operating Junction Temperature  | $T_J$         | -40        | +150               | $^\circ\text{C}$ |
| Storage Temperature   | $T_{storage}$ | -55        | +150               | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C (or A, B) according to ISO16750-1.
2. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance.
3. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (JS-001-2017)  
Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2018
4. Not subjected to production testing.

**Table 4. THERMAL RESISTANCE RATINGS**

| Parameter                    | Symbol          | Max. Value | Units              |
|------------------------------|-----------------|------------|--------------------|
| Thermal Resistance           |                 |            | $^\circ\text{C/W}$ |
| Junction-to-Lead (Note 5)    | $R_{\theta JL}$ | 27.3       |                    |
| Junction-to-Ambient (Note 5) | $R_{\theta JA}$ | 50         |                    |
| Junction-to-Ambient (Note 6) | $R_{\theta JA}$ | 64         |                    |

5. 645 mm<sup>2</sup> pad size, mounted on four-layer 2s2p PCB – FR4, 2 oz. Cu thickness for top layer and 1 oz. Cu thickness for inner layers (planes not electrically connected)
6. 2 cm<sup>2</sup> pad size, mounted on single-layer 2s0p PCB – FR4, 2 oz. Cu thickness

**ELECTRICAL CHARACTERISTICS** ( $7\text{ V} \leq V_D \leq 28\text{ V}$ ;  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  unless otherwise specified)

**Table 5. POWER**

| Rating                           | Symbol         | Conditions  | Value |     |     | Unit             |
|----------------------------------|----------------|---|-------|-----|-----|------------------|
|                                  |                |   | Min   | Typ | Max |                  |
| Operating Supply Voltage         | $V_D$          |   | 4     | –   | 28  | V                |
| Undervoltage Shutdown            | $V_{UV}$       |   | –     | 3.5 | 4   | V                |
| Undervoltage Shutdown Hysteresis | $V_{UV\_hyst}$ |   | –     | 0.4 | –   | V                |
| On Resistance                    | $R_{ON}$       | $I_{OUT} = 2\text{ A}$ , $T_J = 25^\circ\text{C}$   | –     | 120 | –   | $\text{m}\Omega$ |
|                                  |                | $I_{OUT} = 2\text{ A}$ , $T_J = 150^\circ\text{C}$  | –     | –   | 240 |                  |
|                                  |                | $I_{OUT} = 2\text{ A}$ , $V_D = 4.5\text{ V}$ , $T_J = 25^\circ\text{C}$                                | –     | –   | 180 |                  |
| Supply Current (Note 7)          | $I_D$          | OFF-state: $V_D = 13\text{ V}$ ,<br>$V_{IN} = V_{OUT} = 0\text{ V}$ , $T_J = 25^\circ\text{C}$          | –     | 0.2 | 0.5 | $\mu\text{A}$    |
|                                  |                | OFF-state: $V_D = 13\text{ V}$ ,<br>$V_{IN} = V_{OUT} = 0\text{ V}$ , $T_J = 85^\circ\text{C}$ (Note 8) | –     | 0.2 | 0.5 | $\mu\text{A}$    |
|                                  |                | OFF-state: $V_D = 13\text{ V}$ ,<br>$V_{IN} = V_{OUT} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$         | –     | –   | 3   | $\mu\text{A}$    |
|                                  |                | ON-state: $V_D = 13\text{ V}$ ,<br>$V_{IN} = 5\text{ V}$ , $I_{OUT} = 0\text{ A}$                       | –     | 1.9 | 3.5 | $\text{mA}$      |
| On State Ground Current          | $I_{GND(ON)}$  | $V_D = 13\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$<br>$V_{IN} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$       | –     | –   | 6   | $\text{mA}$      |
| Output Leakage Current           | $I_L$          | $V_{IN} = V_{OUT} = 0\text{ V}$ , $V_D = 13\text{ V}$ , $T_J = 25^\circ\text{C}$                        | –     | –   | 0.5 | $\mu\text{A}$    |
|                                  |                | $V_{IN} = V_{OUT} = 0\text{ V}$ , $V_D = 13\text{ V}$ , $T_J = 125^\circ\text{C}$                       | –     | –   | 3   |                  |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Includes PowerMOS leakage current.

8. Not subjected to production testing.

**Table 6. LOGIC INPUTS** ( $V_D = 13.5\text{ V}$ ;  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ )

| Rating                   | Symbol          | Conditions                  | Value |     |     | Unit          |
|--------------------------|-----------------|-----------------------------|-------|-----|-----|---------------|
|                          |                 |                             | Min   | Typ | Max |               |
| Input Voltage – Low      | $V_{IN\_low}$   |                             | –     | –   | 0.9 | V             |
| Input Current – Low      | $I_{IN\_low}$   | $V_{IN} = 0.9\text{ V}$     | 1     | –   | –   | $\mu\text{A}$ |
| Input Voltage – High     | $V_{IN\_high}$  |                             | 2.1   | –   | –   | V             |
| Input Current – High     | $I_{IN\_high}$  | $V_{IN} = 2.2\text{ V}$     | –     | –   | 10  | $\mu\text{A}$ |
| Input Hysteresis Voltage | $V_{IN\_hyst}$  |                             | –     | 0.2 | –   | V             |
| Input Clamp Voltage      | $V_{IN\_cl}$    | $I_{IN} = 1\text{ mA}$      | 12    | 13  | 14  | V             |
|                          |                 | $I_{IN} = -1\text{ mA}$     | -14   | -13 | -12 |               |
| CS_EN Voltage – Low      | $V_{CSE\_low}$  |                             | –     | –   | 0.9 | V             |
| CS_EN Current – Low      | $I_{CSE\_low}$  | $V_{CS\_EN} = 0.9\text{ V}$ | 1     | –   | –   | $\mu\text{A}$ |
| CS_EN Voltage – High     | $V_{CSE\_high}$ |                             | 2.1   | –   | –   | V             |
| CS_EN Current – High     | $I_{CSE\_high}$ | $V_{CS\_EN} = 2.2\text{ V}$ | –     | –   | 10  | $\mu\text{A}$ |
| CS_EN Hysteresis Voltage | $V_{CSE\_hyst}$ |                             | –     | 0.2 | –   | V             |
| CS_EN Clamp Voltage      | $V_{CSE\_cl}$   | $I_{CS\_EN} = 1\text{ mA}$  | 12    | 13  | 14  | V             |
|                          |                 | $I_{CS\_EN} = -1\text{ mA}$ | -14   | -13 | -12 |               |

**Table 7. SWITCHING CHARACTERISTICS** (Note 9) ( $V_D = 13\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ )

| Rating   | Symbol              | Conditions  | Value |      |      | Unit                     |
|--|---------------------|---|-------|------|------|--------------------------|
|  |                     |   | Min   | Typ  | Max  |                          |
| Turn-On Delay Time   | $t_{d\_on}$         | $V_{IN}$ high to 20% $V_{OUT}$ , $R_L = 6.5\ \Omega$ , $T_J = 25^\circ\text{C}$ | 5     | 70   | 120  | $\mu\text{s}$            |
| Turn-Off Delay Time  | $t_{d\_off}$        | $V_{IN}$ low to 80% $V_{OUT}$ , $R_L = 6.5\ \Omega$ , $T_J = 25^\circ\text{C}$  | 5     | 40   | 100  | $\mu\text{s}$            |
| Slew Rate On   | $dV_{out}/dt_{on}$  | 20% to 80% $V_{OUT}$ , $R_L = 6.5\ \Omega$ , $T_J = 25^\circ\text{C}$           | 0.1   | 0.27 | 0.7  | $\text{V} / \mu\text{s}$ |
| Slew Rate Off  | $dV_{out}/dt_{off}$ | 80% to 20% $V_{OUT}$ , $R_L = 6.5\ \Omega$ , $T_J = 25^\circ\text{C}$           | 0.1   | 0.35 | 0.7  | $\text{V} / \mu\text{s}$ |
| Turn-On Switching Loss (Note 9)  | $E_{on}$            | $R_L = 6.5\ \Omega$   | –     | 0.15 | 0.32 | mJ                       |
| Turn-Off Switching Loss (Note 9)   | $E_{off}$           | $R_L = 6.5\ \Omega$   | –     | 0.1  | 0.32 | mJ                       |
| Differential Pulse Skew, ( $t_{OFF}$ – $t_{ON}$ ) see Figure 4 (Switching Characteristics) | $t_{skew}$          | $R_L = 6.5\ \Omega$   | –50   | –    | 50   | $\mu\text{s}$            |

9. Not subjected to production testing.

**Table 8. OUTPUT DIODE CHARACTERISTICS**

| Rating          | Symbol | Conditions  | Value |     |     | Unit |
|-----------------|--------|---|-------|-----|-----|------|
|                 |        |   | Min   | Typ | Max |      |
| Forward Voltage | $V_F$  | $I_{OUT} = -1\text{ A}$ , $T_J = 150^\circ\text{C}$ , $V_F = V_{OUT} - V_D$ | –     | –   | 0.7 | V    |

**Table 9. PROTECTION FUNCTIONS** (Note 10) ( $7\text{ V} \leq V_D \leq 18\text{ V}$ ;  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ )

| Rating   | Symbol            | Conditions  | Value      |            |            | Unit             |
|--|-------------------|---|------------|------------|------------|------------------|
|  |                   |   | Min        | Typ        | Max        |                  |
| Temperature Shutdown (Note 11)                               | $T_{SD}$          |   | 150        | 175        | 200        | $^\circ\text{C}$ |
| Temperature Shutdown Hysteresis ( $T_{SD} - T_R$ ) (Note 11) | $T_{SD\_hyst}$    |   | –          | 7          | –          | $^\circ\text{C}$ |
| Reset Temperature (Note 11)                                  | $T_R$             |   | $T_{RS}+1$ | $T_{RS}+7$ | –          | $^\circ\text{C}$ |
| Thermal Reset of CS_Fault (Note 11)                          | $T_{RCS}$         |   | 135        | –          | –          | $^\circ\text{C}$ |
| Delta T Temperature Limit (Note 11)                          | $T_{DELTA}$       | $T_J = -40^\circ\text{C}$ , $V_D = 13\text{ V}$                       | –          | 60         | –          | $^\circ\text{C}$ |
| DC Output Current Limit                                      | $I_{limH}$        | $V_D = 13\text{ V}$   | 9          | 18         | 27         | A                |
|  |                   | $4\text{ V} < V_D < 18\text{ V}$                                      | –          | –          | 27         | A                |
| Short Circuit Current Limit during Thermal Cycling (Note 11) | $I_{LIMTCycling}$ | $V_D = 13\text{ V}$<br>$T_R < T_J < T_{TSD}$                          | –          | 6          | –          | A                |
| Switch Off Output Clamp Voltage                              | $V_{OUT\_clamp}$  | $I_{OUT} = 0.2\text{ A}$ , $V_{IN} = 0\text{ V}$ , $L = 20\text{ mH}$ | $V_D - 41$ | $V_D - 46$ | $V_D - 52$ | V                |
| Overvoltage Protection                                       | $V_{OV}$          | $V_{IN} = 0\text{ V}$ , $I_D = 20\text{ mA}$                          | 41         | 46         | 52         | V                |
| Output Voltage Drop Limitation                               | $V_{DS\_ON}$      | $I_{OUT} = 0.07\text{ A}$   | –          | 20         | –          | mV               |

10. To ensure long term reliability during overload or short circuit conditions, protection and related diagnostic signals must be used together with a fitting hardware & software strategy. If the device operates under abnormal conditions, this hardware & software solution must limit the duration and number of activation cycles.

11. Not subjected to production testing.

**Table 10. OPEN-LOAD DETECTION** ( $7\text{ V} \leq V_D \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ )

| Rating  | Symbol           | Conditions  | Value |     |     | Unit          |
|---|------------------|---|-------|-----|-----|---------------|
|   |                  |   | Min   | Typ | Max |               |
| Open-load Off State Detection Threshold               | $V_{OL}$         | $V_{IN} = 0\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$                                   | 2     | –   | 4   | V             |
| Open-load Detection Delay at Turn Off                 | $t_{d\_OL\_off}$ |   | 100   | 350 | 850 | $\mu\text{s}$ |
| Off State Output Current                              | $I_{OLOFF1}$     | $V_{IN} = 0\text{ V}$ , $V_{OUT} = V_{OL}$  | –3    | –   | 3   | $\mu\text{A}$ |
| Output rising edge to CS rising edge during open load | $t_{d\_OL}$      | $V_{OUT} = 4\text{ V}$ , $V_{IN} = 0\text{ V}$<br>$V_{CS} = 90\%$ of $V_{CS\_High}$ | –     | 5   | 30  | $\mu\text{s}$ |

**Table 11. CURRENT SENSE CHARACTERISTICS** ( $7\text{ V} \leq V_D \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ )

| Rating   | Symbol                 | Conditions  | Value |     |     | Unit          |
|--|------------------------|---|-------|-----|-----|---------------|
|  |                        |   | Min   | Typ | Max |               |
| Current Sense Ratio                                | $K_0$                  | $I_{OUT} = 0.010\text{ A}$ , $V_{CS} = 0.5\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | 350   | –   | 930 |               |
| Current Sense Ratio                                | $K_1$                  | $I_{OUT} = 0.025\text{ A}$ , $V_{CS} = 0.5\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | 350   | 600 | 880 |               |
| Current Sense Ratio Drift (Note 13)                | $\Delta K_1 / K_1$     | $I_{OUT} = 0.025\text{ A}$ , $V_{CS} = 0.5\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | –25   | –   | 15  | %             |
| Current Sense Ratio                                | $K_2$                  | $I_{OUT} = 0.07\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$   | 350   | 570 | 800 |               |
| Current Sense Ratio Drift (Note 13)                | $\Delta K_2 / K_2$     | $I_{OUT} = 0.07\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$   | –20   | –   | 10  | %             |
| Current Sense Ratio                                | $K_3$                  | $I_{OUT} = 0.15\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$   | 350   | 570 | 755 |               |
| Current Sense Ratio Drift (Note 13)                | $\Delta K_3 / K_3$     | $I_{OUT} = 0.15\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$   | –15   | –   | 10  | %             |
| Current Sense Ratio                                | $K_4$                  | $I_{OUT} = 0.7\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | 450   | 570 | 650 |               |
| Current Sense Ratio Drift (Note 13)                | $\Delta K_4 / K_4$     | $I_{OUT} = 0.7\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | –10   | –   | 10  | %             |
| Current Sense Ratio                                | $K_5$                  | $I_{OUT} = 2\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | 515   | 570 | 600 |               |
| Current Sense Ratio Drift (Note 13)                | $\Delta K_5 / K_5$     | $I_{OUT} = 2\text{ A}$ , $V_{CS} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$  | –5    | –   | 5   | %             |
| Current Sense Leakage Current                      | $CS_{Ilkg}$            | $I_{OUT} = 0\text{ A}$ , $V_{CS} = 0\text{ V}$<br>$V_{CS\_EN} = 5\text{ V}$ , $V_{IN} = 0\text{ V}$                               | –     | –   | 1   | $\mu\text{A}$ |
|  |                        | $I_{OUT} = 0\text{ A}$ , $V_{CS} = 0\text{ V}$<br>$V_{CS\_EN} = 5\text{ V}$ , $V_{IN} = 5\text{ V}$                               | –     | –   | 2   |               |
|  |                        | $I_{OUT} = 2\text{ A}$ , $V_{CS} = 0\text{ V}$<br>$V_{CS\_EN} = 0\text{ V}$ , $V_{IN} = 5\text{ V}$                               | –     | –   | 0.5 |               |
| CS Max Voltage                                     | $CS_{Max}$             | $V_D = 7\text{ V}$ , $V_{IN} = 5\text{ V}$ , $R_{CS} = 10\text{ k}\Omega$ ,<br>$I_{OUT} = 2\text{ A}$ , $V_{CS\_EN} = 5\text{ V}$ | 5     | –   | 7   | V             |
| Current Sense Voltage in Fault Condition (Note 12) | $V_{CS\_fault}$        | $V_D = 13\text{ V}$ , $V_{IN} = 0\text{ V}$ , $R_{CS} = 1\text{ k}\Omega$ ,<br>$V_{OUT} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$ | –     | 10  | –   | V             |
| Current Sense Current in Fault Condition (Note 12) | $I_{CS\_fault}$        | $V_D = 13\text{ V}$ , $V_{CS} = 5\text{ V}$ , $V_{IN} = 0\text{ V}$ ,<br>$V_{OUT} = 4\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$       | 7     | 20  | 30  | mA            |
| Output Saturation Current (Note 13)                | $I_{OUT\_sat}$         | $V_D = 7\text{ V}$ , $V_{CS} = 4\text{ V}$ , $V_{IN} = 5\text{ V}$ ,<br>$T_J = 150^\circ\text{C}$ , $V_{CS\_EN} = 5\text{ V}$     | 2.4   | –   | –   | A             |
| CS_EN High to CS High Delay Time                   | $t_{CS\_High1}$        | $V_{IN} = 5\text{ V}$ , $V_{CS\_EN} = 0\text{ to }5\text{ V}$ ,<br>$R_{CS} = 1\text{ k}\Omega$ , $R_L = 6.5\text{ }\Omega$        | –     | –   | 100 | $\mu\text{s}$ |
| CS_EN Low to CS Low Delay Time                     | $t_{CS\_Low1}$         | $V_{IN} = 5\text{ V}$ , $V_{CS\_EN} = 5\text{ to }0\text{ V}$ ,<br>$R_{CS} = 1\text{ k}\Omega$ , $R_L = 6.5\text{ }\Omega$        | –     | 5   | 25  | $\mu\text{s}$ |
| $V_{in}$ High to CS High Delay Time                | $t_{CS\_High2}$        | $V_{IN} = 0\text{ to }5\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$ ,<br>$R_{CS} = 1\text{ k}\Omega$ , $R_L = 6.5\text{ }\Omega$        | –     | 100 | 250 | $\mu\text{s}$ |
| $V_{in}$ Low to CS Low Delay Time                  | $t_{CS\_Low2}$         | $V_{IN} = 5\text{ to }0\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$ ,<br>$R_{CS} = 1\text{ k}\Omega$ , $R_L = 6.5\text{ }\Omega$        | –     | 50  | 250 | $\mu\text{s}$ |
| Delay Time $I_D$ Rising Edge to Rising Edge of CS  | $\Delta t_{CS\_High2}$ | $V_{IN} = 5\text{ V}$ , $V_{CS\_EN} = 5\text{ V}$<br>$R_{CS} = 1\text{ k}\Omega$ , $I_{CS} = 90\%$ of $I_{CS\_Max}$               | –     | –   | 100 | $\mu\text{s}$ |

12. The following fault conditions included are: Over-temperature, Power Limitation, and OFF State Open-Load Detection.

13. Not subjected to production testing. For more information, refer to the AND9733–D Application Note.

Table 12. TRUTH TABLE

| Conditions              | Input  | Output  | CS ( $V_{CS\_EN} = 5\text{ V}$ ) (Note 14)        |
|-------------------------|--------|---|---|
| Normal Operation        | L<br>H | L<br>H  | 0<br>$I_{CS} = I_{OUT}/K_{NOMINAL}$               |
| Overtemperature         | L<br>H | L<br>L  | 0<br>$V_{CS\_fault}$                              |
| Undervoltage            | L<br>H | L<br>L  | 0<br>0  |
| Overload                | H<br>H | H (no active current mgmt)<br>Cycling (active current mgmt) | $I_{CS} = I_{OUT}/K_{NOMINAL}$<br>$V_{CS\_fault}$ |
| Short circuit to Ground | L<br>H | L<br>L  | 0<br>$V_{CS\_fault}$                              |
| OFF State Open Load     | L      | H   | $V_{CS\_fault}$                                   |

14. If  $V_{CS\_EN}$  is low, the Current Sense output is at a high impedance, its potential depends on leakage currents and external circuitry.



# WAVEFORMS AND GRAPHS

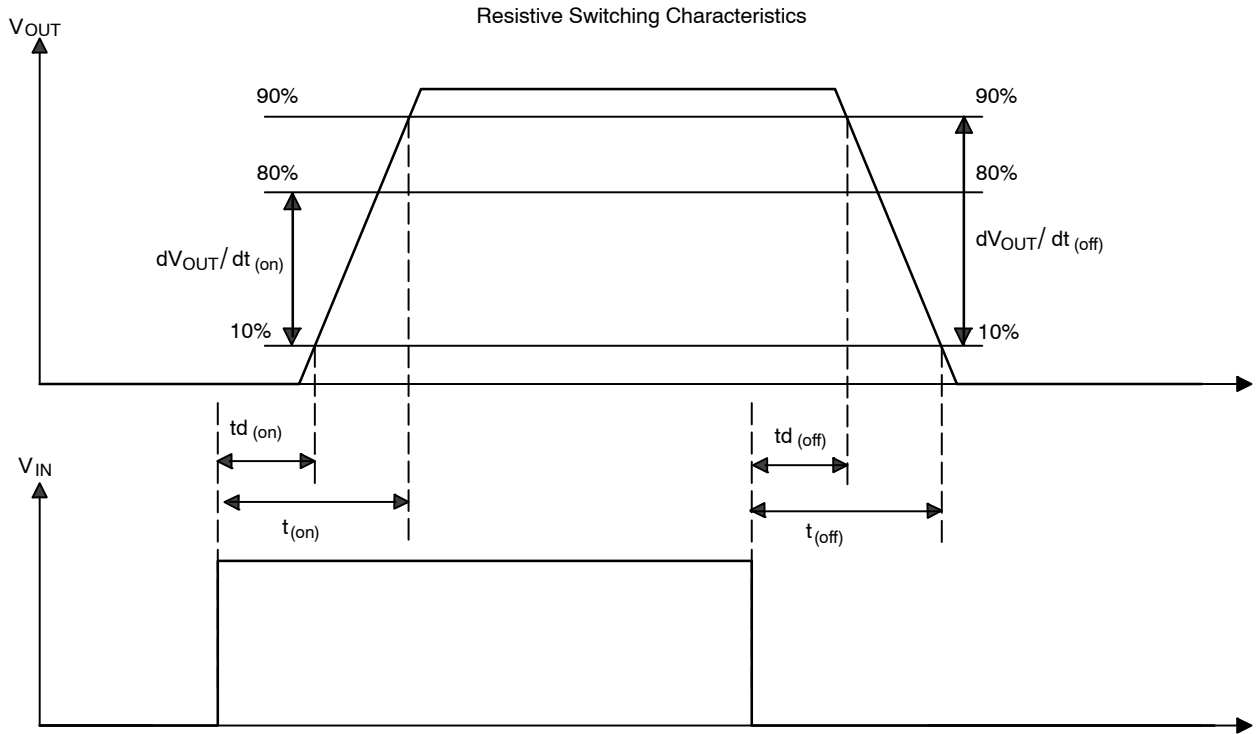


Figure 4. Switching Characteristics

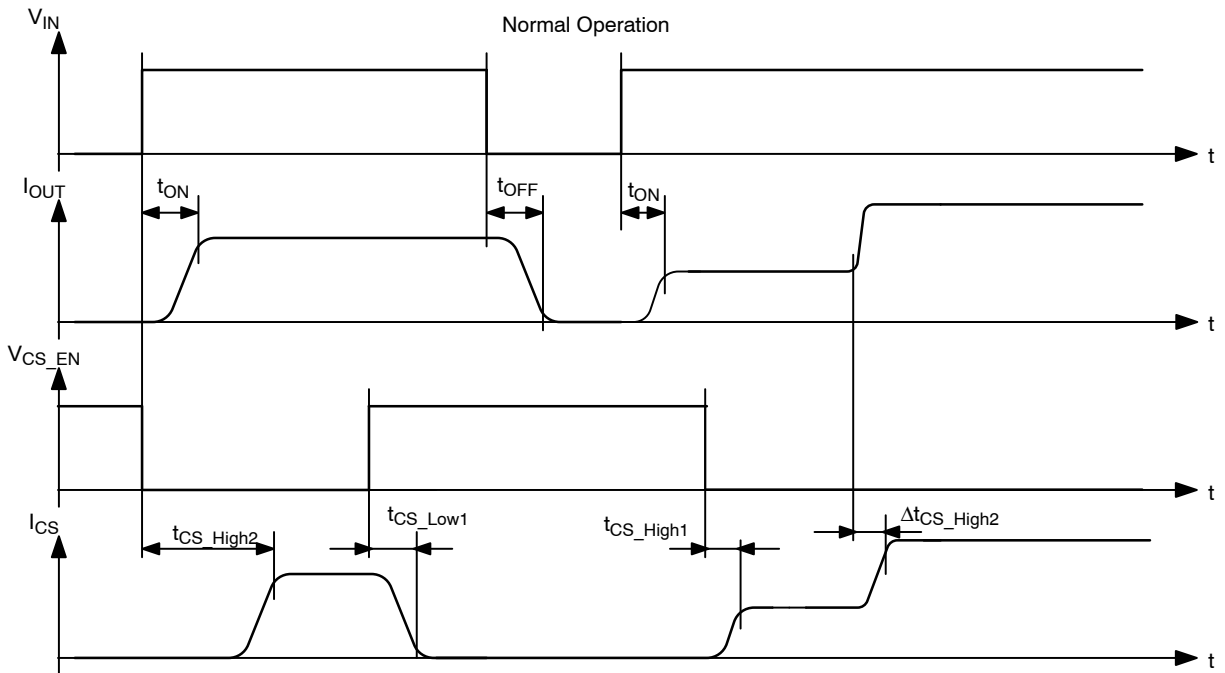


Figure 5. Normal Operation with Current Sense Timing Characteristics

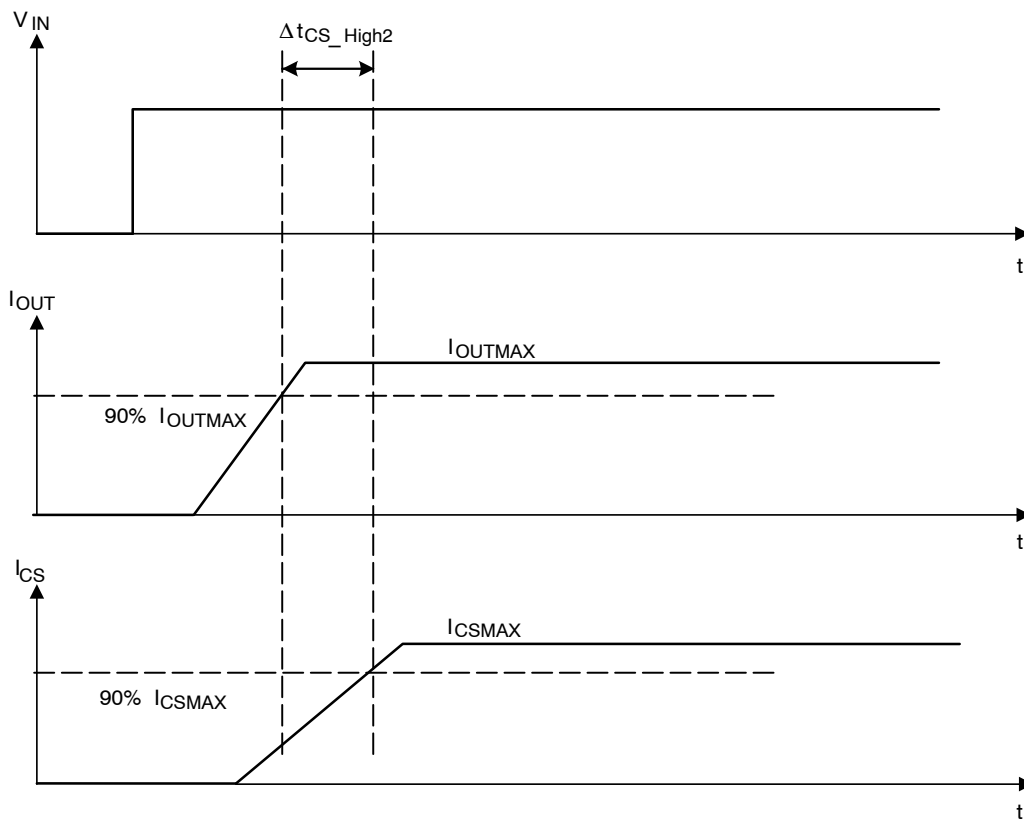


Figure 6. Delay Response from Rising Edge of  $I_{OUT}$  and Rising Edge of CS (for  $CS_{EN} = 5\text{ V}$ )

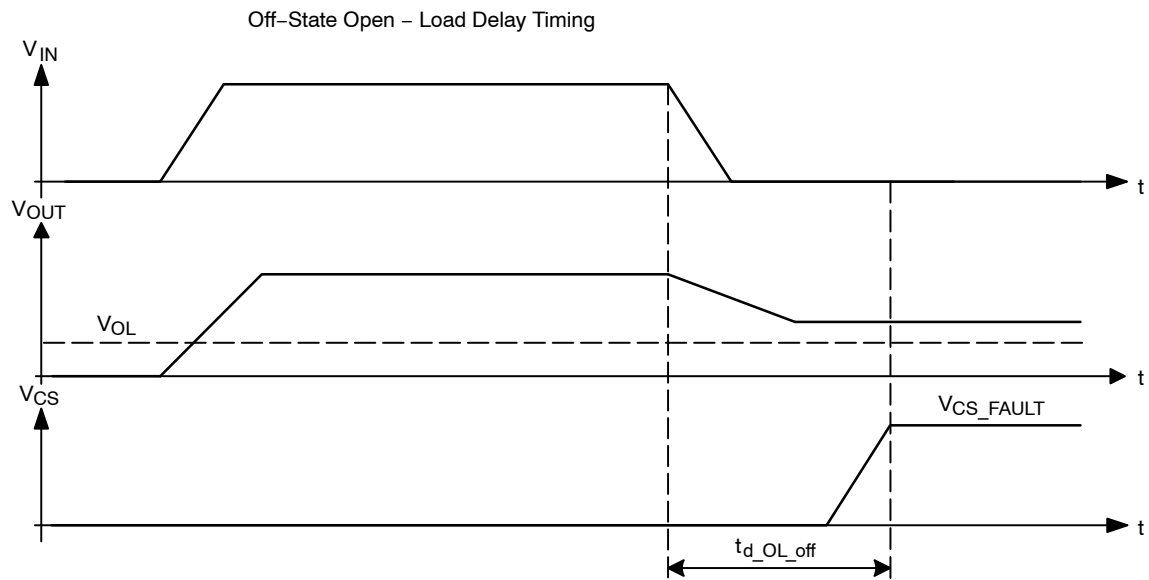


Figure 7. OFF-State Open-Load Flag Delay Timing

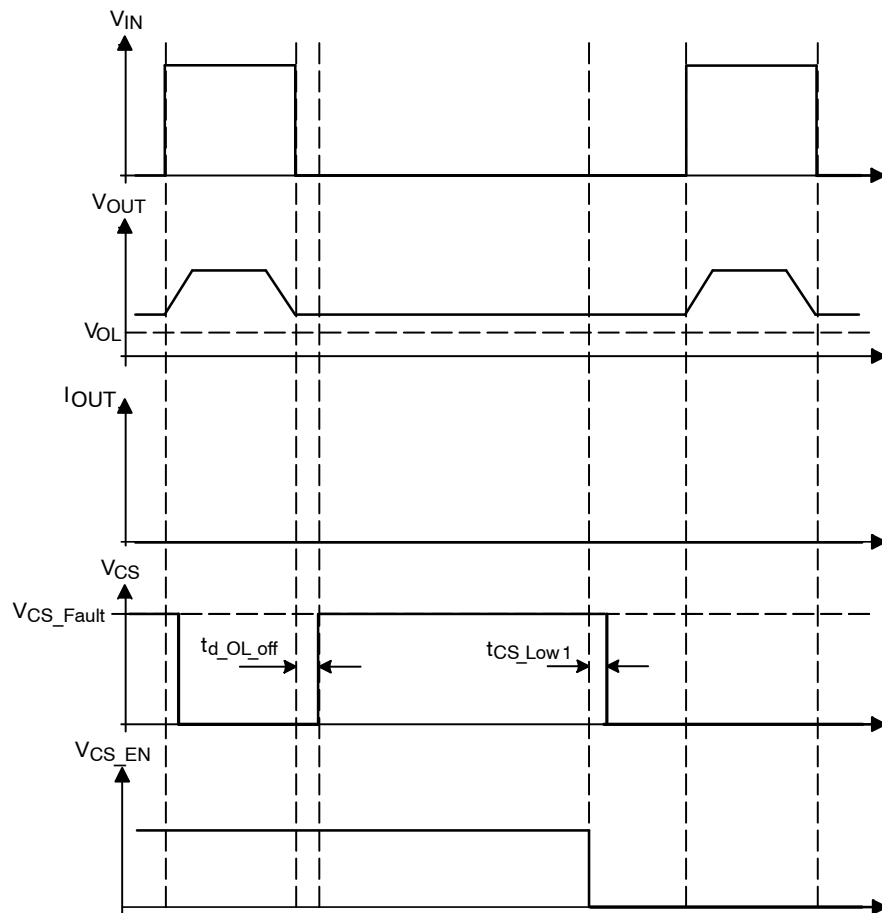


Figure 8. Off-State Open-Load with Added External Components

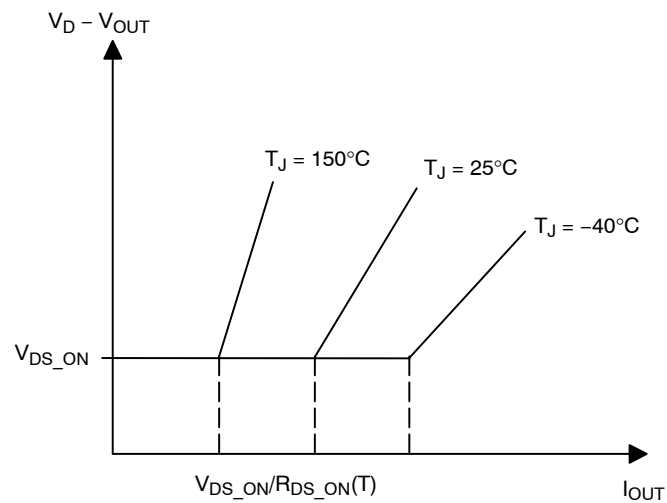


Figure 9. Voltage Drop Limitation for V<sub>DS\_ON</sub>

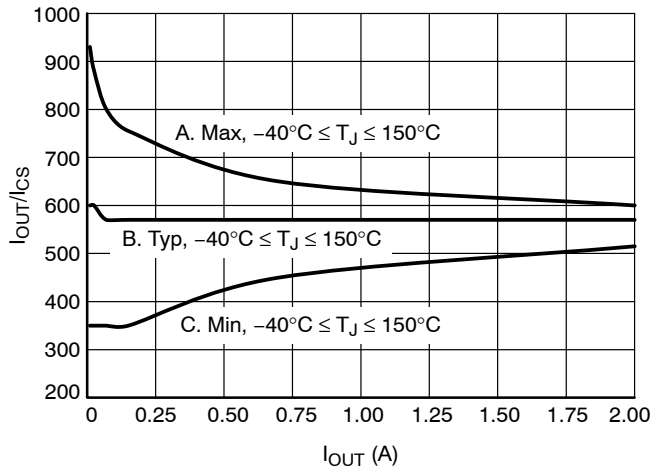


Figure 10.  $I_{OUT}/I_{CS}$  vs.  $I_{OUT}$

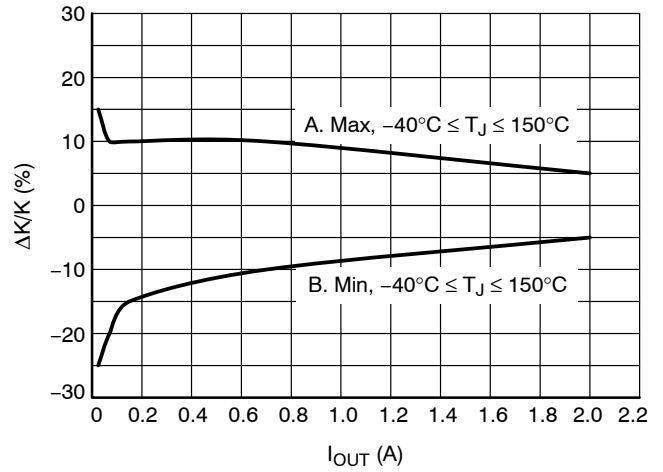


Figure 11. Current Sense Ratio Drift vs. Load Current

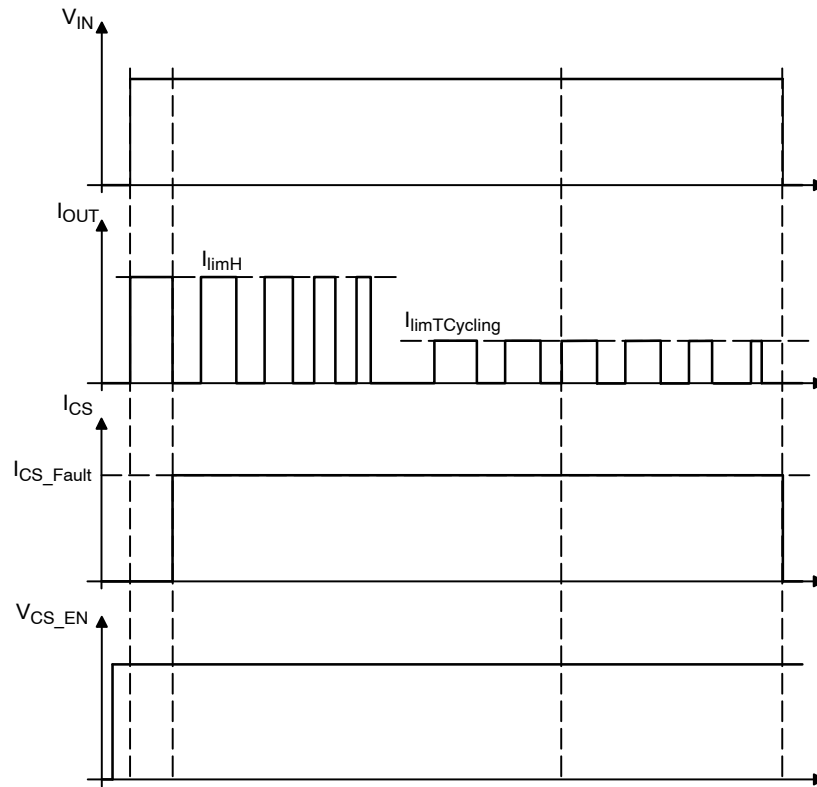


Figure 12. Short to GND or Overload

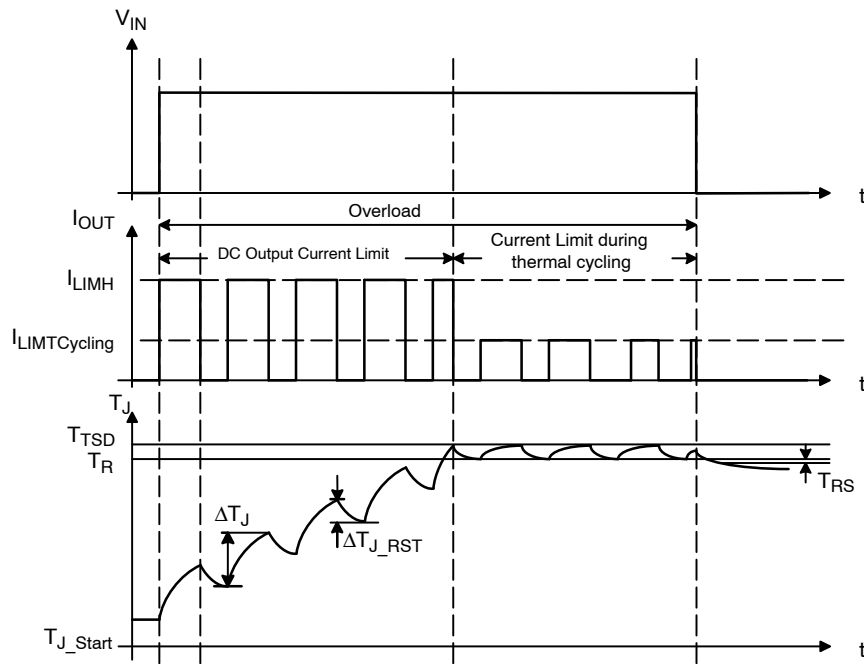


Figure 13. How  $T_j$  progresses During Short to GND or Overload

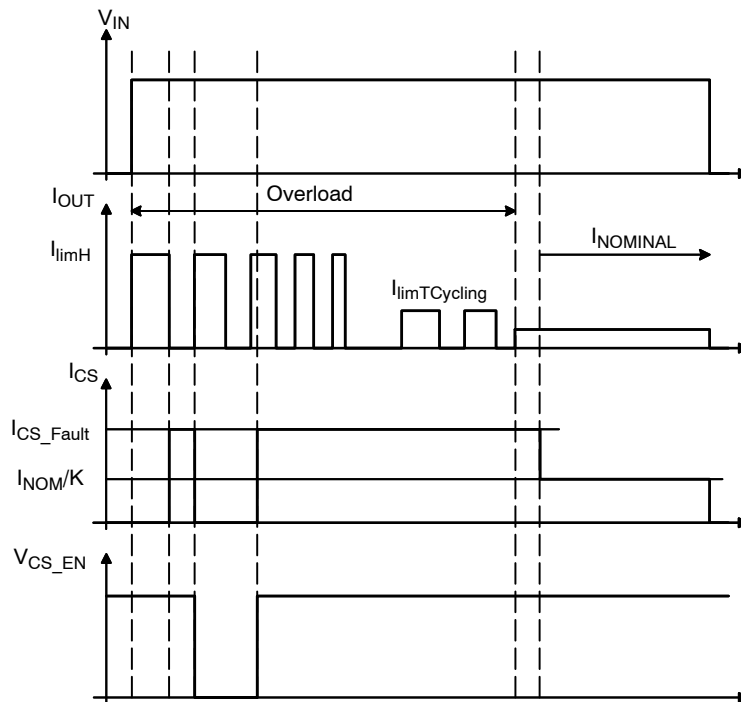


Figure 14. Discontinuous Overload or Short to GND

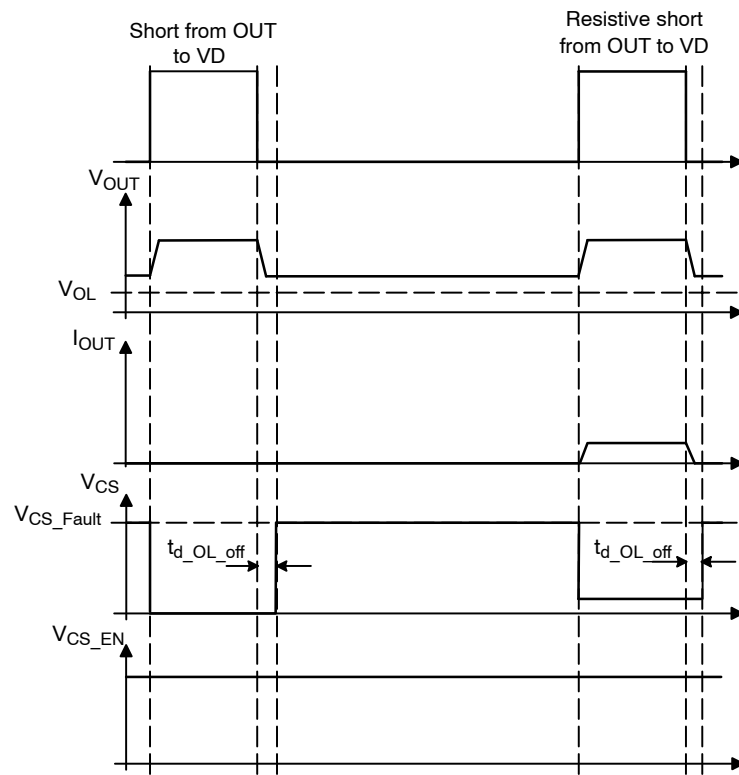


Figure 15. Short Circuit from OUT to  $V_D$

TYPICAL CHARACTERISTICS

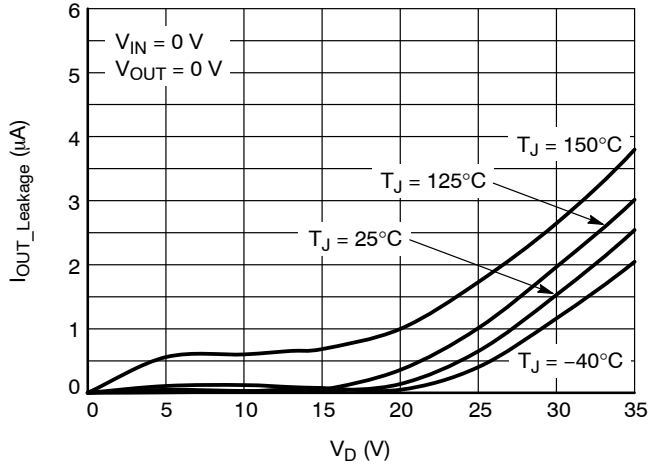


Figure 16. Output Leakage Current vs.  $V_D$

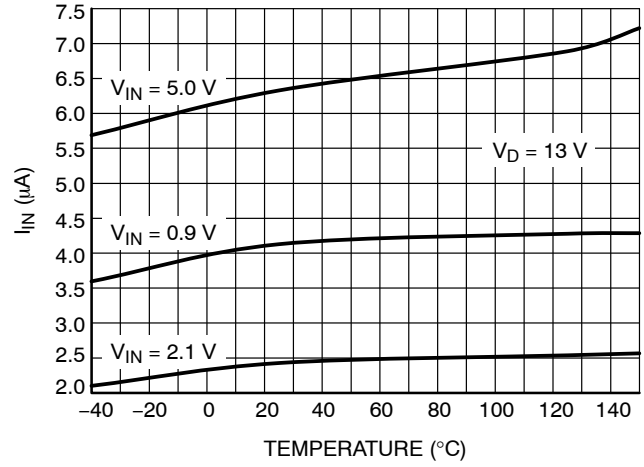


Figure 17. Input Current vs. Temperature

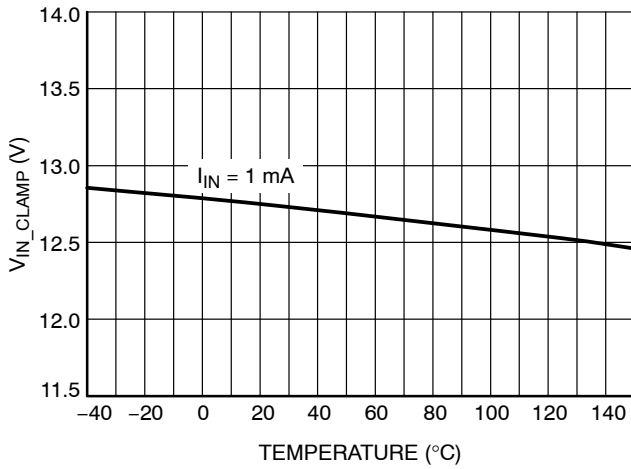


Figure 18. Input Clamp Voltage (Positive) vs. Temperature

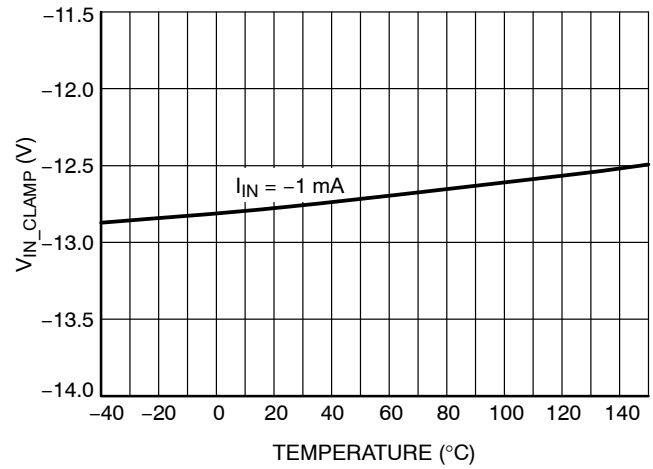


Figure 19. Input Clamp Voltage (Negative) vs. Temperature

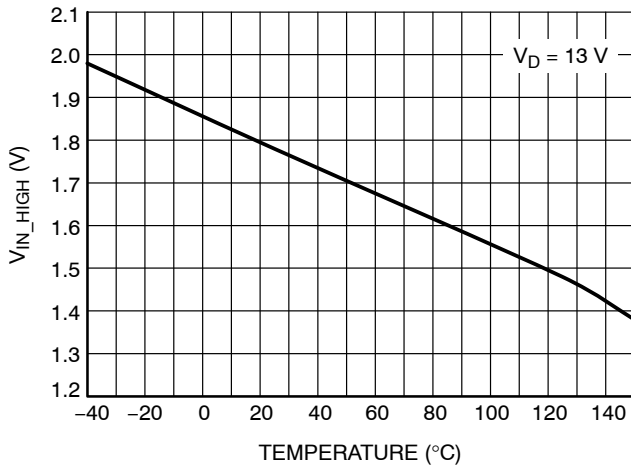


Figure 20.  $V_{IN}$  Threshold High vs. Temperature

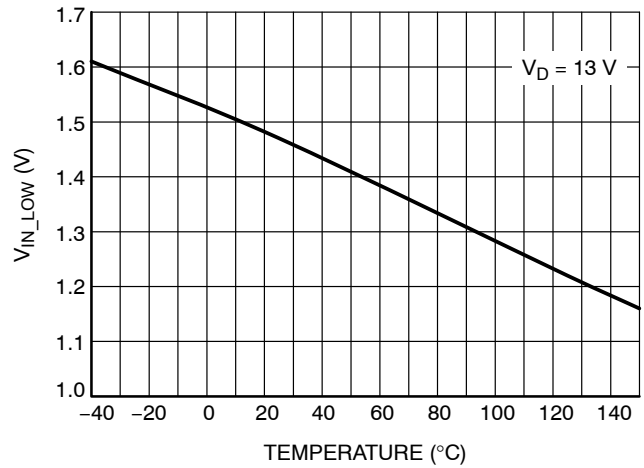


Figure 21.  $V_{IN}$  Threshold Low vs. Temperature

TYPICAL CHARACTERISTICS

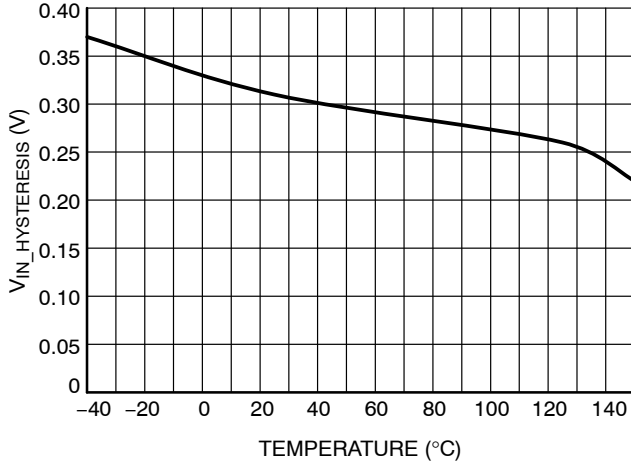


Figure 22. Hysteresis Input Voltage vs. Temperature

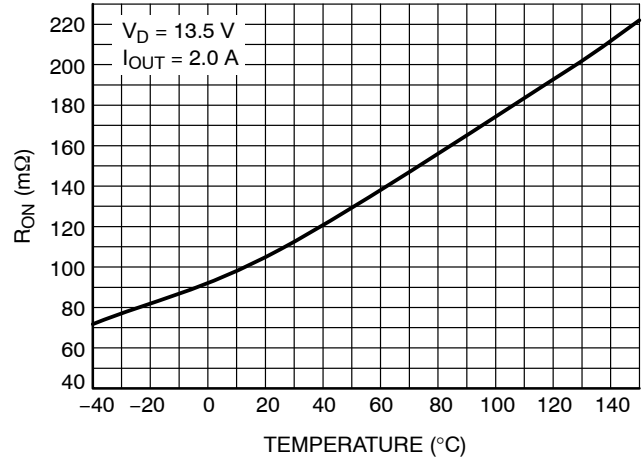


Figure 23. R<sub>ON</sub> vs. Temperature

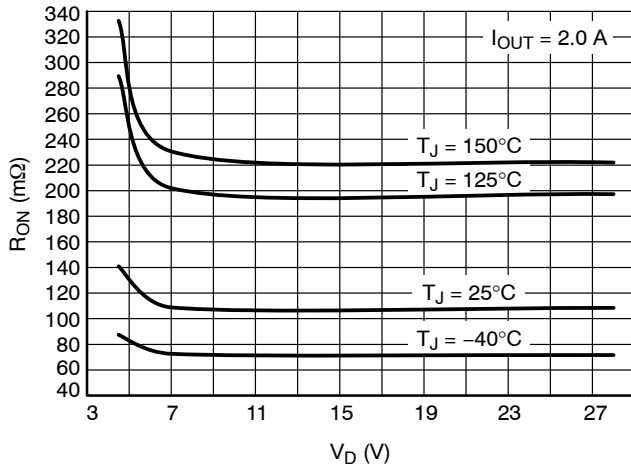


Figure 24. R<sub>ON</sub> vs. V<sub>D</sub> Voltage

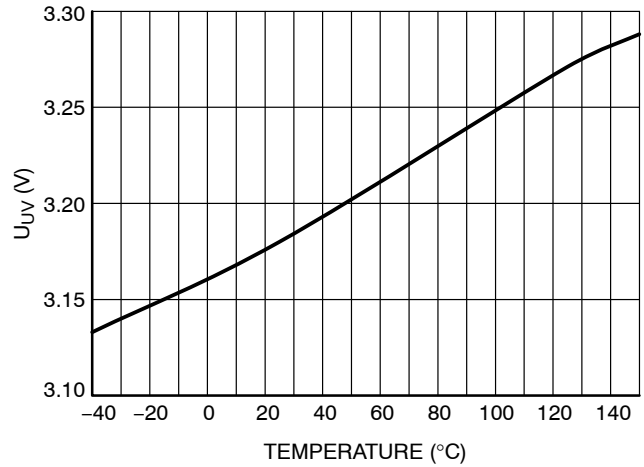


Figure 25. Undervoltage Shutdown vs. Temperature

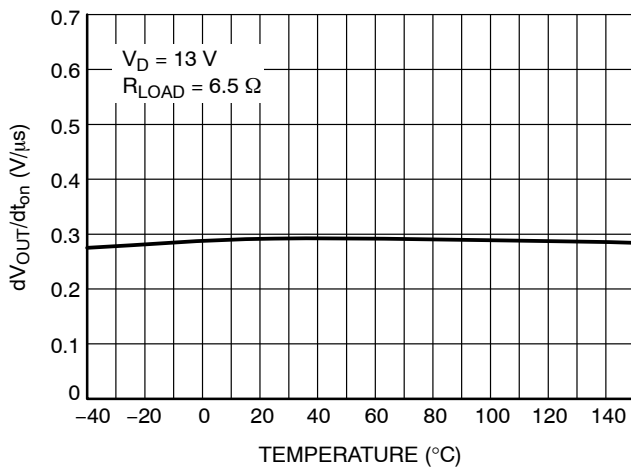


Figure 26. Slew Rate ON vs. Temperature

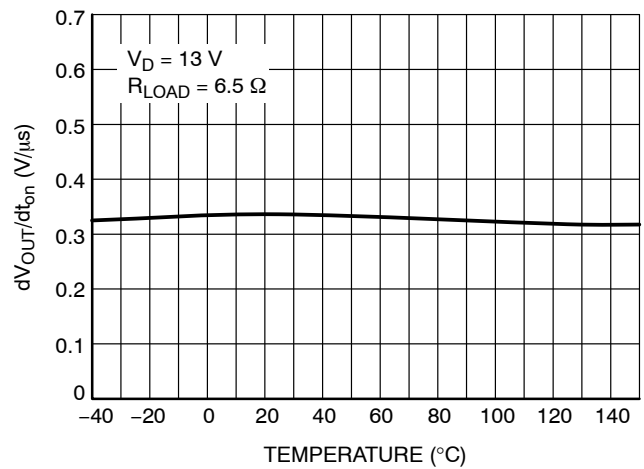


Figure 27. Slew Rate OFF vs. Temperature



TYPICAL CHARACTERISTICS

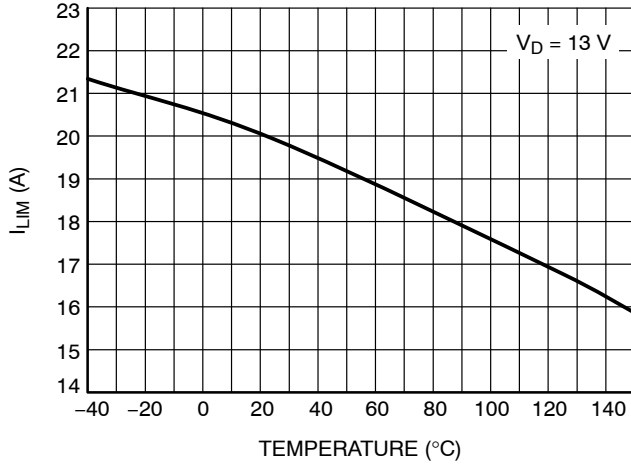


Figure 28. Current Limit vs. Temperature

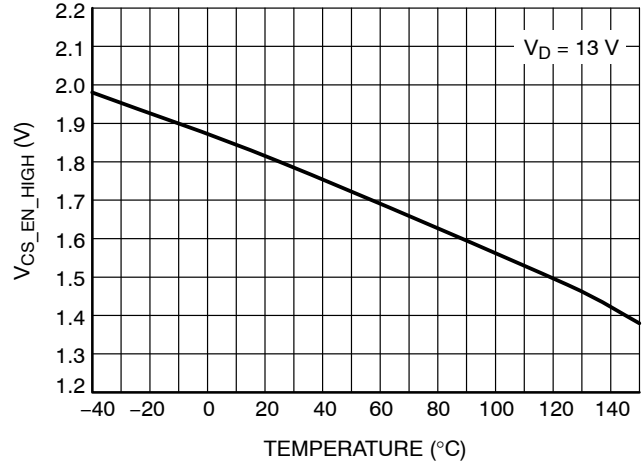


Figure 29. CS\_EN Threshold High vs. Temperature

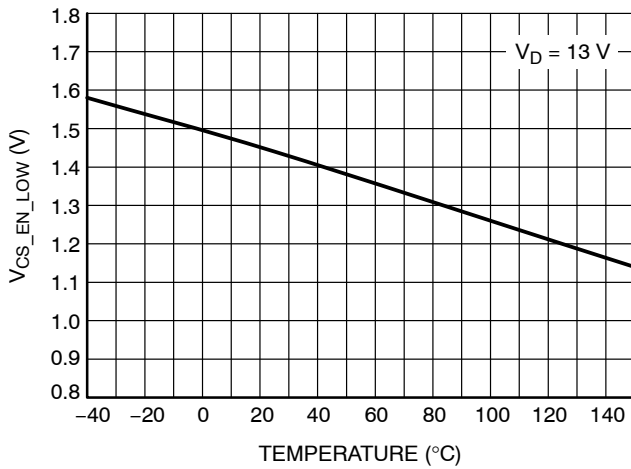


Figure 30. CS\_EN Threshold Low vs. Temperature

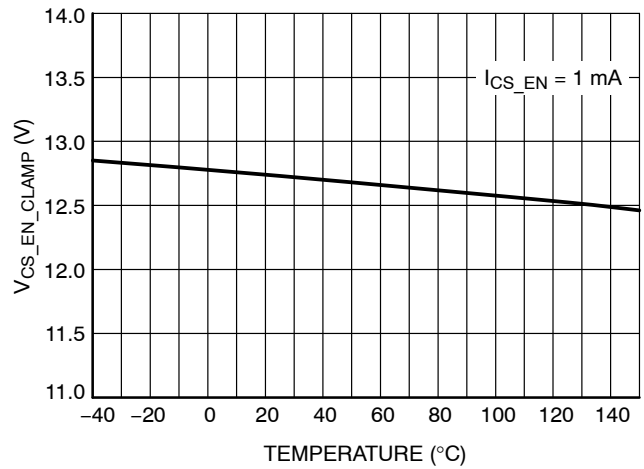


Figure 31. CS\_EN Clamp Voltage (Positive) vs. Temperature

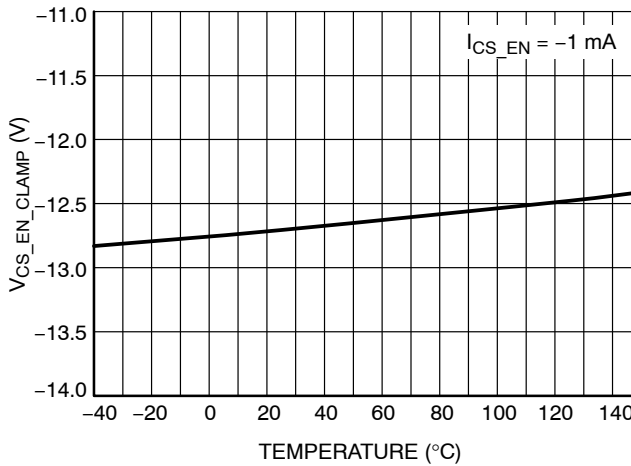


Figure 32. CS\_EN Clamp Voltage (Negative) vs. Temperature

Table 13. ISO 7637-2: 2011(E) PULSE TEST RESULTS

| ISO<br>7637-2:2011(E)<br>Test Pulse | Test Severity Levels  |      | Delays and Impedance     | # of Pulses or Test Time | Pulse / Burst Rep. Time |
|-------------------------------------|---|------|--------------------------|--------------------------|-------------------------|
|                                     | III   | IV   |                          |                          |                         |
| 1                                   | -112  | -150 | 2 ms, 10 $\Omega$        | 500 pulses               | 0.5 s                   |
| 2a                                  | +55   | +112 | 0.05 ms, 2 $\Omega$      | 500 pulses               | 0.5 s                   |
| 3a                                  | -165  | -220 | 0.1 $\mu$ s, 50 $\Omega$ | 1 h                      | 100 ms                  |
| 3b                                  | +112  | +150 | 0.1 $\mu$ s, 50 $\Omega$ | 1 h                      | 100 ms                  |
|                                     |   |      |                          |                          |                         |
| ISO<br>7637-2:2011(E)<br>Test Pulse | Test Results  |      |                          |                          |                         |
|                                     | III   | IV   |                          |                          |                         |
| 1                                   |   | A    |                          |                          |                         |
| 2a                                  |   | C    |                          |                          |                         |
| 3a                                  |   | A    |                          |                          |                         |
| 3b                                  |   | A    |                          |                          |                         |
|                                     |   |      |                          |                          |                         |
| Class                               | Functional Status   |      |                          |                          |                         |
| A                                   | All functions of a device perform as designed during and after exposure to disturbance.   |      |                          |                          |                         |
| B                                   | All functions of a device perform as designed during exposure. However, one or more of them can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A. |      |                          |                          |                         |
| C                                   | One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.  |      |                          |                          |                         |
| D                                   | One or more functions of a device do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device is reset by simple "operator/use" action.   |      |                          |                          |                         |
| E                                   | One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.   |      |                          |                          |                         |

APPLICATION INFORMATION

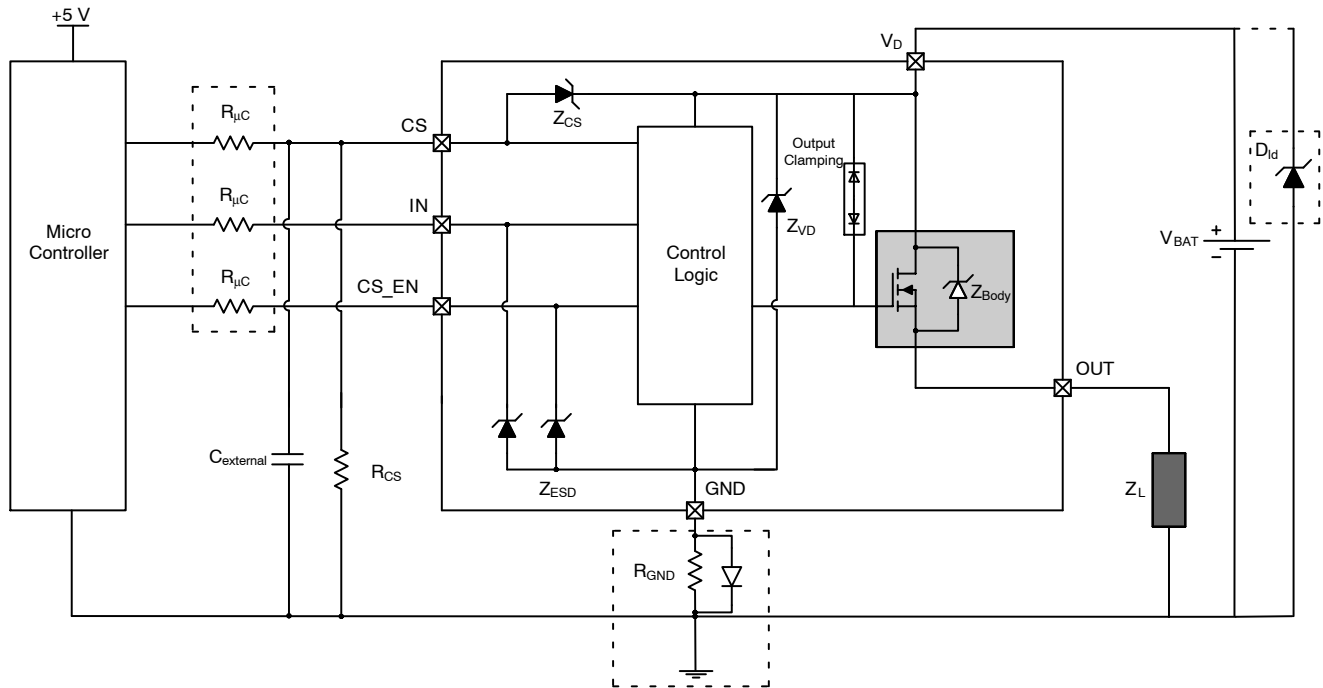


Figure 33. Application Schematic

### Loss of Ground Protection

When device or ECU ground connection is lost and load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Input resistors are recommended between the device and microcontroller.

### Undervoltage Protection

The device has two under-voltage threshold levels,  $V_{D\_MIN}$  and  $V_{UV}$ . Switching function (ON/OFF) requires supply voltage to be at least  $V_{D\_MIN}$ . The device features a lower supply threshold  $V_{UV}$ , above which the output can remain in ON state. While all protection functions are guaranteed when the switch is ON, diagnostic functions are operational only within nominal supply voltage range  $V_D$ .

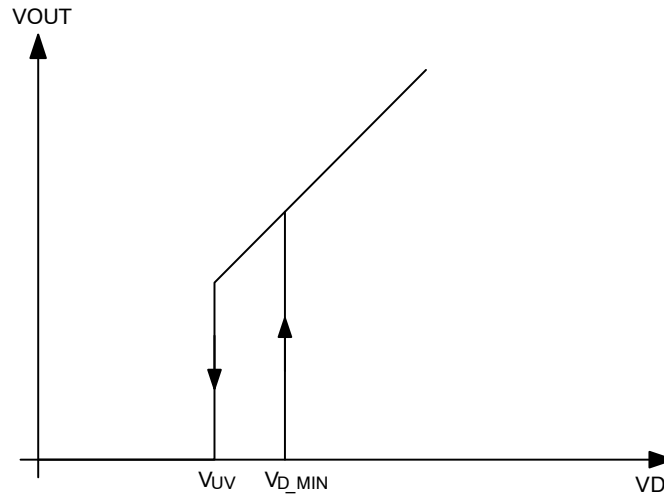


Figure 34. Undervoltage Behavior

### Overvoltage Protection

The NCV84120 has two Zener diodes  $Z_{VD}$  and  $Z_{CS}$ , which provide integrated overvoltage protection.  $Z_{VD}$  protects the logic block by clamping the voltage between supply pin  $V_D$  and ground pin GND to  $V_{ZVD}$ .  $Z_{CS}$  limits voltage at current sense pin CS to  $V_D - V_{ZCS}$ . The output power MOSFET's output clamping diodes provide protection by clamping the voltage across the MOSFET (between  $V_D$  pin and OUT pin) to  $V_{CLAMP}$ . During overvoltage protection, current flowing through  $Z_{VD}$ ,  $Z_{CS}$  and the output clamp must be limited. Load impedance  $Z_L$  limits the current in the body diode  $Z_{Body}$ . In order to limit the current in  $Z_{VD}$  a resistor,  $R_{GND}$  (150  $\Omega$ ), is required in the GND path. External resistors  $R_{CS}$  and  $R_{SENSE}$  limit the

current flowing through  $Z_{CS}$  and out of the CS pin into the micro-controller I/O pin. With  $R_{GND}$ , the GND pin voltage is elevated to  $V_D - V_{ZVD}$  when the supply voltage  $V_D$  rises above  $V_{ZVD}$ . ESD diodes  $Z_{ESD}$  pull up the voltage at logic pins IN, CS\_EN close to the GND pin voltage  $V_D - V_{ZVD}$ . External resistors  $R_{IN}$ , and  $R_{CS\_EN}$  are required to limit the current flowing out of the logic pins into the micro-controller I/O pins. During overvoltage exposure, the device transitions into a self-protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The specified parameters as well as short circuit robustness and energy capability cannot be guaranteed during overvoltage exposure.

## Reverse Battery Protection

*Solution 1: Resistor in the GND line only  
(no parallel Diode)*

The following calculations are true for any type of load.

In the case for no diode in parallel with  $R_{GND}$ , the calculations below explain how to size the resistor.

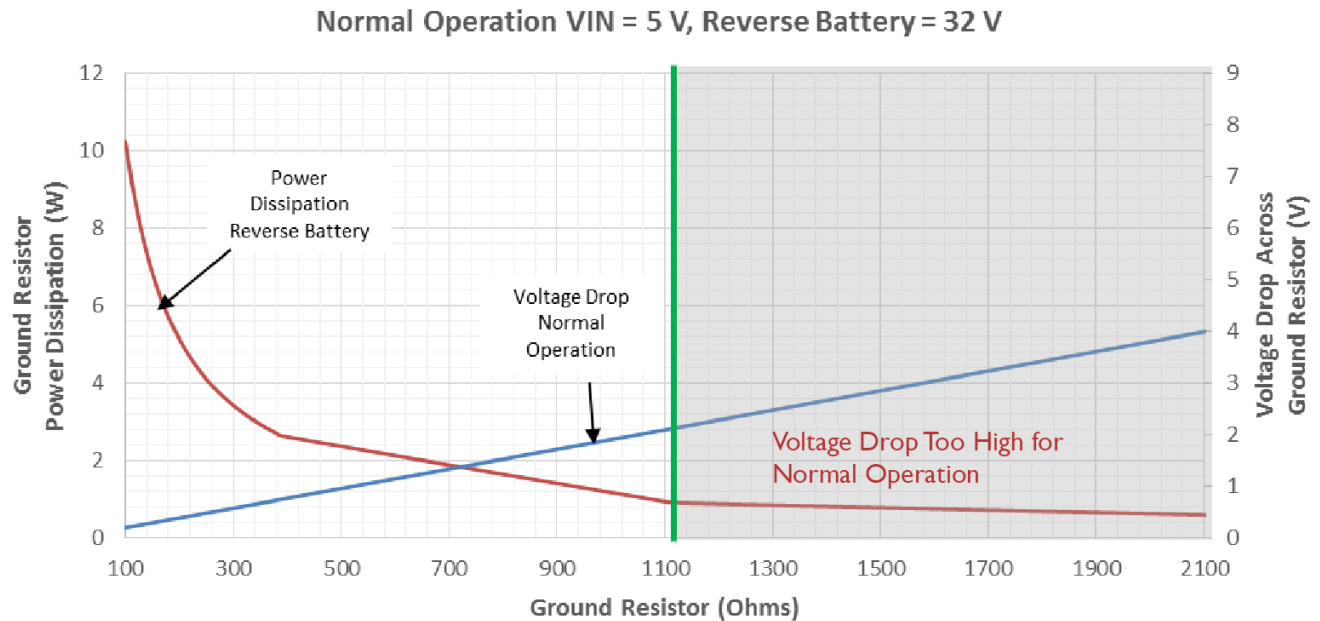
Consider the following parameters:

$-I_{GND}$  Maximum = 200 mA for up to  $-V_D = 32$  V.

Where  $-I_{GND}$  is the DC reverse current through the GND pin and  $-V_D$  is the DC reverse battery voltage.

$$-I_{GND} = \frac{-V_D}{R_{GND}} \quad (\text{eq. 1})$$

Since this resistor can be used amongst multiple High-Side devices, please take note the sum of the maximum active GND currents ( $I_{GND(On)max}$ ) for each device when sizing the resistor. Please note that if the microprocessor GND is not shared by the device GND, then  $R_{GND}$  produces a shift of ( $I_{GND(On)max} \times R_{GND}$ ) in the input thresholds and CS output values. If the calculated power dissipation leads to too large of a resistor size or several devices have to share the same resistor, please look at the second solution for Reverse Battery Protection. Refer to Figure 34 for selecting the proper  $R_{GND}$ .



**Figure 35. Reverse Battery  $R_{GND}$  Considerations**

### Overload Protection

Current limitation as well as overtemperature shutdown mechanisms are integrated into NCV84120 to provide protection from overload conditions such as bulb inrush or short to ground.

### Current Limitation

In case of overload, NCV84120 limits the current in the output power MOSFET to a safe value. Due to high power dissipation during current limitation, the device's junction temperature increases rapidly. In order to protect the device, the output driver is shut down by one of the two overtemperature protection mechanisms. The output current limit is dependent on the device temperature, and will fold back once the die reaches thermal shutdown. If the input remains active during the shutdown, the output power

MOSFET will automatically be re-activated after a minimum OFF time or when the junction temperature returns to a safe level.

### Output Clamping with Inductive Load Switch Off

The output voltage  $V_{OUT}$  drops below GND potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integrated clamp of the device clamps the negative output voltage to a certain level relative to the supply voltage  $V_{BAT}$ . During output clamping with inductive load switch off, the energy stored in the inductance is rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

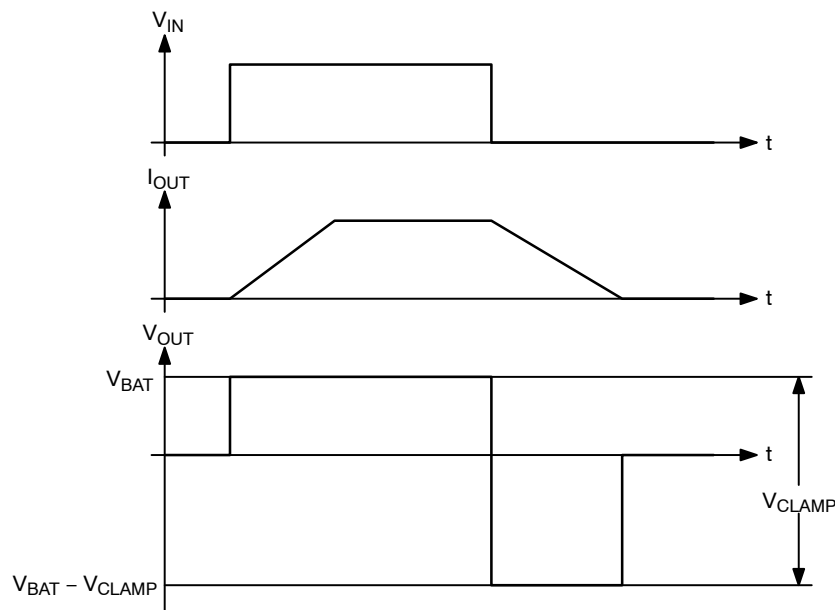


Figure 36. Inductive Load Switching

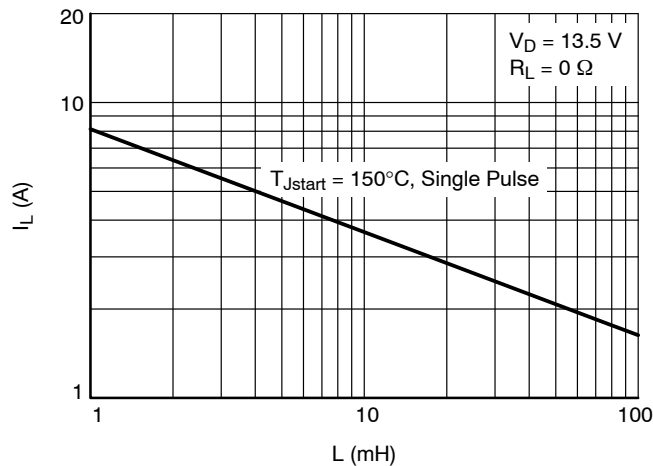


Figure 37. Maximum Switch-Off Current vs. Load Inductance,  $V_D = 13.5 \text{ V}$ ;  $R_L = 0 \text{ } \Omega$

**Inverse Current:**

When the output voltage  $V_{OUT}$  rises above the supply voltage  $V_D$ , the output power MOSFET's integral body diode will be forward biased causing a current flow from the OUT pin to the  $V_D$  pin. The device does not provide any protection function such as current limitation or overtemperature shutdown.

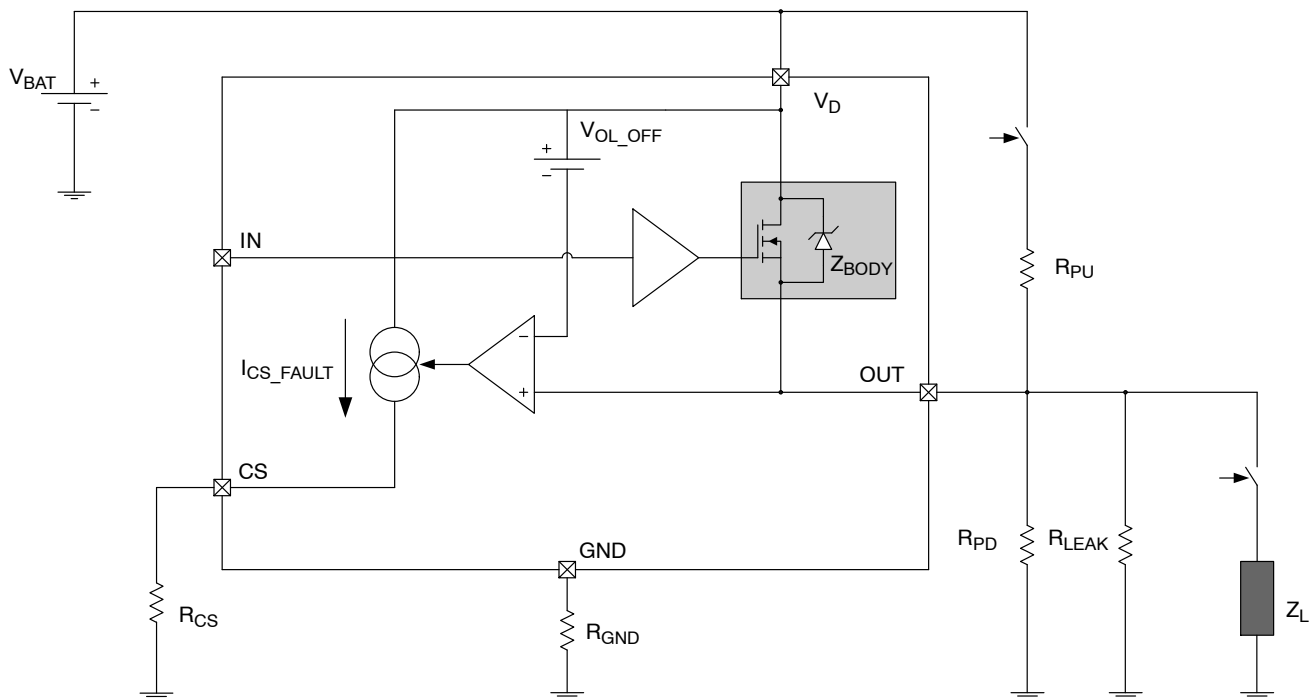
## Underload Detection in ON State

An underload condition in ON state is indicated by reducing the sense output current to a very minimal current. In order to detect an underload condition, NCV84090 performs a real-time monitoring of the load current. In case the output current falls below a specified threshold level

( $I_{OL}$ ), the current sense output current is reduced to a very low value ( $I_{OL}$ ). This mechanism helps to overcome a high absolute tolerance of the current sense signal at very low load current and to implement an accurate underload detection threshold.

### Open Load Detection in OFF State

Open load diagnosis in OFF state can be performed by activating an external resistive pull-up path ( $R_{PU}$ ) to  $V_{BAT}$ . To calculate the pull-up resistance, external leakage currents (designed pull-down resistance, humidity-induced leakage etc) as well as the open load threshold voltage  $V_{OL}$  have to be taken into account.



### Figure 38. Off State Open Load Detection Circuit

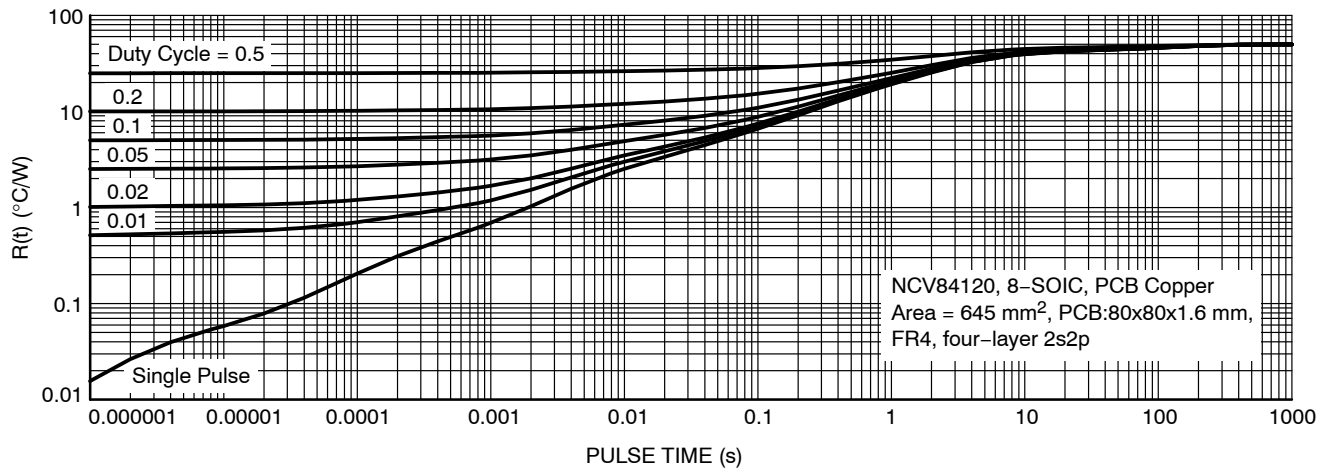
### Current Sense in PWM Mode

When operating in PWM mode, the current sense functionality can be used, but the timing of the input signal and the response time of the current sense need to be considered. When operating in PWM mode, the following performance is to be expected. The CS\_EN pin should be held high to eliminate any unnecessary delay time to the

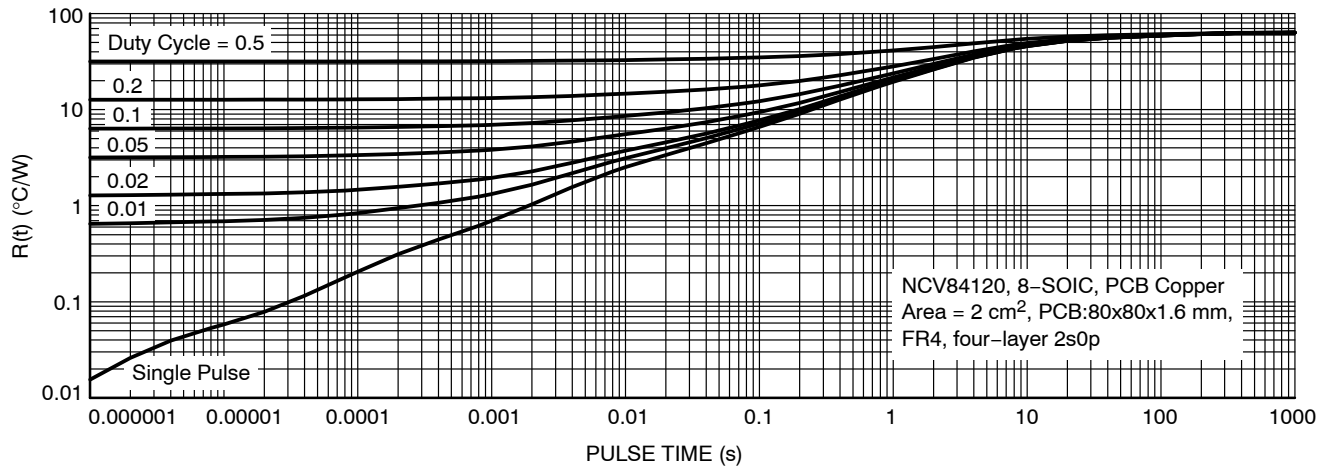
circuit. When  $V_{IN}$  switches from low to high, there will be a typical delay ( $t_{CS\_High2}$ ) before the current sense responds. Once this timing delay has passed, the rise time of the current sense output ( $\Delta t_{CS\_High2}$ ) also needs to be considered. When  $V_{IN}$  switches from high to low a delay time ( $t_{CS\_Low1}$ ) needs to be considered. As long as these timing delays are allowed, the current sense pin can be operated in PWM mode.

# NCV84120

## PACKAGE AND PCB THERMAL DATA



**Figure 39. Junction to Ambient Transient Thermal Impedance (Min Pad Cu Area)**



**Figure 40. Junction to Ambient Transient Thermal Impedance (2 cm<sup>2</sup> Cu Area)**





SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER   | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE   |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE   | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE  | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND  | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1   | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN   |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN  | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN   | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC  | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE   | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1   | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6  | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT   | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC  | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN  | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN  |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |  |  |

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