

Self-Protected Low Side Driver with In-Rush Current Management

NCV8411

The NCV8411 is a three terminal protected Low-Side Smart Discrete FET. The protection features include Delta Thermal Shutdown, overcurrent, overtemperature, ESD and integrated Drain to Gate clamping for over voltage protection. The device also offers fault indication via the gate pin. This device is suitable for harsh automotive environments.

Features

- Short Circuit Protection with In-Rush Current Management
- Delta Thermal Shutdown
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Over Voltage Protection and Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

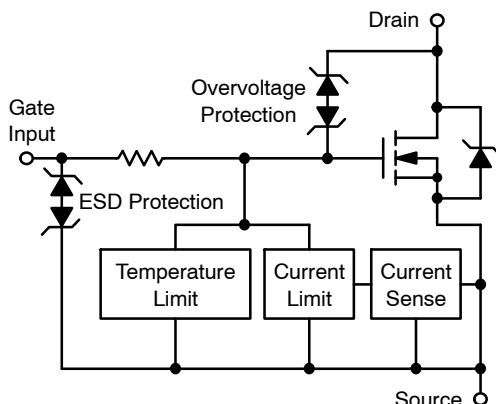


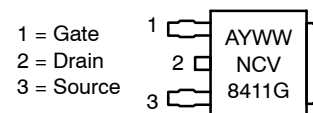
Figure 1. Block Diagram

V_{DS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
42 V	23 mΩ @ 10 V	45 A



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV8411DTRKG	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value (min)	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	42	V
Drain-to-Gate Voltage Internally Clamped	V_{DG}	42	V
Gate-to-Source Voltage	V_{GS}	± 14	V
Drain Current – Continuous	I_D	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	1.3 2.7	W
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R_{thJC} R_{thJA} R_{thJA}	0.65 95 45	$^\circ\text{C/W}$
Single Pulse Inductive Load Switching Energy (Note 3) ($L = 120\text{ mH}$, $T_{J(\text{start})} = 150^\circ\text{C}$)	E_{AS}	600	mJ
Load Dump Voltage ($V_{GS} = 0$ and 10 V , $R_G = 2\ \Omega$, $R_L = 3\ \Omega$) (Note 4)	U_S^*	55	V
Operating Junction Temperature	T_J	-40 to 150	$^\circ\text{C}$
Storage Temperature	T_{storage}	-55 to 150	$^\circ\text{C}$

ESD CHARACTERISTICS (Note 3)

Electro-Static Discharge Capability Human Body Model (HBM)	ESD	4	kV
---	-----	---	----

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR4 board (100 sq mm, 1 oz. Cu, steady state)
2. Mounted onto a 2" square FR4 board (645 sq mm, 1 oz. Cu, steady state)
3. Not tested in production.
4. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750-1.

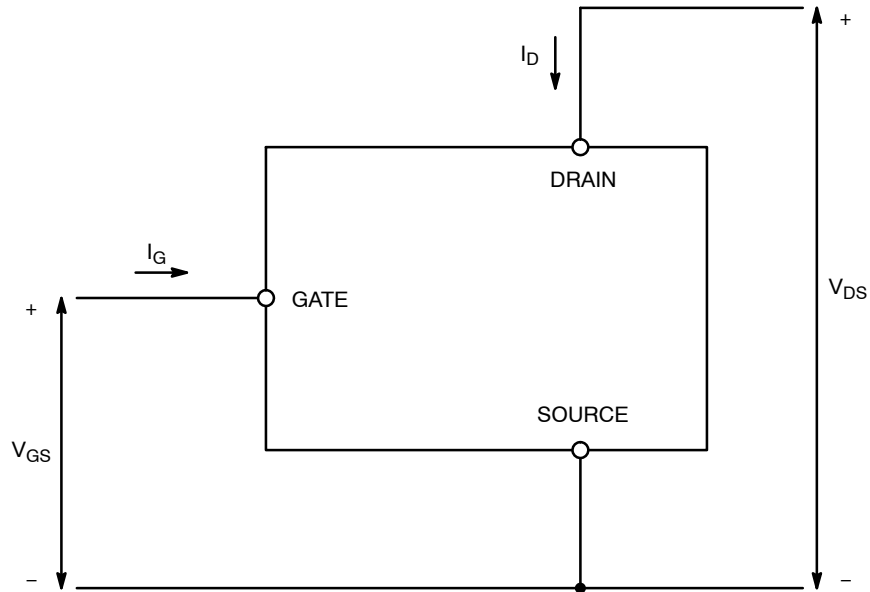


Figure 2. Voltage and Current Convention

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Clamped Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	$V_{(BR)DSS}$	42	46	50	V
	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}, T_J = 150^\circ\text{C}$ (Note 5)		42	44	50	
Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	–	1.5	5	μA
	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$ (Note 5)		–	5.5	–	
Gate Input Current	$V_{GS} = 5\text{ V}, V_{DS} = 0\text{ V}$	I_{GSS}	–	50	100	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1.2\text{ mA}$	$V_{GS(th)}$	1.0	1.8	2.5	V
Threshold Temperature Coefficient	$V_{GS} = V_{DS}, I_D = 1.2\text{ mA}$ (Note 5)		–	5	–	$\text{mV}/^\circ\text{C}$
Static Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(ON)}$	–	23	29	$\text{m}\Omega$
	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}, T_J = 150^\circ\text{C}$ (Note 5)		–	43	55	
	$V_{GS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 25^\circ\text{C}$		–	28	34	
	$V_{GS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 150^\circ\text{C}$ (Note 5)		–	50	60	
Source Drain Forward On Voltage	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	–	0.8	1.1	V
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Time (10% V_{GS} to 90% I_D)	$V_{GS} = 0\text{ V to } 5\text{ V}, V_{DS} = 12\text{ V}, I_D = 1\text{ A}$	t_{ON}	–	29	50	μs
Turn-Off Time (90% V_{GS} to 10% I_D)		t_{OFF}	–	53	150	
Turn-On Time (10% V_{GS} to 90% I_D)	$V_{GS} = 0\text{ V to } 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 1\text{ A}$	t_{ON}	–	14	25	
Turn-Off Time (90% V_{GS} to 10% I_D)		t_{OFF}	–	80	180	
Slew Rate On (80% V_{DS} to 50% V_{DS})	$V_{GS} = 0\text{ V to } 10\text{ V}, V_{DD} = 12\text{ V}, R_L = 4.7\text{ }\Omega$	$-dV_{DS}/dt_{ON}$	–	1.52	2.5	$\text{V}/\mu\text{s}$
Slew Rate Off (50% V_{DS} to 80% V_{DS})		dV_{DS}/dt_{OFF}	–	0.71	0.85	
SELF PROTECTION CHARACTERISTICS						
Current Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$ (Note 6)	I_{LIM}	29	33	40	A
	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, T_J = 150^\circ\text{C}$ (Notes 5, 6)		27	31	37	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$ (Notes 5, 6)		23	34	46	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, T_J = 150^\circ\text{C}$ (Notes 5, 6)		23	33	46	
Temperature Limit (Turn-Off)	$V_{GS} = 5\text{ V}$ (Notes 5, 6)	$T_{LIM(OFF)}$	150	170	185	$^\circ\text{C}$
Thermal Hysteresis		$\Delta T_{LIM(ON)}$	–	10	–	
Temperature Limit (Turn-Off)	$V_{GS} = 10\text{ V}$ (Notes 5, 6)	$T_{LIM(OFF)}$	150	180	200	
Thermal Hysteresis		$\Delta T_{LIM(ON)}$	–	10	–	
GATE INPUT CHARACTERISTICS (Note 5)						
Device ON Gate Input Current – Normal Operation	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, I_D = 1\text{ A}$	I_{GON}	–	50	100	μA
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, I_D = 1\text{ A}$		200	318	500	
Device ON Gate Input Current – Thermal Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}, I_D = 0\text{ A}$	I_{GTL}	–	633	900	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, I_D = 0\text{ A}$		–	1470	2000	
Device ON Gate Input Current – Current Limit	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$	I_{GCL}	–	245	600	
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$		–	1121	1500	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Not tested in production.

6. Refer to Apps Note AND8202D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

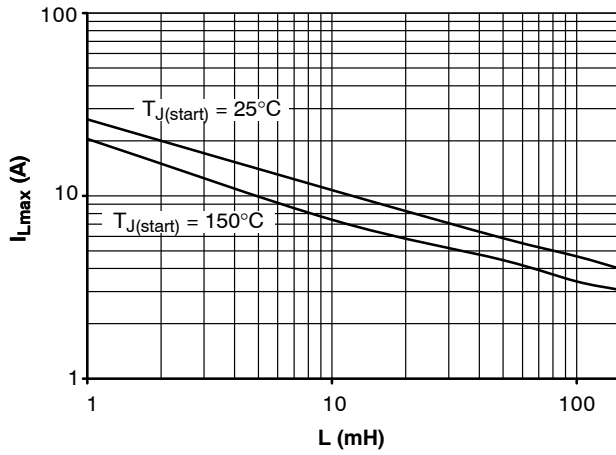


Figure 3. Single Pulse Maximum Switch-off Current vs. Load Inductance

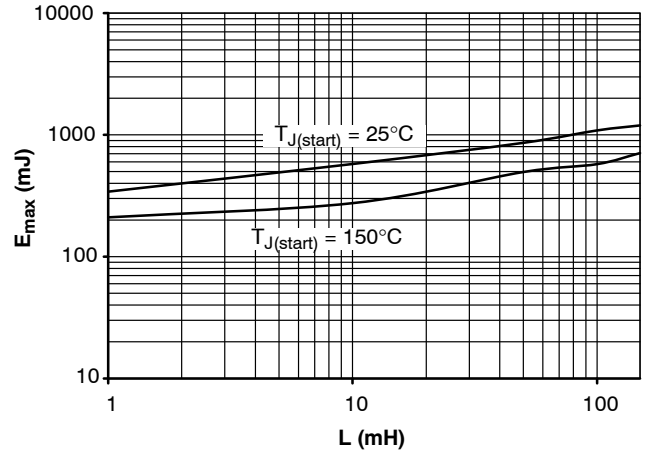


Figure 4. Single Pulse Maximum Switching Energy vs. Load Inductance

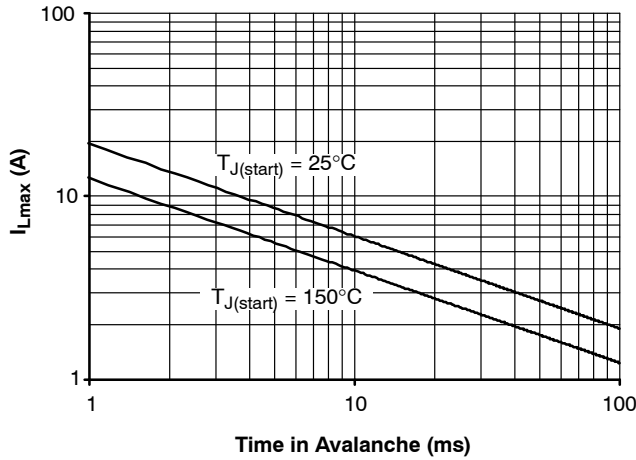


Figure 5. Single Pulse Maximum Inductive Switch-off Current vs. Time in Avalanche

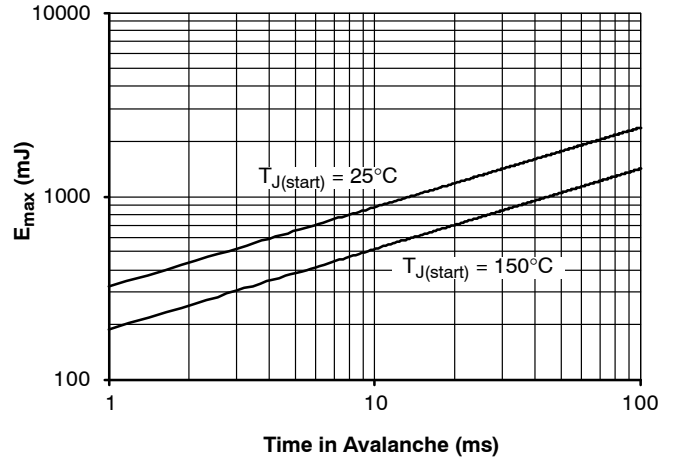


Figure 6. Single Pulse Maximum Inductive Switching Energy vs. Time in Avalanche

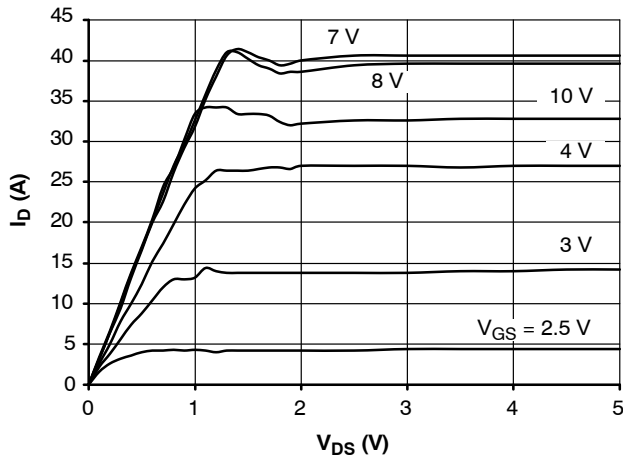


Figure 7. On-state Output Characteristics at 25°C

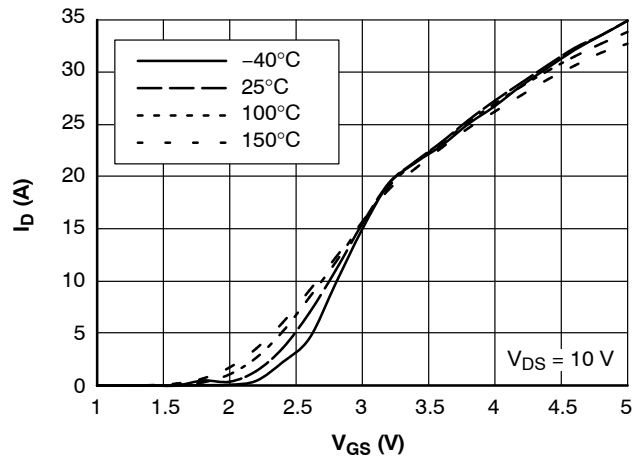


Figure 8. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

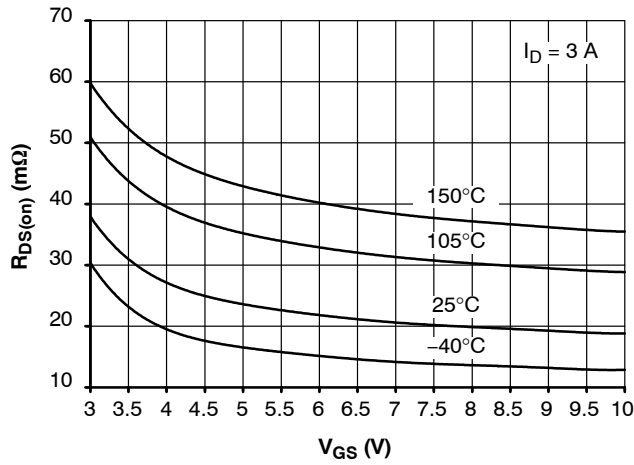


Figure 9. $R_{DS(on)}$ vs. Gate-Source Voltage

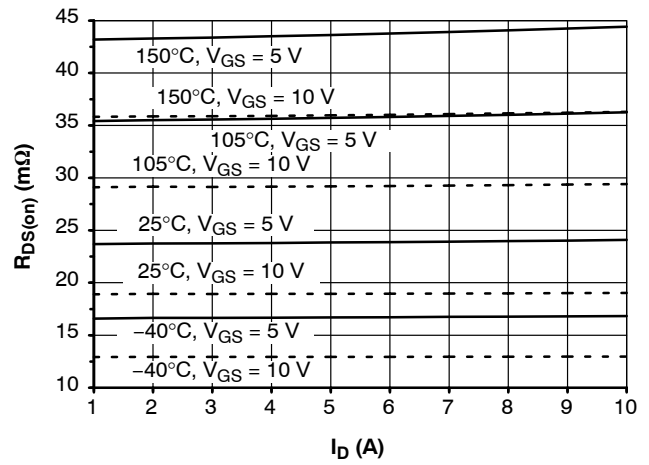


Figure 10. $R_{DS(on)}$ vs. Drain Current

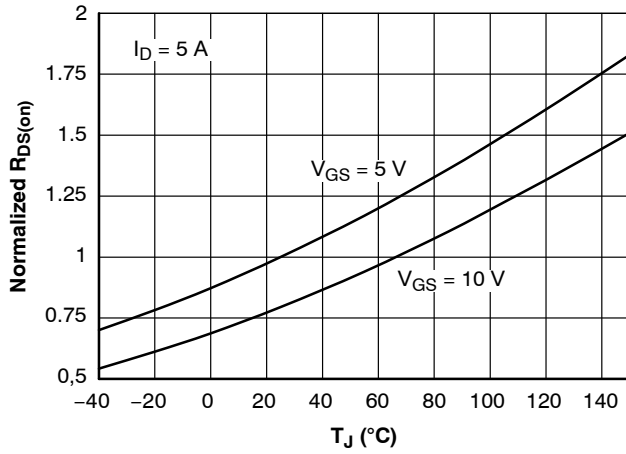


Figure 11. Normalized $R_{DS(on)}$ vs. Temperature

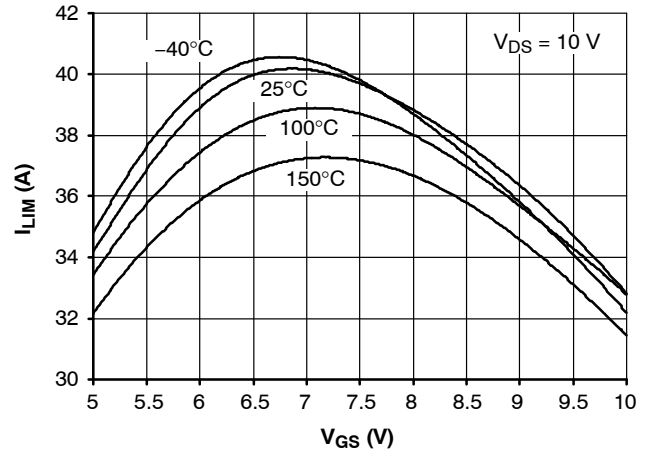


Figure 12. Current Limit vs. Gate-Source Voltage

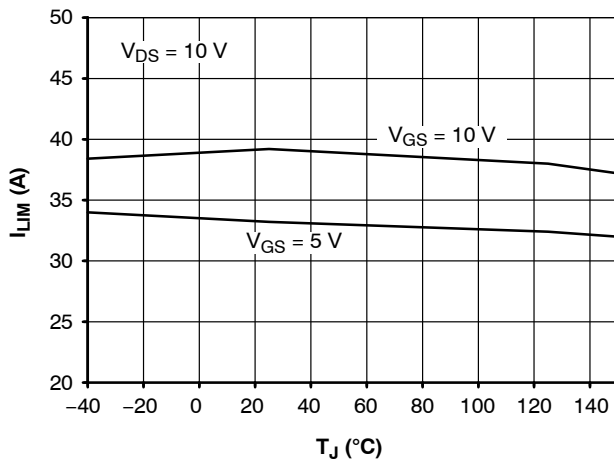


Figure 13. Current Limit vs. Junction Temperature

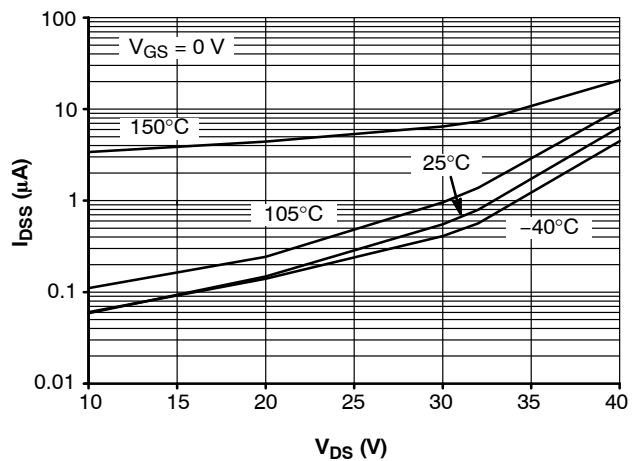


Figure 14. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

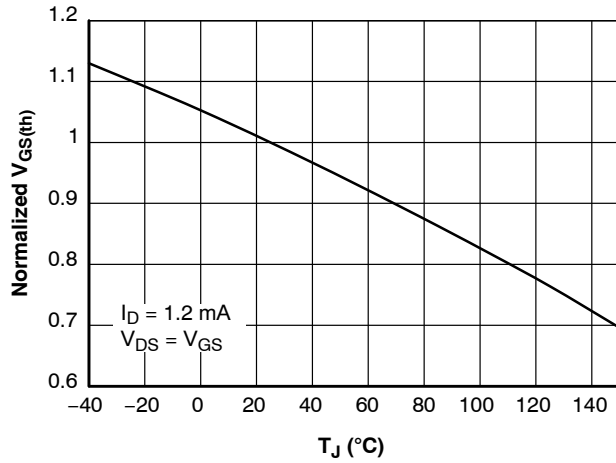


Figure 15. Normalized Threshold Voltage vs. Temperature

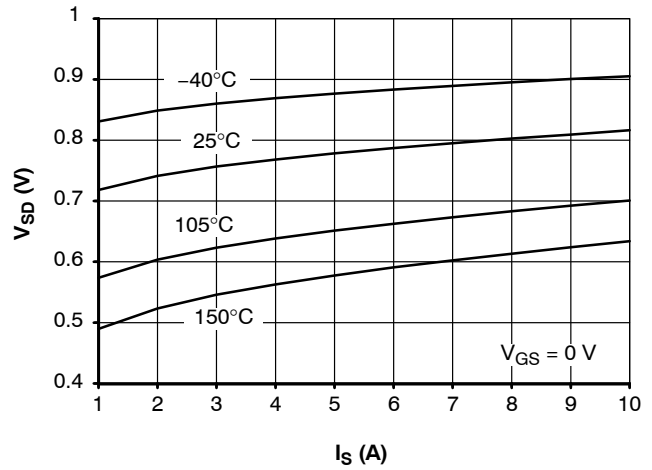


Figure 16. Source-Drain Diode Forward Characteristics

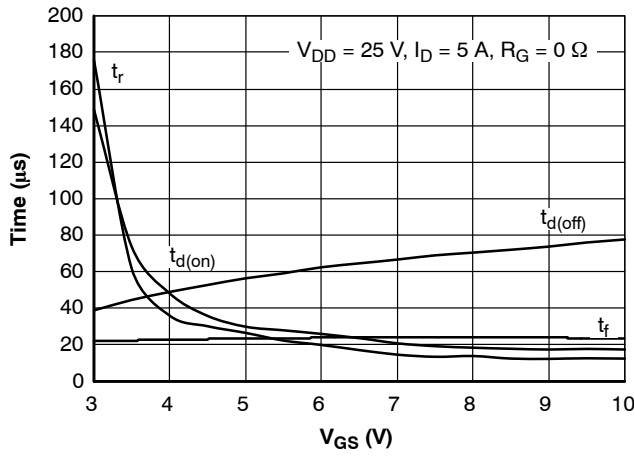


Figure 17. Resistive Load Switching Time vs. Gate-Source Voltage

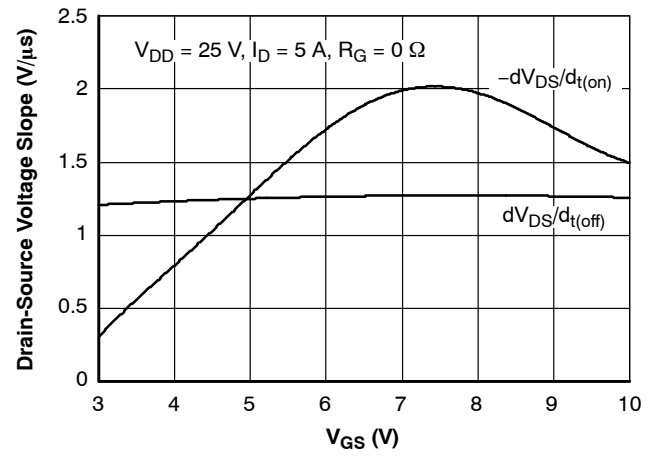


Figure 18. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

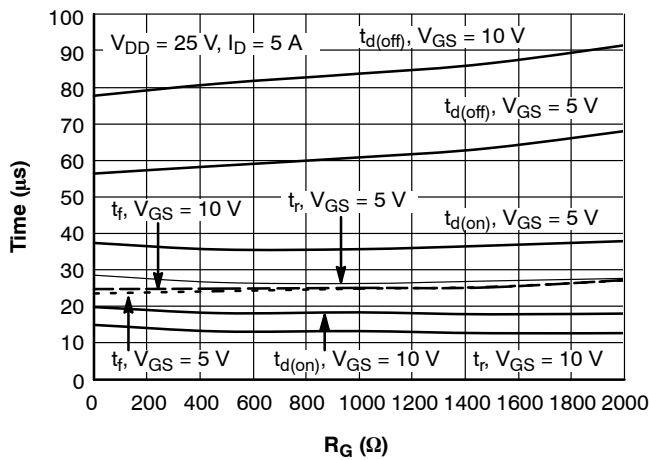


Figure 19. Resistive Load Switching Time vs. Gate Resistance

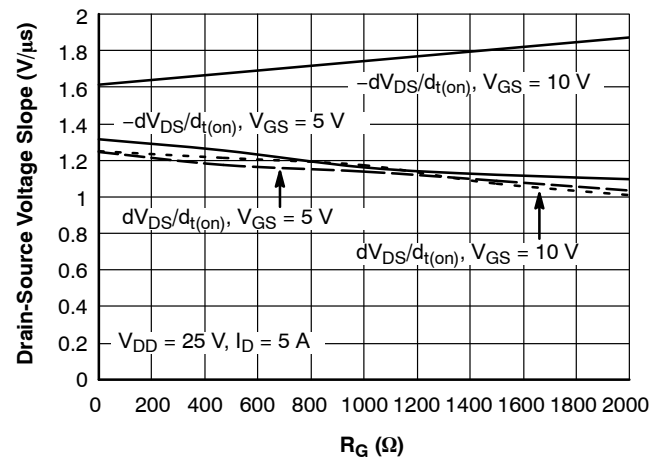


Figure 20. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

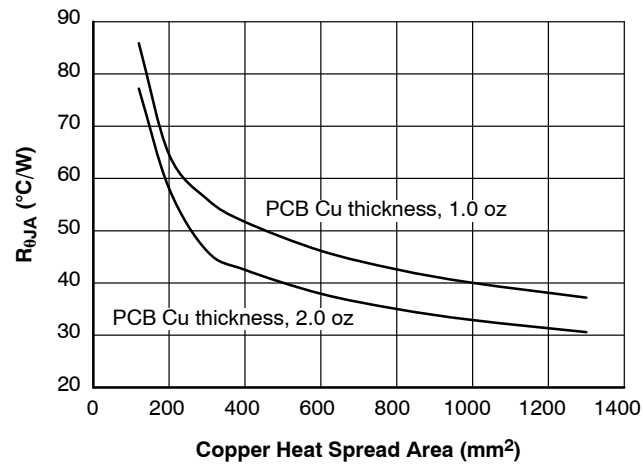


Figure 21. R_{θJA} vs. Copper Area

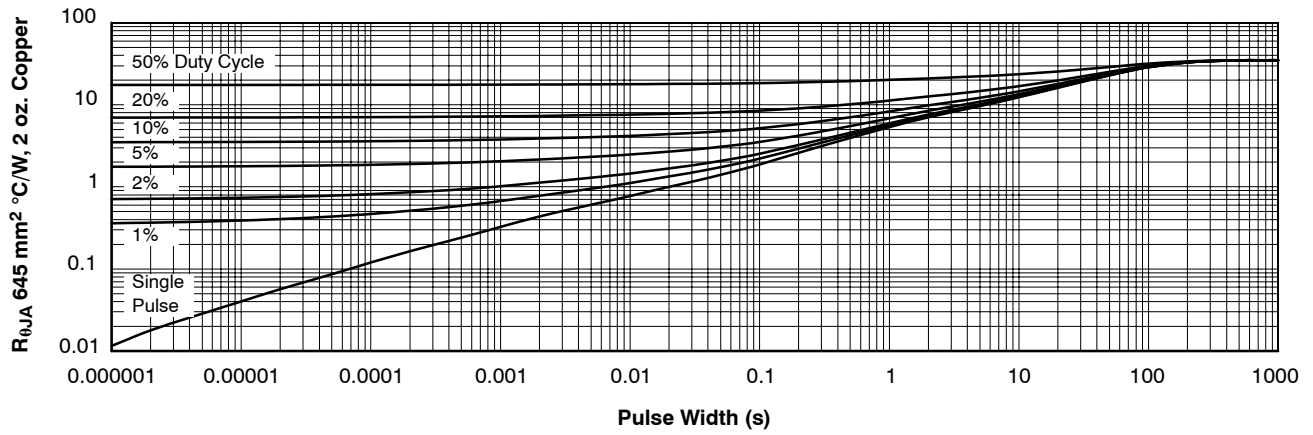


Figure 22. Transient Thermal Resistance

APPLICATION INFORMATION

Circuit Protection Features

The NCV8411 has three main protections. Current Limit, Thermal Shutdown and Delta Thermal Shutdown. These protections establish robustness of the NCV8411.

Current Limit and Short Circuit Protection

The NCV8411 has current sense element. In the event that the drain current reaches designed current limit level, integrated Current Limit protection establishes its constant level.

Delta Thermal Shutdown

Delta Thermal Shutdown (DTSD) Protection increases higher reliability of the NCV8411. DTSD consist of two independent temperature sensors – cold and hot sensors. The

NCV8411 establishes a slow junction temperature rise by sensing the difference between the hot and cold sensors. ON/OFF output cycling is designed with hysteresis that results in a controlled saw tooth temperature profile (Figure 23). The die temperature slowly rises (DTSD) until the absolute temperature shutdown (TSD) is reached around 175°C.

Thermal Shutdown with Automatic Restart

Internal Thermal Shutdown (TSD) circuitry is provided to protect the NCV8411 in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the NCV8411 turns off. This feature is provided to prevent failures from accidental overheating.

TEST CIRCUITS AND WAVEFORMS

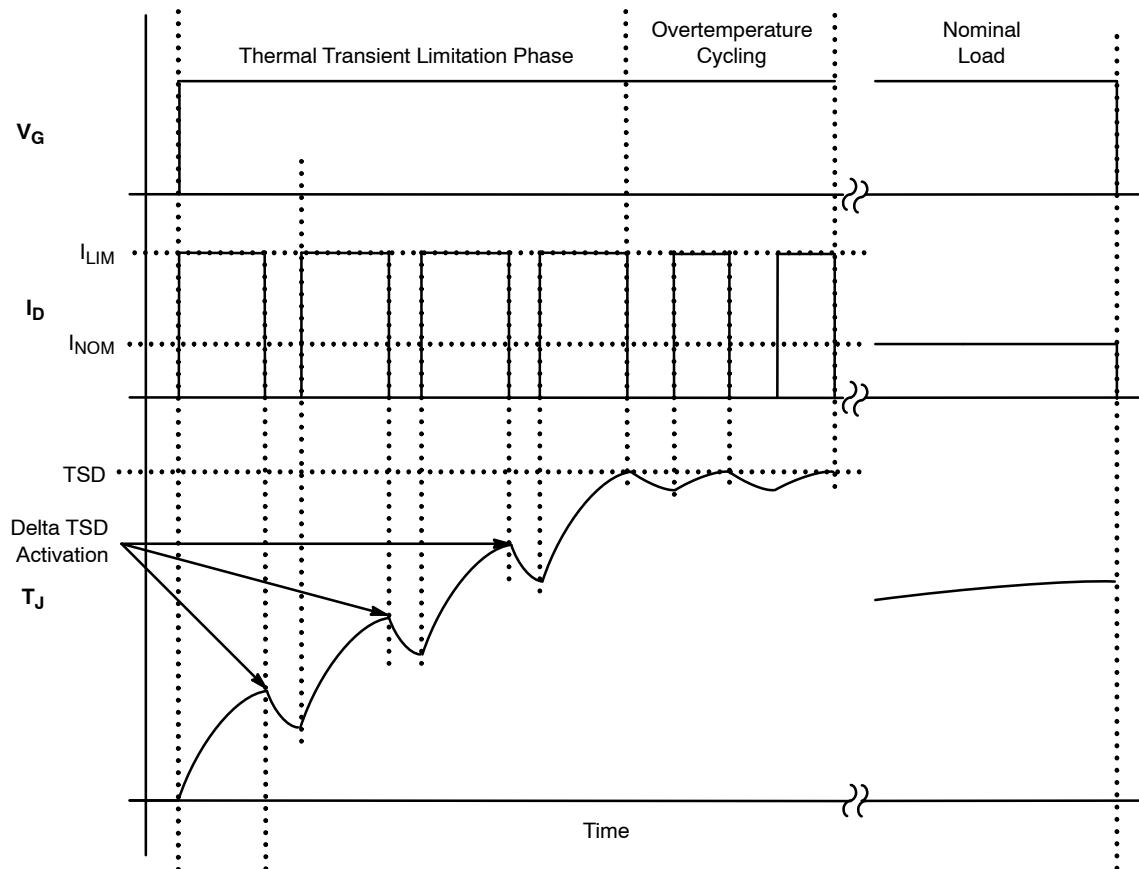


Figure 23. Overload Protection Behavior

TEST CIRCUITS AND WAVEFORMS

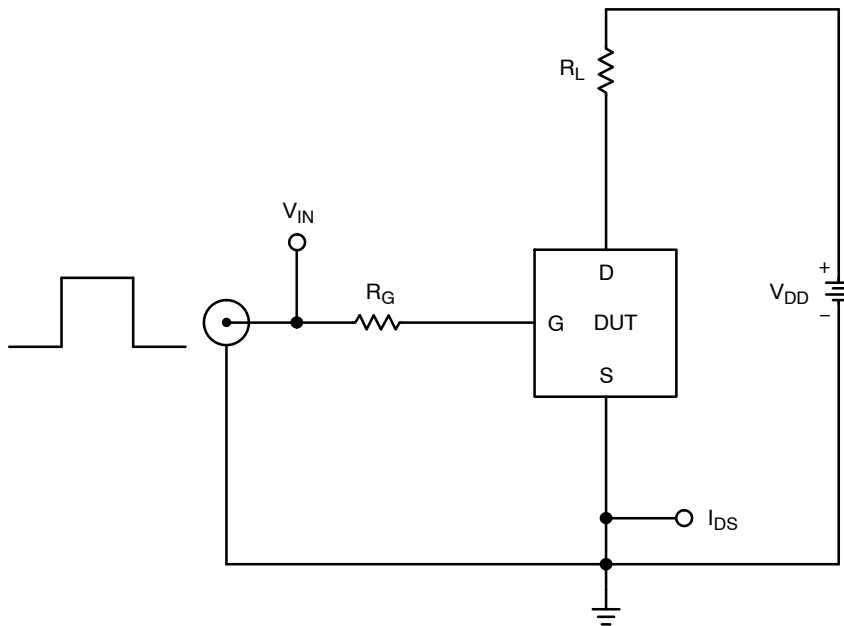


Figure 24. Resistive Load Switching Test Circuit

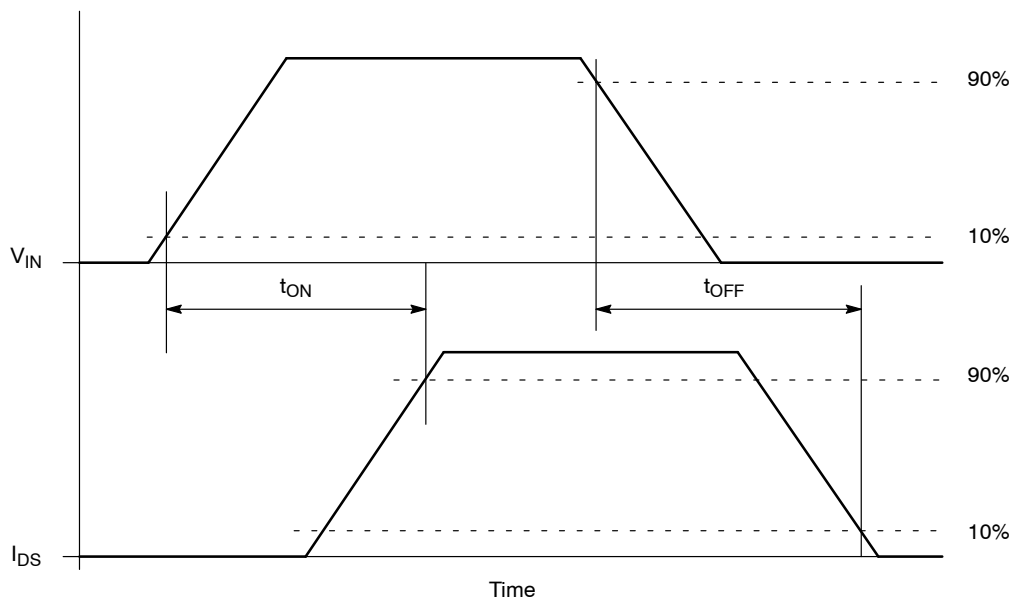


Figure 25. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

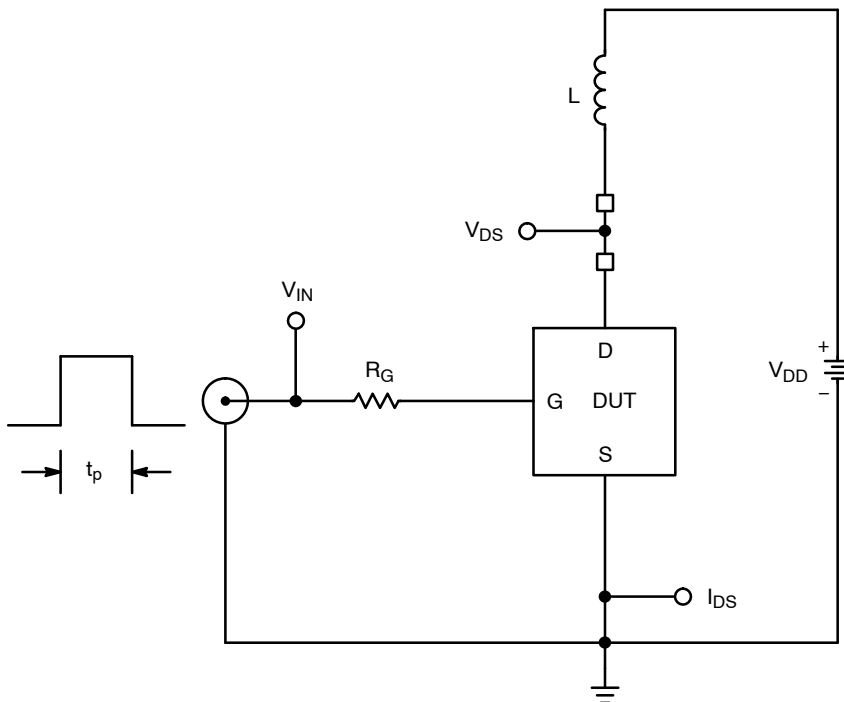


Figure 26. Inductive Load Switching Test Circuit

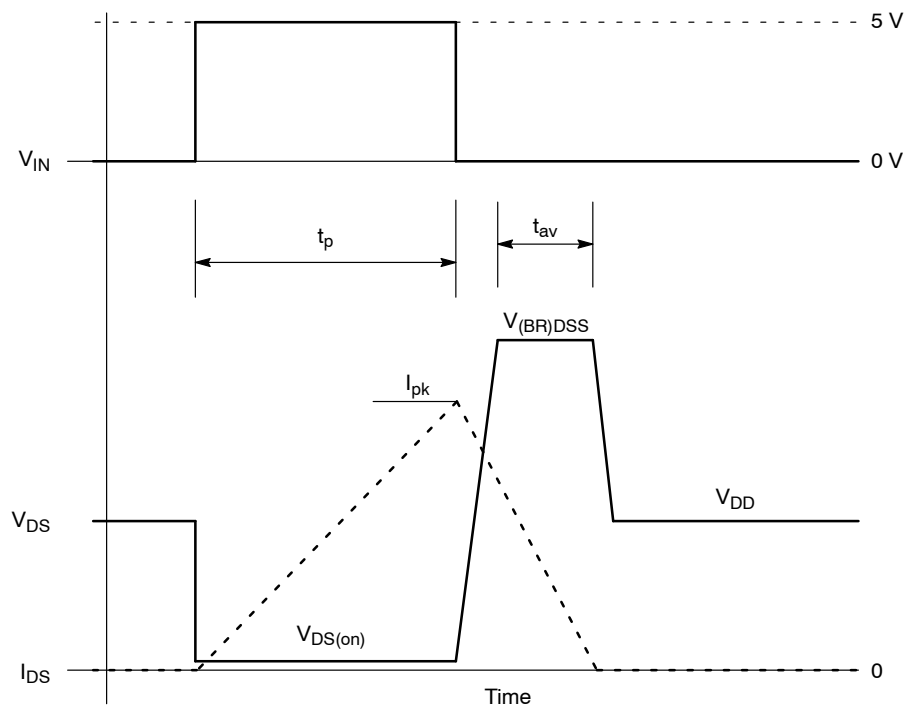
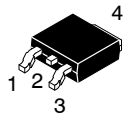


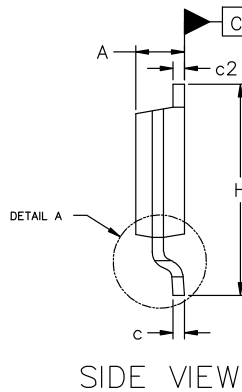
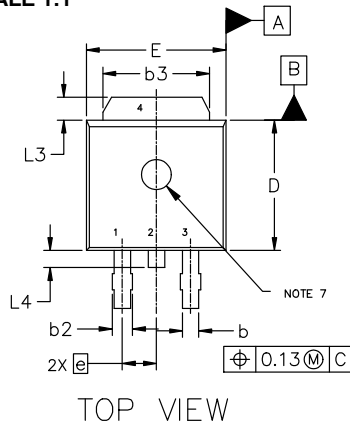
Figure 27. Inductive Load Switching Waveform



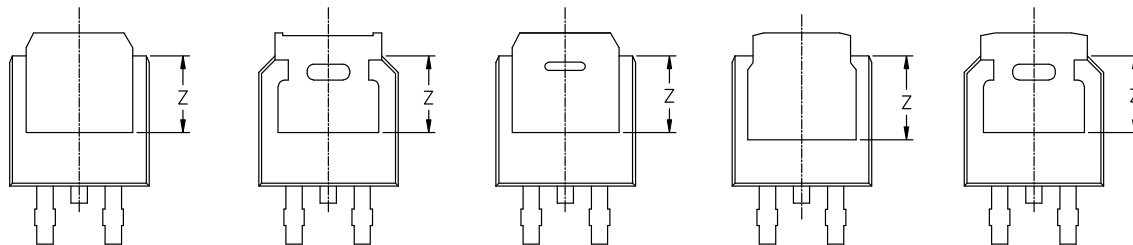
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1

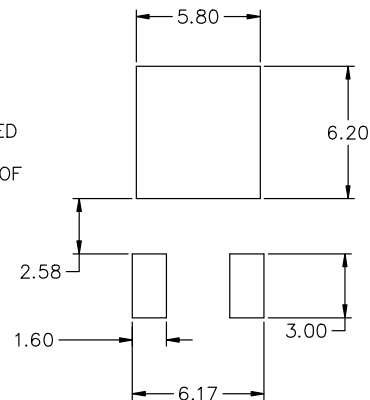
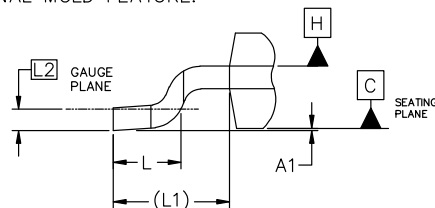


MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

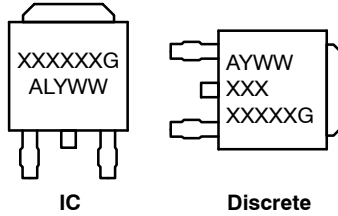
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 2 OF 2

onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales