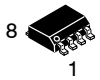
# High Speed Low Power CAN Transceiver

# NCV7349




**SOIC-8**
**CASE 751AZ**

## Description

The NCV7349 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7349 is a new addition to the CAN high-speed transceiver family complementing NCV734x CAN family and previous generations of CAN transceivers such as AMIS42665, AMIS3066x, etc.

Due to the wide common-mode voltage range of the receiver inputs and other design features, the NCV7349 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, very low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

## Features

- Compatible with the ISO 11898-5 Standard
- High Speed (up to 1 Mbps)
- $V_{IO}$ Pin on NCV7349-3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- Very Low Current Standby Mode with Wake-up via the Bus
- Low Electromagnetic Emission (EME) and Extremely High Electromagnetic Immunity
- Very Low EME without Common-mode (CM) Choke
- No Disturbance of the Bus Lines with an Un-powered Node
- Transmit Data (TxD) Dominant Time-out Function
- Under All Supply Conditions the Chip Behaves Predictably
- Very High ESD Robustness of Bus Pins, >10 kV System ESD Pulses
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive
- These are Pb-Free Devices

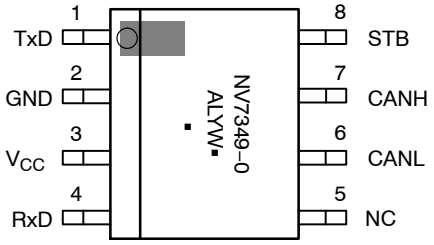
## Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

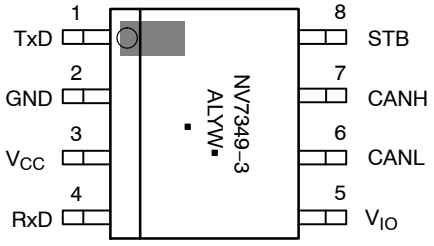
## Typical Applications

- Automotive
- Industrial Networks

## PIN ASSIGNMENT

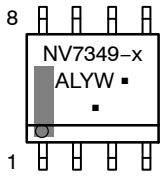



NCV7349D10R2G
**(Top View)**




NCV7349D13R2G
**(Top View)**

## MARKING DIAGRAM




NV7349–x = Specific Device Code
x = 0 or 3
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

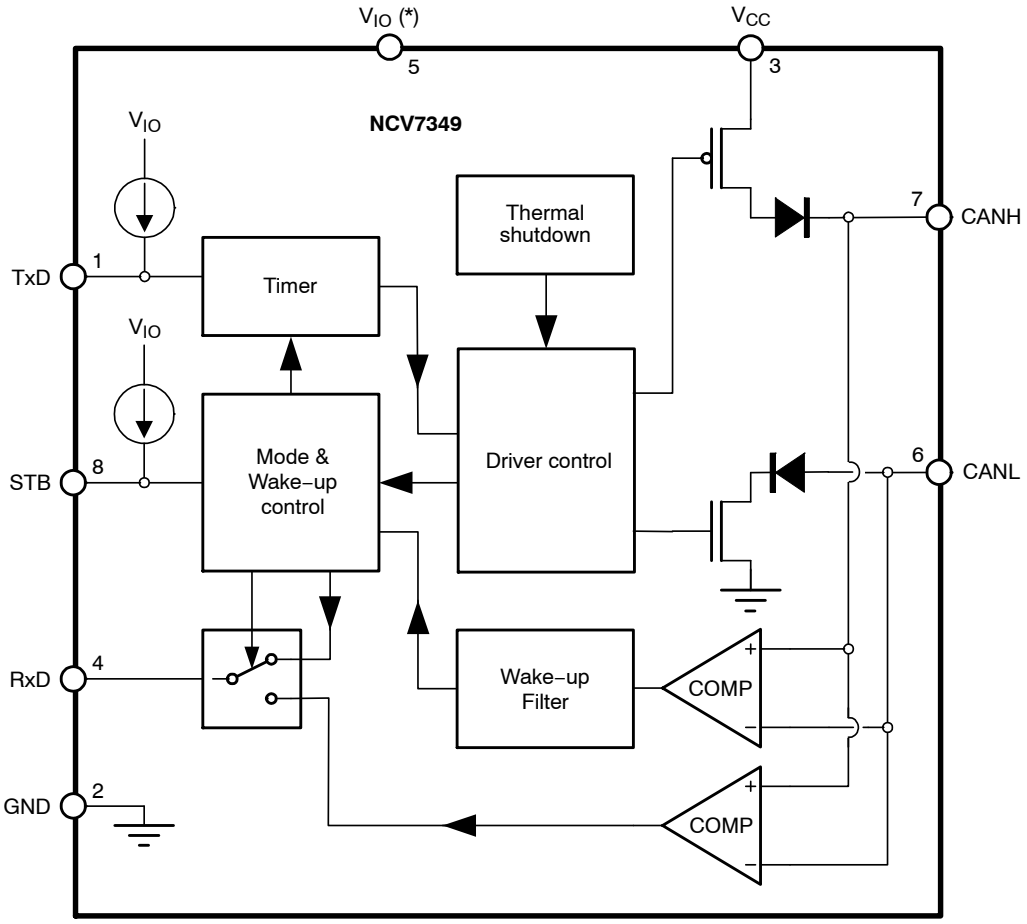
**Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | (Note 1) | 4.75 (4.5) | 5.25 (5.5) | V |
| $V_{UV}$ | Undervoltage detection voltage on pin Vcc | | 2 | 4 | V |
| $V_{CANH}$ | DC voltage at pin CANH | $0 < V_{CC} < 5.5$ V; no time limit | −50 | +50 | V |
| $V_{CANL}$ | DC voltage at pin CANL | $0 < V_{CC} < 5.5$ V; no time limit | −50 | +50 | V |
| $V_{CANH,Lmax}$ | DC voltage at pin CANH and CANL during load dump condition | $0 < V_{CC} < 5.5$ V, less than one second | – | +58 | V |
| $V_{ESD}$ | Electrostatic discharge voltage | IEC 61000−4−2 at pins CANH and CANL | −15 | 15 | kV |
| $V_{O(dif)(bus\_dom)}$ | Differential bus output voltage in dominant state | $45\ \Omega < R_{LT} < 65\ \Omega$ | 1.5 | 3 | V |
| CM-range | Input common-mode range for comparator | Guaranteed differential receiver threshold and leakage current | −35 | +35 | V |
| $C_{load}$ | Load capacitance on IC outputs | | – | 15 | pF |
| $t_{pd0}$ | Propagation delay (NCV7349-0 version) | See Figure 7 | – | 245 | ns |
| $t_{pd3}$ | Propagation delay (NCV7349-3 version) | See Figure 7 | – | 250 | ns |
| $T_J$ | Junction temperature | | −40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. In the range of 4.5 V to 4.75 V and from 5.25 V to 5.5 V the chip is fully functional; some parameters may be outside of the specification.

## BLOCK DIAGRAM




* On NCV7349-0 version pin 5 is not connected. $V_{IO}$ supply is provided by $V_{CC}$.

**Figure 1. Block Diagram**

## TYPICAL APPLICATION

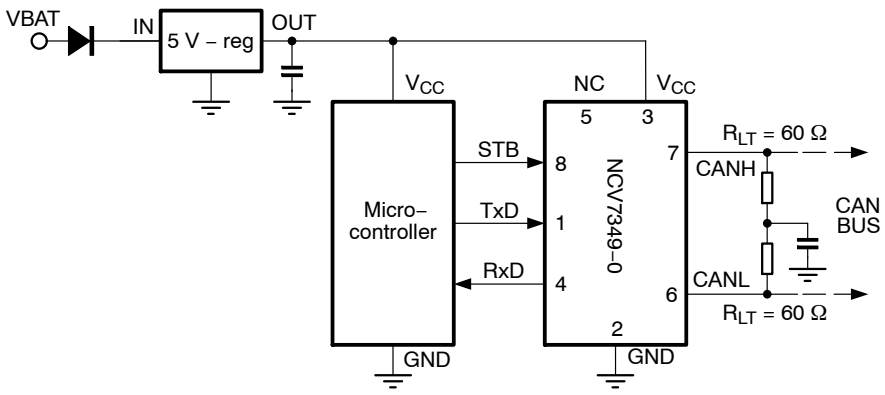



**Figure 2. Application Diagram, NCV7349-0**

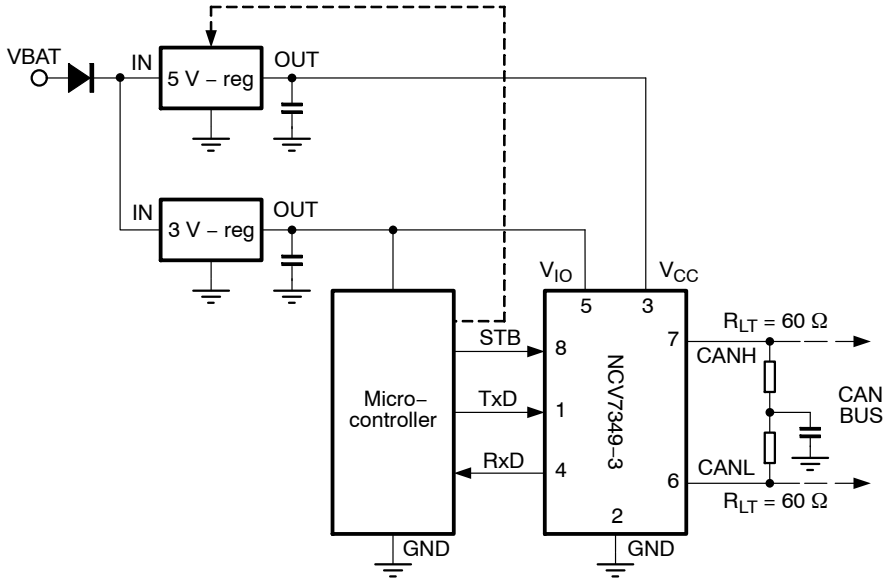



**Figure 3. Application Diagram, NCV7349-3**

**Table 2. PIN FUNCTION DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | TxD | Transmit data input; low input → Driving dominant on bus; internal pull-up current |
| 2 | GND | Ground |
| 3 | $V_{CC}$ | Supply voltage |
| 4 | RxD | Receive data output; bus in dominant → low output |
| 5<br>5 | NC<br>$V_{IO}$ | Not connected. On NCV7349-0 only.<br>Input / Output pins supply voltage. On NCV7349-3 only |
| 6 | CANL | Low-level CAN bus line (low in dominant mode) |
| 7 | CANH | High-level CAN bus line (high in dominant mode) |
| 8 | STB | Standby mode control input; internal pull-up current |

## FUNCTIONAL DESCRIPTION

**NCV7349** has two versions which differ from each other only by function of pin 5.

**NCV7349-0:** Pin 5 is not connected. (see Figure 2)

**NCV7349-3:** Pin 5 is $V_{IO}$ pin, which is supply pin for transceiver digital inputs/output (supplying pins TxD, RxD, STB) The $V_{IO}$ pin should be connected to microcontroller supply pin. By using $V_{IO}$ supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. This adjustment allows in applications with microcontroller supply down to 3 V to easy communicate with the transceiver. (See Figure 3)

### Operating Modes

NCV7349 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

**Table 3. OPERATING MODES**

| Pin STB | Mode | Pin RxD | |
|---|---|---|---|
| | | Low | High |
| Low | Normal | Bus dominant | Bus recessive |
| High | Standby | Wake-up request detected | No wake-up request detected |

### Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

### Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low-power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μA. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of $t_{wake}$, the RxD pin is driven low by the transceiver to inform the controller of the wake-up request.

### $V_{IO}$ Supply pin

The $V_{IO}$ pin available only on NCV7349-3 version should be connected to microcontroller supply pin. By using $V_{IO}$ supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 3. Pin $V_{IO}$ on NCV7349-3 does not provide the internal supply voltage for low-power differential receiver of the transceiver. Detection of wake-up request is not possible when there is no supply voltage on pin $V_{CC}$.

### Wake-up

When a valid wake-up (dominant state longer than $t_{wake}$) is received during the standby mode the RxD pin is driven low. The wake-up detection is not latched: RxD returns to High state after $t_{dwakedr}$ when the bus signal is released back to recessive - see Figure 4.

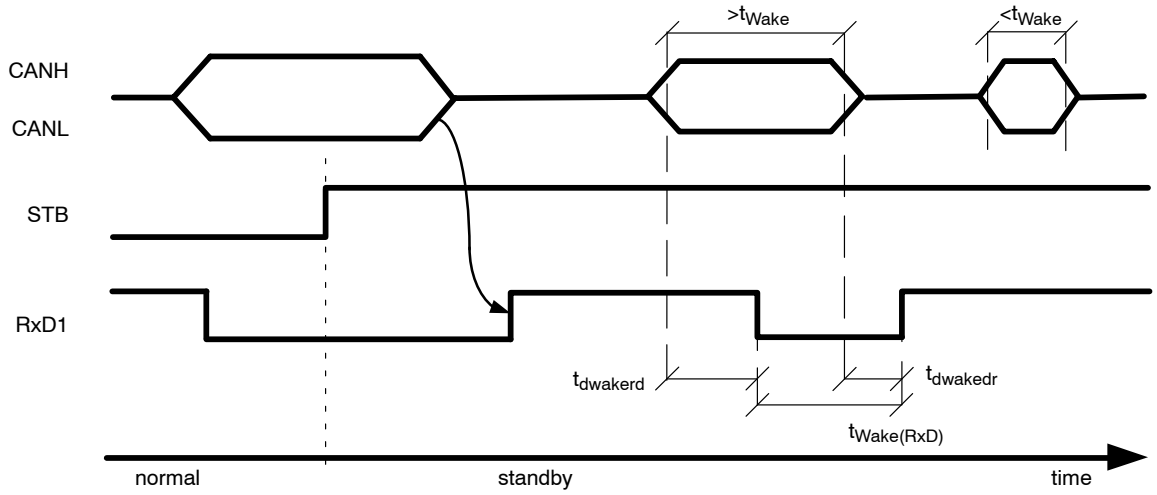



**Figure 4. NCV7349 Wake-up Behavior**

### Over-temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 170°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

### TxD Dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant time-out time ($t_{dom(TxD)}$) defines the minimum possible bit rate to 15 kbps.

### Fail Safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Undervoltage on $V_{CC}$ pin prevents the chip sending data on the bus when there is not enough $V_{CC}$ supply voltage. After supply is recovered TxD pin must be first released to high to allow sending dominant bits again. Recovery time from undervoltage detection is equal to $t_{d(stb-nm)}$ time.

$V_{IO}$ supply dropping below $V_{UVDVIO}$ undervoltage detection level will cause the transmitter to disengage from the bus (no bus loading) until the $V_{IO}$ voltage recovers (NCV7349-3 version only).

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 7). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the $V_{IO}$ supply be removed.

## ELECTRICAL CHARACTERISTICS

### Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

## ABSOLUTE MAXIMUM RATINGS

**Table 4. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{SUP}$ | Supply voltage $V_{CC}$, $V_{IO}$ | | −0.3 | +6 | V |
| $V_{CANH}$ | DC voltage at pin CANH | 0 < $V_{CC}$ < 5.5 V; no time limit | −50 | +50 | V |
| $V_{CANL}$ | DC voltage at pin CANL | 0 < $V_{CC}$ < 5.5 V; no time limit | −50 | +50 | V |
| $V_{IO}$ | DC voltage at pin TxD, RxD, STB | | −0.3 | 6 | V |
| $V_{esd}$ | Electrostatic discharge voltage at all pins | (Note 2)<br>(Note 3) | −6<br>500 | 6<br>500 | kV<br>V |
| | Electrostatic discharge voltage at CANH and CANL pins | (Note 4) | −10 | 10 | kV |
| $V_{schaff}$ | Transient voltage | (Note 5) | −150 | 100 | V |
| Latch-up | Static latch-up at all pins | (Note 6) | – | 150 | mA |
| $T_{stg}$ | Storage temperature | | −55 | +150 | °C |
| $T_A$ | Ambient temperature | | −40 | +125 | °C |
| $T_J$ | Maximum junction temperature | | −40 | +170 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA-JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Standardized charged device model ESD pulses when tested according to ESD-STM5.3.1-1999.
4. System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND.
5. Pulses 1, 2a, 3a and 3b according to ISO 7637 part 3. Indicative values based on structural similarity to NCV7340 where results were verified by external test house.
6. Static latch-up immunity: Static latch-up protection level when tested according to EIA/JESD78.

**Table 5. THERMAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA\_1}$ | Thermal Resistance Junction-to-Air, 1S0P PCB (Note 7) | Free air | 125 | K/W |
| $R_{\theta JA\_2}$ | Thermal Resistance Junction-to-Air, 2S2P PCB (Note 8) | Free air | 75 | K/W |

7. Test board according to EIA/JEDEC Standard JESD51-3, signal layer with 10% trace coverage
8. Test board according to EIA/JEDEC Standard JESD51-7, signal layers with 10% trace coverage

## ELECTRICAL CHARACTERISTICS

**Table 6. ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.8 V to 5.5 V (NCV7349-3 only); $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless specified otherwise. On chip versions without $V_{IO}$ pin, reference voltage for all digital inputs and outputs is $V_{CC}$ instead of $V_{IO}$.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY (Pin $V_{CC}$)** | | | | | | |
| $I_{CC}$ | Supply current | Dominant; $V_{TxD}$ = 0 V<br>Recessive; $V_{TxD}$ = $V_{IO}$ | – | 48<br>6 | 75<br>10 | mA |
| $I_{CCS}$ | Supply current in standby mode | $T_J \le 100°C$, (Note 9) | – | 10 | 15 | μA |
| $V_{UVDVCC}$ | Undervoltage detection voltage on $V_{CC}$ pin | | 2 | 3 | 4 | V |
| **SUPPLY (pin $V_{IO}$) on NCV7349-3 Version Only** | | | | | | |
| $V_{IO}$ | Supply voltage on pin $V_{IO}$ | | 2.8 | – | 5.5 | V |
| $I_{IOS}$ | Supply current on pin $V_{IO}$ in standby mode | Standby mode | – | 1 | – | μA |
| $I_{IONM}$ | Supply current on pin $V_{IO}$ in normal mode | Dominant; $V_{TxD}$ = 0 V<br>Recessive; $V_{TxD}$ = $V_{IO}$<br>For $V_{IO} \le V_{CC}$ | – | – | 1<br>0.2 | mA |
| $V_{UVDVIO}$ | Undervoltage detection voltage on $V_{IO}$ pin | | 1.3 | – | 2.7 | V |
| **TRANSMITTER DATA INPUT (Pin TxD)** | | | | | | |
| $V_{IH}$ | High-level input voltage | Output recessive | 2.0 | – | $V_{IO}$ | V |
| $V_{IL}$ | Low-level input voltage | Output dominant | −0.3 | – | +0.8 | V |
| $I_{IH}$ | High-level input current | $V_{TxD}$ = $V_{IO}$ | −5 | 0 | +5 | μA |
| $I_{IL}$ | Low-level input current | $V_{TxD}$ = 0 V | −350 | −200 | – | μA |
| $C_i$ | Input capacitance | (Note 9) | – | 5 | 10 | pF |
| **TRANSMITTER MODE SELECT (Pin STB)** | | | | | | |
| $V_{IH}$ | High-level input voltage | Standby mode | 2.0 | – | $V_{IO}$ | V |
| $V_{IL}$ | Low-level input voltage | Normal mode | −0.3 | – | +0.8 | V |
| $I_{IH}$ | High-level input current | $V_{STB}$ = $V_{IO}$ | −5 | 0 | +5 | μA |
| $I_{IL0}$ | Low-level input current, NCV7349-0 | $V_{STB}$ = 0 V | −10 | −4 | −1 | μA |
| $I_{IL3}$ | Low-level input current, NCV7349-3 | $V_{STB}$ = 0 V | −40 | −20 | −4 | μA |
| $C_i$ | Input capacitance | (Note 9) | – | 5 | 10 | pF |
| **RECEIVER DATA OUTPUT (Pin RxD)** | | | | | | |
| $I_{OH}$ | High-level output current | Normal mode,<br>$V_{RxD}$ = $V_{IO}$ − 0.4 V | −1 | −0.4 | −0.1 | mA |
| $I_{OL}$ | Low-level output current | $V_{RxD}$ = 0.4 V | 1.6 | 6 | 12 | mA |
| $V_{OH}$ | High-level output voltage,<br>Weaker RxD pin in Standby mode is on NCV7349-0 version only | Standby mode, $I_{RxD}$ = −100 μA | $V_{CC}$ −<br>1.1 | $V_{CC}$ −<br>0.7 | $V_{CC}$ −<br>0.4 | V |
| **BUS LINES (Pins CANH and CANL)** | | | | | | |
| $V_{o(reces)}$ (norm) | Recessive bus voltage on pins CANH and CANL | $V_{TxD}$ = $V_{IO}$; no load;<br>normal mode | 2.0 | 2.5 | 3.0 | V |
| $V_{o(reces)}$ (stby) | Recessive bus voltage on pins CANH and CANL | $V_{TxD}$ = $V_{IO}$; no load;<br>standby mode | −100 | 0 | 100 | mV |
| $I_{o(reces)}$ (CANH) | Recessive output current at pin CANH | −35 V < $V_{CANH}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | – | +2.5 | mA |
| $I_{o(reces)}$ (CANL) | Recessive output current at pin CANL | −35 V < $V_{CANL}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | – | +2.5 | mA |

**Table 6. ELECTRICAL CHARACTERISTICS** (continued) ($V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.8 V to 5.5 V (NCV7349-3 only); $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless specified otherwise. On chip versions without $V_{IO}$ pin, reference voltage for all digital inputs and outputs is $V_{CC}$ instead of $V_{IO}$.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BUS LINES (Pins CANH and CANL)** (continued) | | | | | | |
| $I_{LI(CANH)}$ | Input leakage current to pin CANH | 0 Ω < R($V_{CC}$ to GND) < 1 MΩ<br>$V_{CANL}$ = $V_{CANH}$ = 5 V | −10 | 0 | 10 | μA |
| $I_{LI(CANL)}$ | Input leakage current to pin CANL | 0 Ω < R($V_{CC}$ to GND) < 1 MΩ<br>$V_{CANL}$ = $V_{CANH}$ = 5 V | −10 | 0 | 10 | μA |
| $V_{o(dom)}$ (CANH) | Dominant output voltage at pin CANH | $V_{TxD}$ = 0 V | 3.0 | 3.6 | 4.25 | V |
| $V_{o(dom)}$ (CANL) | Dominant output voltage at pin CANL | $V_{TxD}$ = 0 V | 0.5 | 1.4 | 1.75 | V |
| $V_{o(dif)}$ (bus_dom) | Differential bus output voltage ($V_{CANH}$ - $V_{CANL}$) | $V_{TxD}$ = 0 V; dominant;<br>45 Ω < $R_{LT}$ < 65 Ω | 1.5 | 2.25 | 3.0 | V |
| $V_{o(dif)}$ (bus_rec) | Differential bus output voltage ($V_{CANH}$ - $V_{CANL}$) | $V_{TxD}$ = $V_{IO}$; recessive; no load | −120 | 0 | +50 | mV |
| $I_{o(sc)}$ (CANH) | Short circuit output current at pin CANH | $V_{CANH}$ = 0 V; $V_{TxD}$ = 0 V | −100 | −70 | −45 | mA |
| $I_{o(sc)}$ (CANL) | Short circuit output current at pin CANL | $V_{CANL}$ = 36 V; $V_{TxD}$ = 0 V | 45 | 70 | 100 | mA |
| $V_{i(dif)R}$ (th) | Differential receiver threshold voltage − Dominant to Recessive (see Figure 6) | −2 V < $V_{CANL}$ < +7 V;<br>−2 V < $V_{CANH}$ < +7 V | 0.5 | 0.6 | 0.7 | V |
| $V_{i(dif)D}$ (th) | Differential receiver threshold voltage − Recessive to Dominant (see Figure 6) | −2 V < $V_{CANL}$ < +7 V;<br>−2 V < $V_{CANH}$ < +7 V | 0.7 | 0.8 | 0.9 | V |
| $V_{ihcmR(dif)}$ (th) | Differential receiver threshold voltage − Dominant to Recessive (see Figure 6) | −35 V < $V_{CANL}$ < +35 V;<br>−35 V < $V_{CANH}$ < +35 V | 0.4 | − | 0.8 | V |
| $V_{ihcmD(dif)}$ (th) | Differential receiver threshold voltage − Recessive to Dominant (see Figure 6) | −35 V < $V_{CANL}$ < +35 V;<br>−35 V < $V_{CANH}$ < +35 V | 0.6 | − | 1 | V |
| $V_{ihcmD12(dif)}$ (th) | Differential receiver threshold voltage − Both transitions (see Figure 6) | −12 V < $V_{CANL}$ < +12 V;<br>−12 V < $V_{CANH}$ < +12 V | 0.5 | − | 0.9 | V |
| $V_{i(dif)}$ (hys) | Differential receiver input voltage hysteresis | −2 V < $V_{CANL}$ < +7 V;<br>−2 V < $V_{CANH}$ < +7 V | 100 | 200 | 300 | mV |
| $V_{i(dif)}$ (th)_STDBY | Differential receiver threshold voltage in standby mode | −12 V < $V_{CANL}$ < +12 V;<br>−12 V < $V_{CANH}$ < +12 V | 0.4 | 0.8 | 1.15 | V |
| $R_{i(cm)}$ (CANH) | Common-mode input resistance at pin CANH | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)}$ (CANL) | Common-mode input resistance at pin CANL | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)}$ (m) | Matching between pin CANH and pin CANL common mode input resistance | $V_{CANH}$ = $V_{CANL}$ | −3 | 0 | +3 | % |
| $R_{i(dif)}$ | Differential input resistance | | 25 | 50 | 75 | kΩ |
| $C_{i(CANH)}$ | Input capacitance at pin CANH | $V_{TxD}$ = $V_{IO}$; (Note 9) | − | − | 30 | pF |
| $C_{i(CANL)}$ | Input capacitance at pin CANL | $V_{TxD}$ = $V_{IO}$; (Note 9) | − | − | 30 | pF |
| $C_{i(dif)}$ | Differential input capacitance | $V_{TxD}$ = $V_{IO}$; (Note 9) | − | 3.75 | 10 | pF |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(sd)}$ | Shutdown junction temperature | Junction temperature rising | 150 | 170 | 185 | °C |
| **TIMING CHARACTERISTICS (see Figure 5 and Figure 8)** | | | | | | |
| $t_{d(TxD-BUSon)}$ | Delay TxD to bus active | $C_i$ = 100 pF between CANH to CANL | − | 50 | − | ns |
| $t_{d(TxD-BUSoff)}$ | Delay TxD to bus inactive | $C_i$ = 100 pF between CANH to CANL | − | 60 | − | ns |
| $t_{d(BUSon-RxD)}$ | Delay bus active to RxD | $C_{RxD}$ = 15 pF | − | 60 | − | ns |

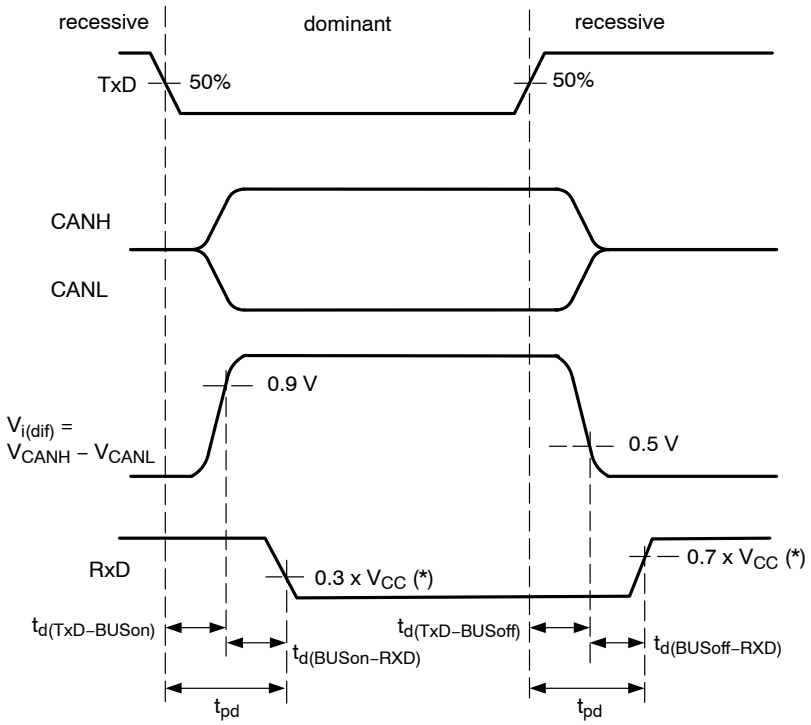
**Table 6. ELECTRICAL CHARACTERISTICS** (continued) ($V_{CC}$ = 4.75 V to 5.25 V; $V_{IO}$ = 2.8 V to 5.5 V (NCV7349-3 only); $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless specified otherwise. On chip versions without $V_{IO}$ pin, reference voltage for all digital inputs and outputs is $V_{CC}$ instead of $V_{IO}$.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS (see Figure 5 and Figure 8)** | | | | | | |
| $t_{d(BUSoff-RxD)}$ | Delay bus inactive to RxD | $C_{RxD}$ = 15 pF | – | 60 | – | ns |
| $t_{pd}$ | Propagation delay TxD to RxD (NCV7349-0 version) | $C_i$ = 100 pF between CANH to CANL | – | 125 | 245 | ns |
| | Propagation delay TxD to RxD (NCV7349-3 version) | $C_i$ = 100 pF between CANH to CANL | – | 130 | 250 | ns |
| $t_{d(stb-nm)}$ | Delay standby mode to normal mode | | 5 | 8 | 20 | μs |
| $t_{wake}$ | Dominant time for wake-up via bus | | 0.5 | 2.5 | 5 | μs |
| $t_{dwakerd}$ | Delay to flag wake event (recessive to dominant transitions) (See Figure 4) | Valid bus wake-up event, $C_{RxD}$ = 15 pF | 1 | 4.5 | 10 | μs |
| $t_{dwakedr}$ | Delay to flag wake event (dominant to recessive transitions) (See Figure 4) | Valid bus wake-up event, $C_{RxD}$ = 15 pF | 0.5 | 3.3 | 7 | μs |
| $t_{wake(RxD)}$ | Minimum pulse width on RxD (See Figure 4) | 5 μs $t_{WAKE}$, $C_{RxD}$ = 15 pF | 0.5 | – | – | μs |
| $t_{dom(TxD)}$ | TxD dominant time for time-out | $V_{TxD}$ = 0 V | 1.2 | 2.6 | 4 | ms |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Values based on design and characterization, not tested in production

## MEASUREMENT SETUPS AND DEFINITIONS




* On NCV7349−3 $V_{CC}$ is replaced by $V_{IO}$

**Figure 5. Transceiver Timing Diagram**

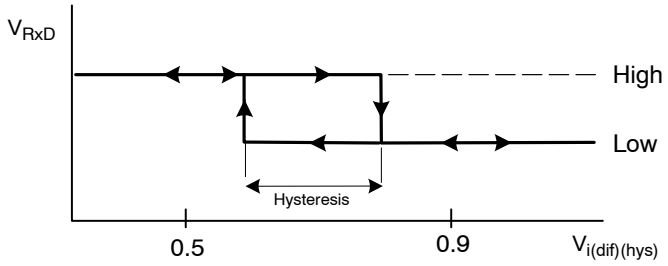



**Figure 6. Hysteresis of the Receiver**

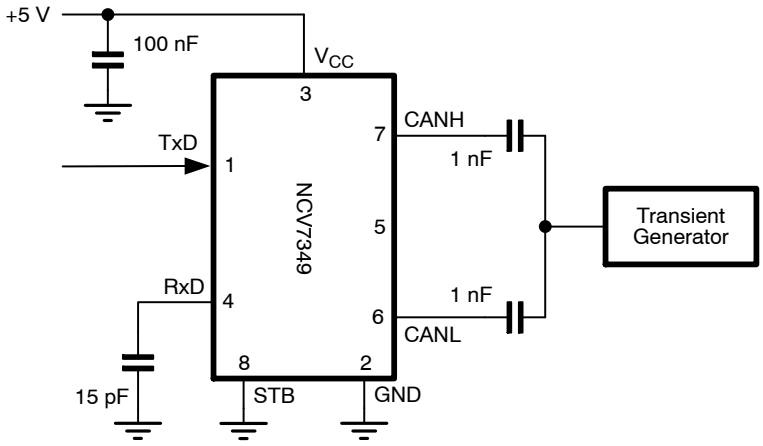



**Figure 7. Test Circuit for Automotive Transients**

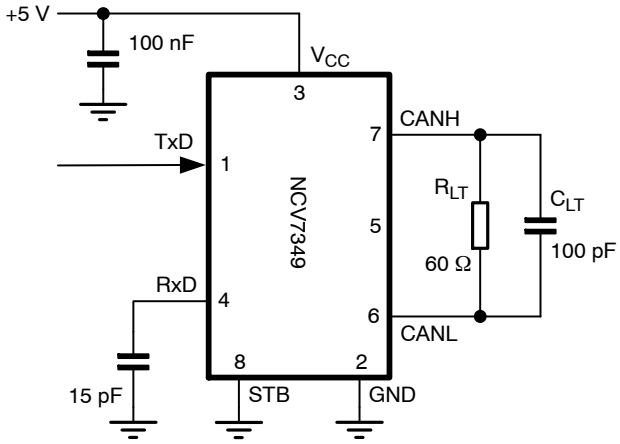



**Figure 8. Test Circuit for Timing Characteristics**

## DEVICE ORDERING INFORMATION

| Part Number | Description | Temperature Range | Package | Shipping† |
|---|---|---|---|---|
| NCV7349D10R2G | High Speed Low Power CAN Transceiver for the Japanese Market | −40°C to +125°C | SOIC 150 8 GREEN (Matte Sn, JEDEC MS-012) (Pb-Free) | 3,000 / Tape & Reel |
| NCV7349D13R2G | High Speed Low Power CAN Transceiver for the Japanese Market with $V_{IO}$ pin | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

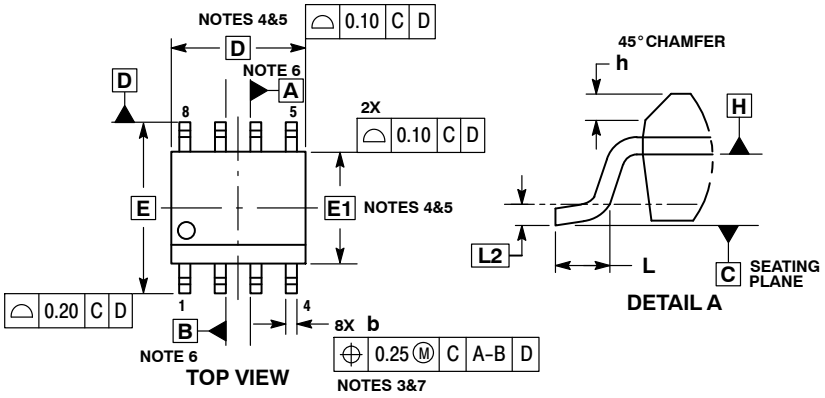
## REVISION HISTORY

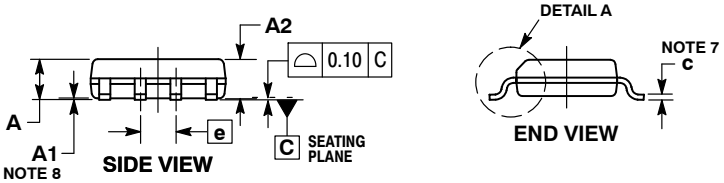
| Revision | Description of Changes | Date |
|---|---|---|
| 2 | Rebranded the Data Sheet to **onsemi** format. | 5/21/2025 |

**SCALE 1:1**

**SOIC−8**
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

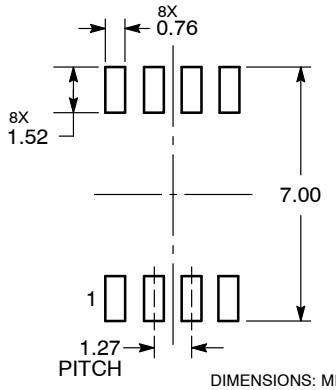



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | --- |
| b | 0.31 | 0.51 |
| c | 0.10 | 0.25 |
| D | 4.90 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| h | 0.25 | 0.41 |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |

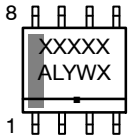
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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