NCV451

3A Ultra-Small Low Ron and Controlled Load Switch with Auto-Discharge Path

The NCV451 is a very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with NMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail.

Proposed in a wide input voltage range from 0.75 V to 5.5 V, in a small DFNW6 2.2 x 2 mm, 0.65 pitch package.

Features

- 0.75 V – 5.5 V Operating Range
- 21 mΩ N MOSFET from 3.6 V to 5.5 V
- 22 mΩ N MOSFET from 1 V to 3.3 V
- DC Current Up to 3 A
- Output Auto−Discharge
- Active High EN Pin
- DFNW6 2.2 x 2 mm, 0.65 pitch
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- ADAS System
- Camera Module
- Power Management

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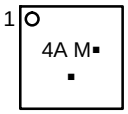
DFNW6
CASE 507AF

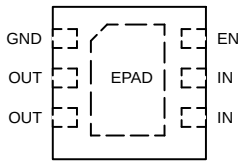
MARKING DIAGRAM



4A	= Specific Device Code
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

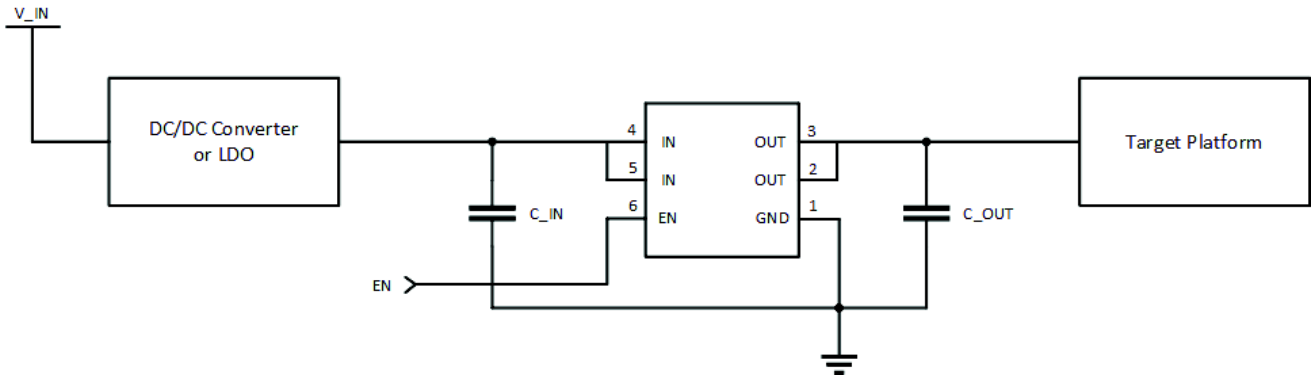


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	4, 5	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	1	POWER	Ground connection.
EN	6	INPUT	Enable input, logic high turns on power switch.
OUT	2, 3	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.
EPAD	7	POWER	Exposed pad, connect to ground potential.

BLOCK DIAGRAM

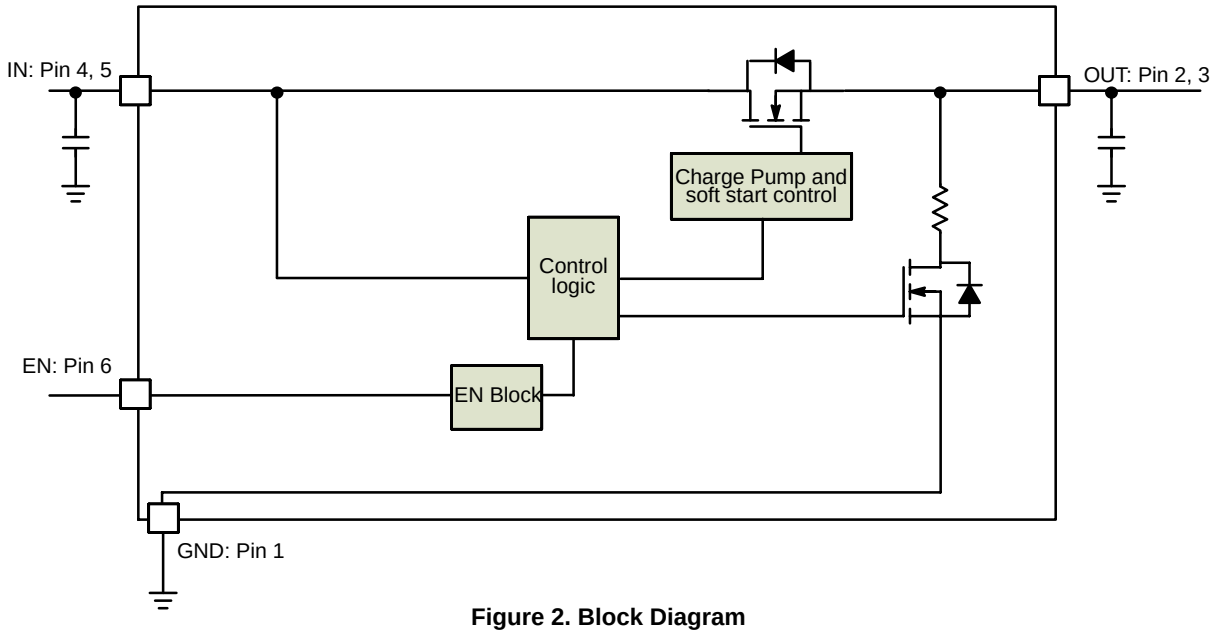


Figure 2. Block Diagram

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
IN, OUT, EN, Pins: (Note 1)	$V_{EN,}$ $V_{IN,}$ V_{OUT}	−0.3 to + 7.0	V
From IN to OUT Pins: Input/Output (Note 1)	$V_{IN,}$ V_{OUT}	0 to + 7.0	V
Human Body Model (HBM) ESD Rating are (Notes 1 and 2)	ESD HBM	1.5	kV
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±1.5 kV per JEDEC standard: JESD22−A114 for all pins.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		0.75		5.5	V
V_{EN}	Enable Voltage		0		5.5	V
T_A	Ambient Temperature Range		−40	25	+105	°C
T_J	Junction Temperature Range		−40	25	+125	°C
C_{IN}	Decoupling input capacitor		1			μF
C_{OUT}	Decoupling output capacitor		1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	(Note 4)		122		°C/W
I_{OUT}	Maximum DC current				3	A
P_D	Power Dissipation Rating (Note 5)			0.164		W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Value based on 1s0p board with copper 650 mm^2 (or 1 in^2) of 1 oz thickness and FR4 PCB substrate
5. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J between −40°C to +125°C for V_{IN} between 0.75 V to 5.0 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{IN} = 3.6 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 5 V	I_{OUT} = 200 mA, T_A = 25°C		21	40	mΩ
			T_J = 125°C			50	
		V_{IN} = 3.6 V	I_{OUT} = 200 mA, T_A = 25°C		21	40	
			T_J = 125°C			50	
		V_{IN} = 3.3 V	I_{OUT} = 200 mA, T_A = 25°C		21	40	
			T_J = 125°C			50	
		V_{IN} = 2.5 V	I_{OUT} = 200 mA, T_A = 25°C		21	40	
			T_J = 125°C			50	
		V_{IN} = 1.8 V	I_{OUT} = 200 mA, T_A = 25°C		21	40	
			T_J = 125°C			50	
		V_{IN} = 1.0 V	I_{OUT} = 200 mA, T_A = 25°C		23	45	
			T_J = 125°C			55	
		V_{IN} = 0.75 V	I_{OUT} = 200 mA, T_A = 25°C		25	45	
			T_J = 125°C			55	
R_{DIS}	Output discharge path	EN = low			1.0	1.7	kΩ
V_{IH}	High−level input voltage			0.8			V
V_{IL}	Low−level input voltage					0.4	
I_{EN}	EN pin leakage current	V_{IN} = 3.6 V				0.1	μA
QUIESCENT CURRENT							
Istd	Standby current	V_{IN} = 4.2 V	EN = low, No load, T_A = −40°C to 85°C		0.9	3	μA
Iq	Quiescent current	V_{IN} = 3.6 V V_{IN} = 2.5 V V_{IN} = 1.8 V V_{IN} = 1.2 V V_{IN} = 1.0 V V_{IN} = 0.75 V	EN = high, No load (Note 6)		8	15	μA
TIMINGS							
T_{EN}	Enable time	V_{IN} = 3.6 V (Note 7)	R_L = 25 Ω, C_{OUT} = 1 μF		600		μs
T_R	Output rise time		R_L = 25 Ω, C_{OUT} = 1 μF		800		
T_{ON}	ON time (T_{EN} + T_R)		R_L = 25 Ω, C_{OUT} = 1 μF		1400		
T_F	Output fall time		R_L = 25 Ω, C_{OUT} = 1 μF		55		
TIMINGS							
T_{EN}	Enable time	V_{IN} = 3.6 V (Note 7)	R_L = 10 Ω, C_{OUT} = 0.1 μF		540		μs
T_R	Output rise time		R_L = 10 Ω, C_{OUT} = 0.1 μF		670		
T_{ON}	ON time (T_{EN} + T_R)		R_L = 10 Ω, C_{OUT} = 0.1 μF		1210		
T_F	Output fall time		R_L = 10 Ω, C_{OUT} = 0.1 μF		2.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Production tested at V_{IN} = 3.6 V.
7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

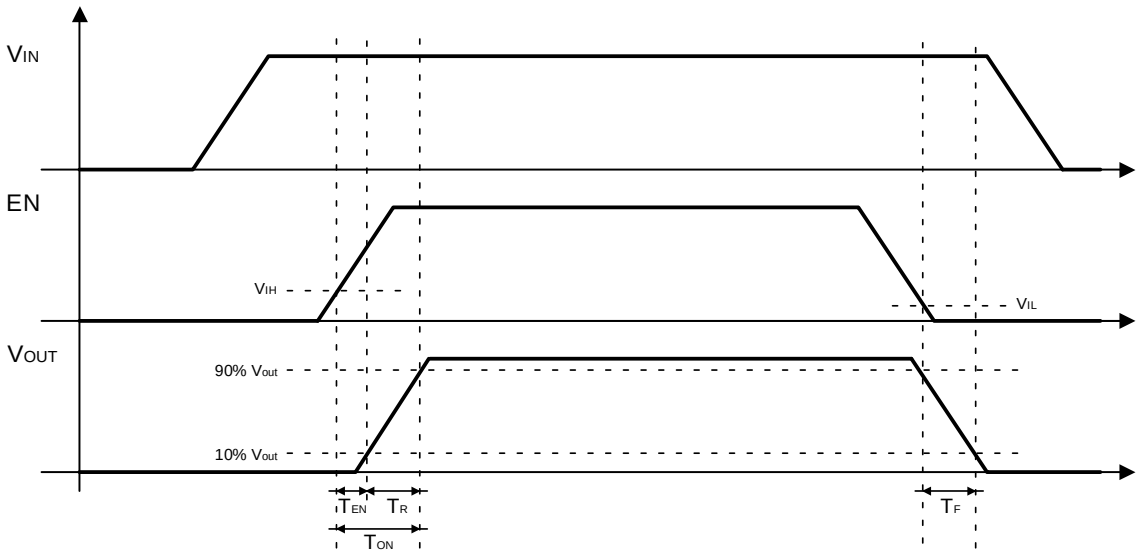


Figure 3. Enable, Rise and Fall Time

ELECTRICAL CURVES

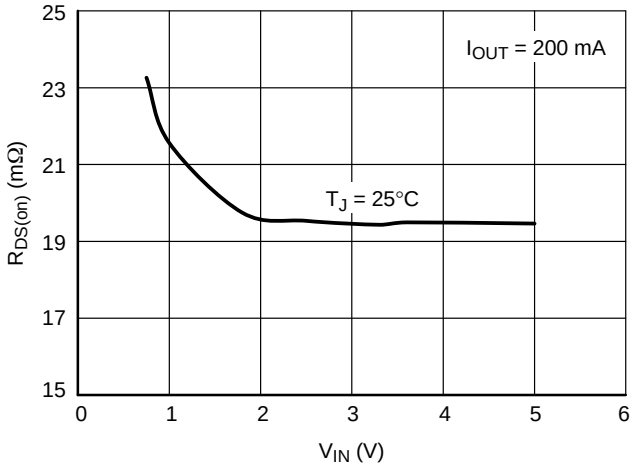


Figure 4. $R_{DS(on)}$ vs. V_{IN}, Low Load

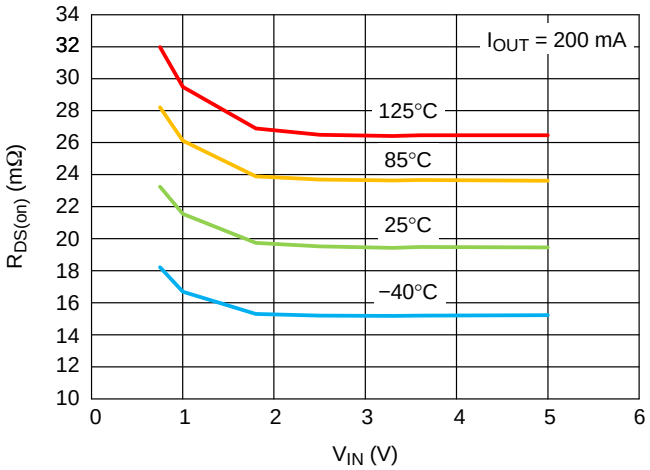


Figure 5. $R_{DS(on)}$ vs. V_{IN}, Low Load, Multi Junction Temperature

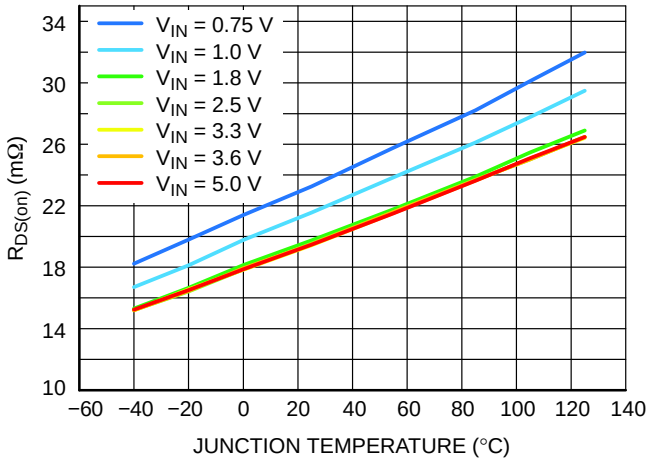


Figure 6. $R_{DS(on)}$ vs. Temperature, Multi V_{IN} Voltage

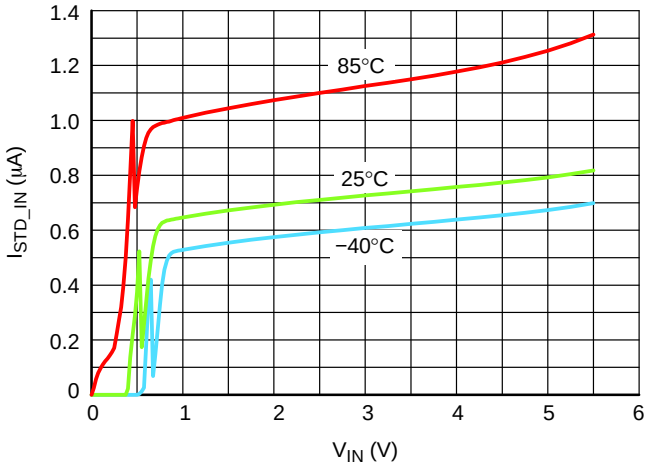


Figure 7. Standby Current (μA) vs. V_{IN}, Multi Junction Temperature

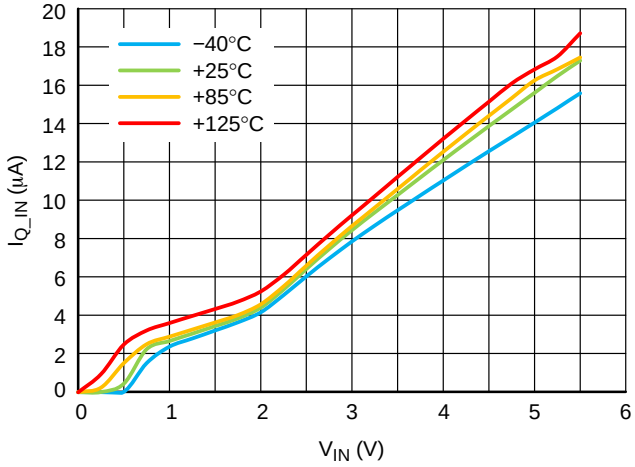


Figure 8. Quiescent Current (μA) vs. V_{IN}, Multi Junction Temperature

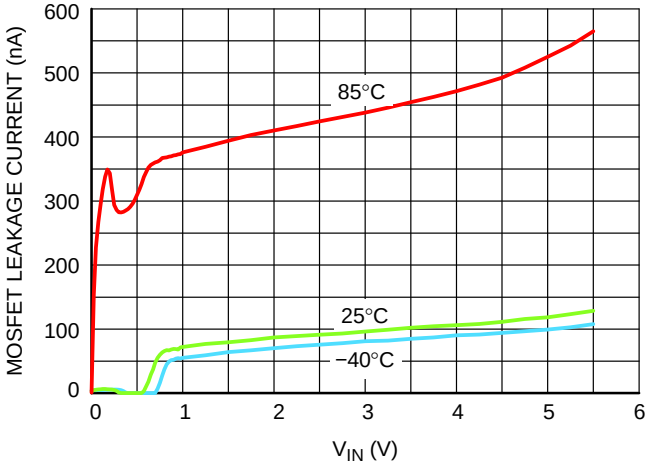


Figure 9. MOSFET Leakage Current (nA) vs. V_{IN}, Multi Junction Temperature

ELECTRICAL CURVES

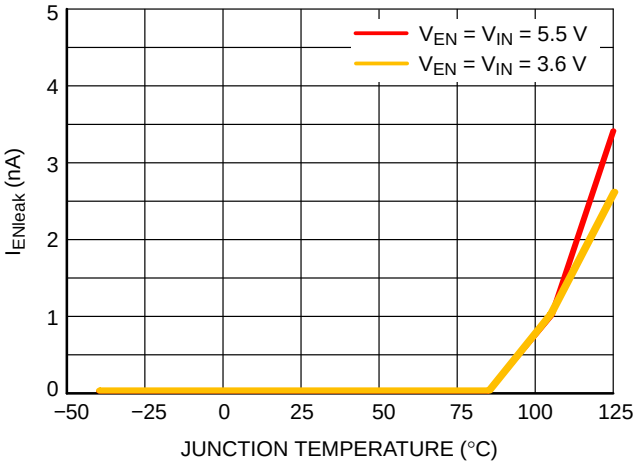


Figure 10. EN Pin Leakage vs. Junction Temperature

FUNCTIONAL DESCRIPTION

Overview

The NCV451 is a high side N channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing N−MOSFET switch off.

The IN/OUT path is activated with a minimum of Vin of 0.75 V and EN forced to high level.

Auto Discharge

N−MOSFET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 0.75 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at R_{DIS}.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)

$R_{DS(on)}$ = Power MOSFET on resistance (Ω)

I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)

$R_{\theta JA}$ = Package thermal resistance (°C/W)

T_A = Ambient temperature (°C)

PCB Recommendations

The NCV451 integrates an up to 3 A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across 2 internal inners.

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCV451AMNWTBG	4A	Auto Discharge 1 kΩ	DFNW6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

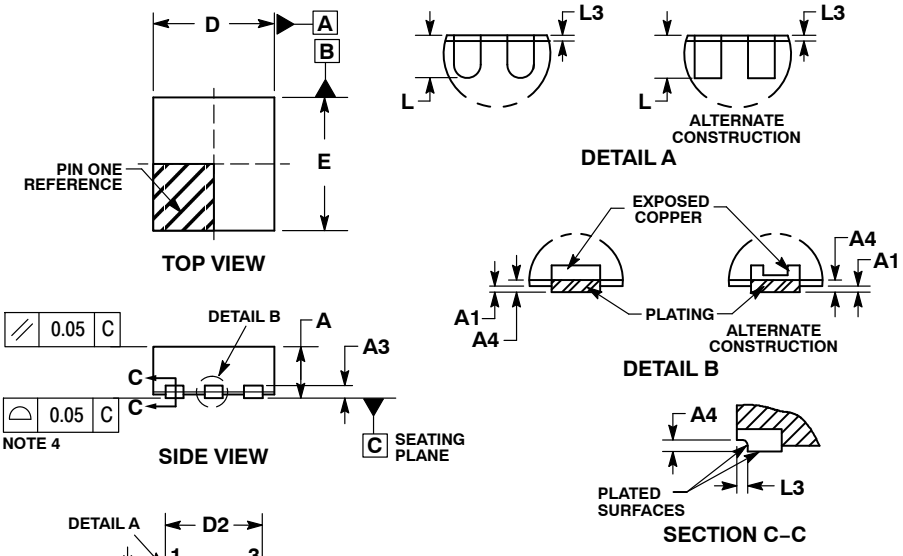
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

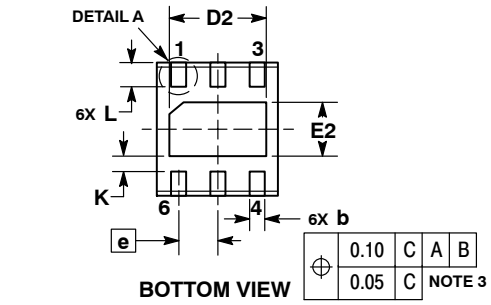
ON Semiconductor®

SCALE 2:1

DFNW6 2.0x2.2, 0.65P
CASE 507AF
ISSUE O

DATE 18 AUG 2017

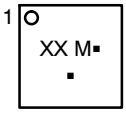




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	---	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.10	2.20	2.30
E2	0.79	0.89	0.99
e		0.65 BSC	
K		0.26 REF	
L	0.30	0.40	0.50
L3		0.05 REF	

GENERIC MARKING DIAGRAM*

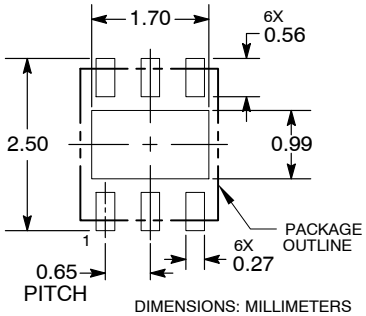


XX = Specific Device Code
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON73486G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFNW6 2.0X2.2, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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