Self Test Ground Fault Circuit Interrupter (GFCI)

NCS37015

1

QFN16
CASE 485FQ

The NCS37015 is a UL943 compliant signal processor for GFCI applications with self test. The device integrates a flexible power supply (including a 12 V shunt and two 3.3 V internal series regulators), differential fault, and grounded−neutral detection circuits. Self test is monitored at start up and then every 17 minutes.

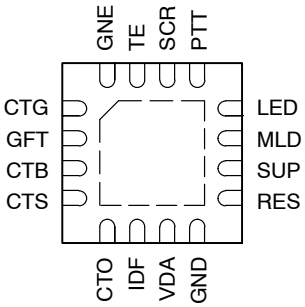
Features

- Meets UL943 Self−test GFCI Requirements
- 4.0 – 12 Volt Operation (120−480 V AC mains with the appropriate series impedance)
- −40°C to 95°C
- Typical 575 μA Quiescent Current @ 11 V
- 16 Pin QFN
- Inverted and Latched SCR Output to Facilitate a Solenoid Operation
- Self Syncing Internal Oscillator adjusts to AC Mains Frequency to Guarantee Full Resolution on 60 Hz Distribution Systems
- Optimized Solenoid Deployment (coil is not energized near the AC mains zero crossings)
- Power Supply Monitor that Verifies Full Diode Bridge Operation
- Tiered Trip Times that Increase Immunity to Noise
- Under−voltage Detection that Allows for Increased Operation at Lower AC Input Voltages

Typical Applications

- Portable GFCI Plugs
- GFCI Receptacles

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM

37015	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

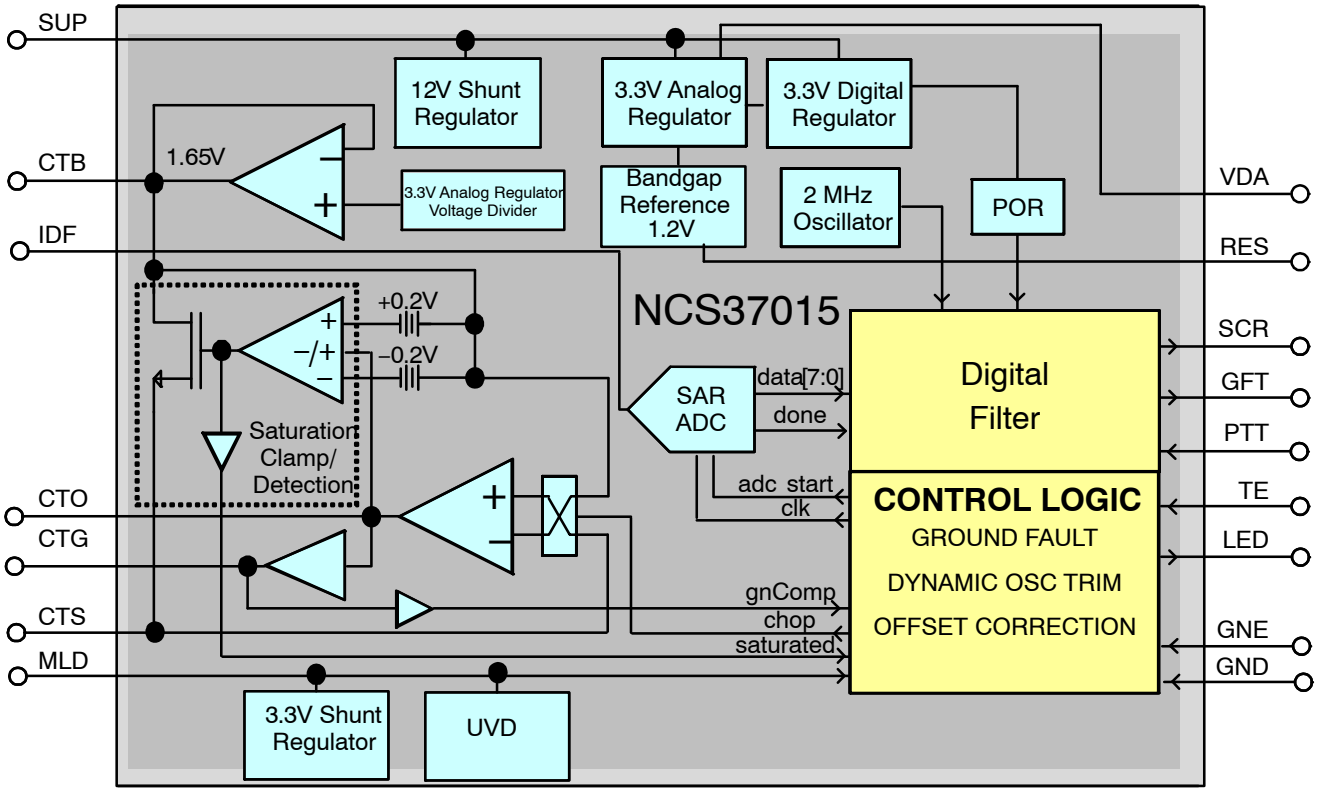


Figure 1. Simplified Block Diagram

Table 1. QFN PIN DESCRIPTION

Pin #	Name	Pad Description
1	CTG	Ground Neutral current transformer stimulus
2	GFT	Differential self test output signal
3	CTB	Differential current transformer bias voltage
4	CTS	Differential current input
5	CTO	Differential current to voltage output
6	IDF	Differential low pass filter/ADC input
7	VDA	Analog 3.3 V regulator output/ ADC reference voltage
8	GND	Electronics ground
9	RES	Reference current bias input
10	SUP	Power supply input
11	MLD	Mains level/under voltage detector
12	LED	End of life LED drive
13	PTT	Push to test input
14	SCR	SCR gate drive signal
15	TE	Test enable
16	GNE	Ground−neutral enable input

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	Vs	13.5	V
Supply Current	Is	10	mA
Input Voltage Range (Note 3)	V_{in}	−0.3 to 3.6	V
Output Voltage Range	V_{out}	−0.3 to 3.6 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	140	°C
Storage Temperature Range	TSTG	−65 to 150	°C
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 4)	ESD_{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 5)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation above the Recommended Operating Conditions is not implied. Extended
2. Exposure to stresses above the Recommended Operating Conditions may affect device reliability.
3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JS−001−2012
   ESD Charge Device Model tested per JESD22−C101−F
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78D
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3x3.3 mm (Note 6) Thermal Resistance, Junction−to−Air (Note 7)	$R_{\theta JA}$	64	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

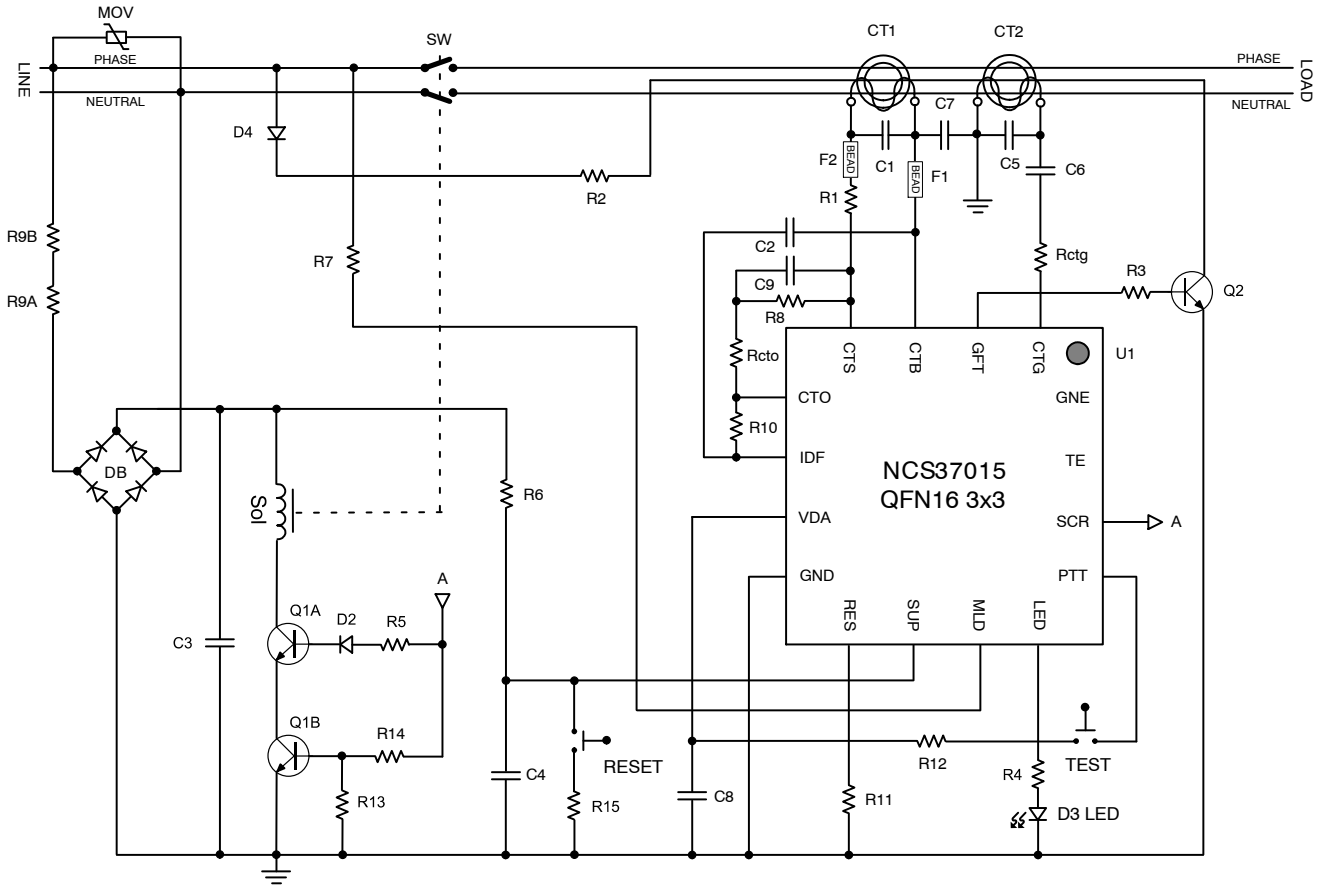
Table 4. OPERATING RANGES (Unless otherwise noted, I_{SUP} = 3 mA, MLD input = 60 Hz, Refer to Figure 2)

Parameter	Conditions	Min	Typ	Max	Units
Operating Temperature	Ambient	−40		95	C
Shunt Regulator Voltage	SUP to GND, I_{SUP} = 1 mA		12	13	V
Shunt Regulator Current	I_{SUP}			10	mA
Quiescent Current	I_{SUP}, SUP = 10.5 V		575	750	μA
RMS Trip Threshold Voltage	IDF to CTB, R8 = 32 kΩ, R_{CTO} = 500 Ω	191	203	215	mV
SCR Trigger Current	I_{SCR}, SCR = 1 V, I_{SHUNT} < 6 mA	4			mA
SCR Trigger Output Voltage	SCR to GND, SUP < 4 V	3		3.6	V
LED Output Voltage	LED to GND, SUP < 4 V	3		3.6	V
CTB Bias Voltage	CTB to GND, VDA = 3.3 V		1.65		V
CTS−CTB Absolute Offset Voltage	CTS−CTB	−250		250	μV
Fault Response Time	6 mA ≤ I_{DIFF} < 10 mA			125	ms
Fault Response Time	10 mA ≤ I_{DIFF} < 15 mA			95	ms
Fault Response Time	15 mA ≤ I_{DIFF} < 17.5 mA			75	ms
Fault Response Time	17.5 mA ≤ I_{DIFF} < 20 mA			60	ms
Fault Response Time	20 mA ≤ I_{DIFF} < 22.5 mA			50	ms
Fault Response Time	22.5 mA ≤ I_{DIFF} < 26.5 mA			40	ms
Fault Response Time	26.5 mA ≤ I_{DIFF} < 29 mA			35	ms
Fault Response Time	29 mA ≤ I_{DIFF} < 33 mA			25	ms
Fault Response Time	I_{DIFF} ≥ 33 mA			20	ms
CTG Comparator Threshold	CTG to GND, VDA = 3.3 V		1.95		V
CTG Timer	CTG > Threshold		45		μs
CTG GN Trip Frequency	CTG to GND	2		7	kHz
GN Response Time	Continuous GN Fault			350	ms
Internal Oscillator Frequency	F_{AC} = 60 Hz ±0.1	1.8	2	2.2	MHz
Under Voltage Detect	V_{AC} to GND, R7 = 1 MΩ, ±1%	80	87	95	Vrms
MLD Max Clamp Current	I_{MLD} Max Sink Current			400	μA
MLD Pull Down Current	MLD = 1 V		500		nA
First ST Timer	VDA > 3 V	1.7	2	2.3	seconds
Periodic ST Timer, Pass	Steady State, ST Pass	15	17	20	minutes
LED Blink Frequency	First ST Failure	1.8	2	2.2	Hz
ST Cycle GF Pass Window	I_{DIFF} Ground Fault	6		14	mA
MLD Pin Check Wait Time to Enable LED	No MLD signal		500		ms
MLD Pin Continuity Pass	Input Frequency	25			Hz
LED Blink Frequency	No MLD signal	1.5	2	2.5	Hz
MLD Pin Check Wait Time to Enable SCR	No MLD signal		6		minutes

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

APPLICATIONS INFORMATION



Note: A practical design for a portable GFCI application can be changed based on the requirements of a latching mechanism of a switch.

Figure 2. Portable GFCI Application Diagram (example)

Table 5. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
NPN	Q1A, Q1B, Q2	–	MMBT6517LT1−D
Diode Bridge	DB	–	
Diode	D2, D4	–	1N4007
LED	D3	–	LED for self test failure
Capacitor	C1	33 nF	Differential current filter capacitor
Capacitor	C2	56 nF	Anti−aliasing filter (1 kHz corner frequency)
Capacitor	C3	10 μF	Solenoid firming capacitor
Capacitor	C4	1 μF	SUP pin holding capacitor
Capacitor	C5	22−220 pF	Ground Neutral CT resonance capacitor
Capacitor	C6	4.7−47 nF	Ground Neutral CT AC coupler
Capacitor	C7	1 nF	CTB bias filter
Capacitor	C8	1 μF	Analog 3.3 V regulator filter
Capacitor	C9	1 nF	High frequency filter
Capacitor	C10	0.1−1 nF	High frequency filter for zero cross
Resistor	R1	243 Ω	Precision resistor (1%) differential low pass filter
Resistor	R2	–	Sets a resistance to create 8 mA fault current
Resistor	R3	10 kΩ	Sets the current in the base of Q2
Resistor	R4	6.8 kΩ	Limits current to the LED D3
Resistor	R5	20−47 kΩ	Sets base current in Q1A
Resistor	R6	72 kΩ	Power supply current limit
Resistor	R7	1 MΩ	MLD current limit/under voltage attenuator
Resistor	R8	32 kΩ	Precision resistor (1%) for differential trip level
Resistor	R9A, R9B	3.3−15 kΩ	Diode bridge short current limit
Resistor	R10	10−20 kΩ	Differential filter resistor
Resistor	R11	120 kΩ	Precision resistor (1%), Current reference bias resistor
Resistor	R12	10 kΩ	Test button pull−up resistor
Resistor	R13	47 kΩ	Q1B base pull−down resistor
Resistor	R14	20−47 kΩ	Sets base current in Q1B
Resistor	R15	22 kΩ	Reset button pull−down resistor
Resistor	Rcto	0.47−1.5 kΩ	Precision resistor (1%), Sets the differential trip level at 5 mA_{RMS}
Resistor	Rctg	0 − 200 Ω	Sets the GN sensitivity
Current Transformer	CT1	800	Differential current transformer
Current Transformer	CT2	250	GN current transformer

Functional Description (refer to application circuit)

The NCS37015 provides for a single IC controller solution for ground fault, grounded neutral and self−test protection per UL standard UL943 for GFCI applications.

The key internal blocks include: 12 V shunt regulator, precision bandgap reference, two 3.3 V linear regulators (one for the digital and one for the analog circuit) sense amplifier with V_{OS} cancellation, 1.65 V reference for the CT, 2 MHz oscillator dynamically trimmed to the AC line frequency, 8 bit SAR ADC, comparators, digital filters and digital control logic.

To work more easily with portable GFCI applications the SCR pin will assert high on power−up. If a fault is detected or self−test fails the SCR pin will drive low and remain in this state until the part goes through a power on reset.

The internal shunt regulator clamps the SUP pin voltage at 12 volts. This provides the bias voltage for the analog (vda) and digital (vdd) internal circuitry via two 3.3 V linear regulators.

At POR detection (vda>2.475) the logic is reset and the bias circuitry is enabled, the LED pin will blink once for 250 ms. The MLD pin is continually checked for an input signal greater than 25 Hz. If the MLD signal is greater than 25 Hz, this test passes. If it fails, the LED blinking logic will be enabled. A six minute timer will start and if no MLD signal is detected, the SCR will be enabled. If a MLD signal occurs before the six minute timer and is longer than one minute, the timer will be reset.

The first self test (ST) cycle will occur at two seconds and thereafter every 17 minutes. During the ST cycle the GFT pin will be enabled and the CT current (set at 8 mA, R2) will be verified for two half cycles. If a ST cycle fails due to a low GF detection or a GF signal greater than 30 mA, the LED blinking logic will enable and the SCR pin will assert low.

The CT is biased at 1.65 volts. The sense amplifier monitors the ground fault current. This current is converted to a voltage level at the CTO pin which is the input to the ADC (IDF pin). The resistor R8 sets the GF threshold per the following equation:

$$I_{diff} = \frac{0.203 \times CT_1 \times \left(R_{CT1} + R_1 + 2\pi f_{AC} L_{CT1}\right)}{R_8 \times \left(R_{CT1} + 2\pi f_{AC} L_{CT1}\right)} \quad \text{(eq. 1)}$$

CT_1 = Turns ratio of differential CT

R_{CT1} = DC winding resistance of differential CT

f_{AC} = AC mains frequency

L_{CT1} = Inductance of differential CT

The ground fault detection circuit has different levels of time delay before the SCR is enabled:

6 mA to 10 mA	≤ 125 ms
10 mA to 15 mA	≤ 95 ms
15 mA to 17.5 mA	≤ 75 ms
17.5 mA to 20 mA	≤ 60 ms
20 mA to 22.5 mA	≤ 50 ms
22.5 mA to 26.5 mA	≤ 40 ms
26.5 mA to 29 mA	≤ 35 ms
29 mA to 33 mA	≤ 25 ms
>33 mA	≤ 20 ms

If a very high GF occurs and a greater than 200 mV signal occurs across the CT for greater than 1.4 ms, the SCR pin will be driven low immediately.

Note that the above equation is for an ideal CT. In practice, the GF threshold can be ±30% different and should be empirically set.

When the PTT pin is enabled for greater than 64ms and if the GNE PIN is high (16ms when GNE PIN is low), a ST cycle will be enabled. If the ST cycle passes, the SCR pin will drive to 0V and the LED blinks once. If the ST cycle fails, the LED will enable to blink and the SCR pin will drive to 0 V.

The PTT pin has a 50 kΩ pull down resistor. This pin is a CMOS input with hysteresis. To enable the PTT function, the input voltage should go above 2.4 volts.

The MLD pin monitors the phase and zero cross for the AC supply. The MLD circuit clamps the pin voltage to gnd and vda. When the pin is clamped at vda, the current is compared to a threshold so if the VAC voltage is below 87 V_{RMS}, the ST GF threshold will be reduced by 50%. This function provides for an AC under voltage detection which allows for the ST cycle to pass with a lower GF threshold. The AC UVD threshold can be user programmable by changing R7.

Grounded Neutral detection is accomplished by the addition of a GN coil to generate a “dormant oscillator” circuit. When a GN condition occurs, both the sense coil and GN coils are mutually coupled and the GN amplifier will oscillate. This oscillation can be observed at the CTG pin. When the oscillation at the CTG pin is above 1.95 volts for greater than 45 μs, and if this condition (oscillation) lasts for longer than 64 ms, the internal NCS37015 logic will disable the GN amplifier to stop the CTG oscillation for approximately 90 ms. The amplifier will be enabled again and if the oscillation on the CTG pin returns, the GN fault will be detected and the SCR will be enabled. This total sequence cycle takes a maximum of 175 ms. During power up, an additional maximum of 175 ms is required. The maximum time required during power up is 350 ms. The sensitivity of the GN detection can be changed by capacitor C6 and resistor Rctg. The frequency of this CTG oscillation needs to be in the 2 kHz to 7 kHz.

The internal oscillator is trimmed to 2 MHz when the AC frequency is 60 Hz. If the AC frequency is lower, the GF trip threshold response time will be slower and the GN sensitivity will be lower.

The RES pin will bias at 1.2 volts and should have an external precision 120 kΩ resistor connected to the GND pin. This resistor sets up an internal precision current source.

The TE pin is used for internal production testing only. A 50 kΩ pull down resistor is connected to this pin. This pin should be open or connected to the GND pin (preferred).

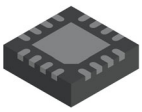
The GNE pin has an internal 50 kΩ pull up resistor connected to the internal 3.3 V supply. If this pin is pulled low, the GN function will be disabled.

Contact ON Semiconductor for self−test requirement details and noise filtering recommendations.

ORDERING INFORMATION

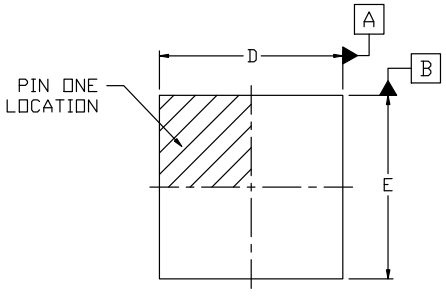
Device	Package	Shipping †
NCS37015MNTWG	QFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

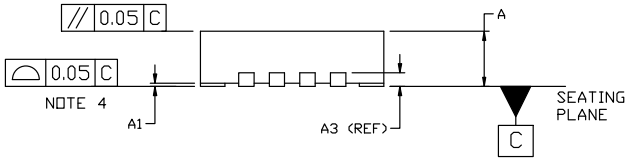


QFN16 3x3, 0.5P
CASE 485FQ
ISSUE B

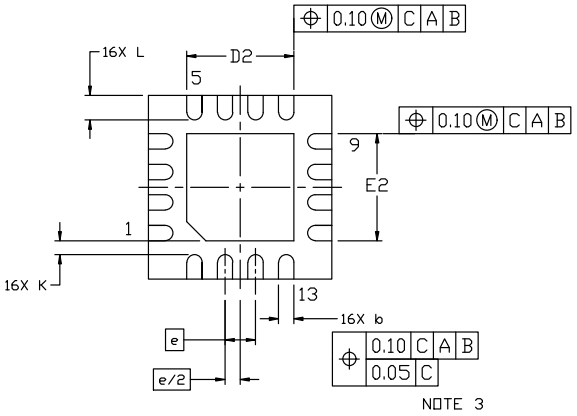
DATE 12 JUL 2022



TOP VIEW



SIDE VIEW

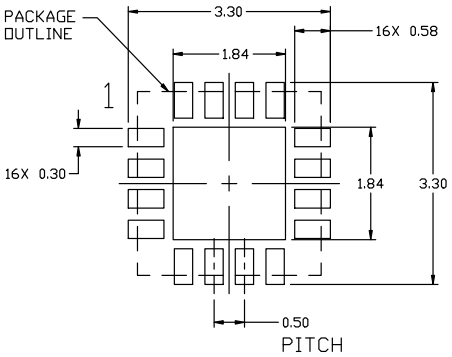


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASUREDBETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	2.90	3.00	3.10
D2	1.65	1.75	1.85
E	2.90	3.00	3.10
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON84763G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN16 3x3, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales