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DATA SHEET
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Operational Amplifier, Precision, Zero-Drift, 50 µV Offset, 0.25 µV/°C, 35 µA

NCS325, NCS2325, NCS4325

The NCS325, NCS2325 and NCS4325 are CMOS operational amplifiers providing precision performance. The Zero−Drift architecture allows for continuous auto−calibration, which provides very low offset, near−zero drift over time and temperature, and near flat 1/f noise at only 35 µA (max) quiescent current. These benefits make these devices ideal for precision DC applications. These op amps provide rail−to−rail input and output performance and are optimized for low voltage operation as low as 1.8 V and up to 5.5 V. The single channel NCS325 is available in the space−saving SOT23−5 package. The dual channel NCS2325 is available in Micro8 and SOIC−8. The quad channel NCS4325 is available in SOIC−14.

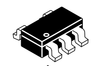
Features

- Low Offset Voltage: 14 µV typ, 50 µV max at 25°C for NCS325
- Zero Drift: 0.25 µV/°C max
- Low Noise: 1 µVpp, 0.1 Hz to 10 Hz
- Quiescent Current: 21 µA typ, 35 µA max at 25°C
- Supply Voltage: 1.8 V to 5.5 V
- Rail−to−Rail Input and Output
- Internal EMI Filtering
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Current Sensing

MARKING DIAGRAMS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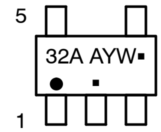
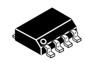
TSOP−5 (SOT23−5) SN SUFFIX CASE 483

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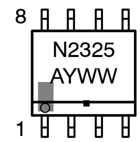
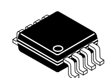
SOIC−8 D SUFFIX CASE 751

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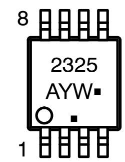
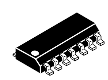
MSOP−8 DM SUFFIX CASE 846A

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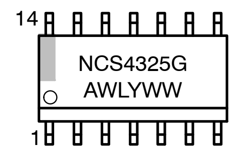
SOIC−14 D SUFFIX CASE 751A



A	= Assembly Location
Y	= Year
WL	= Wafer Lot
W or WW	= Work Week
G or ▪	= Pb−Free Package

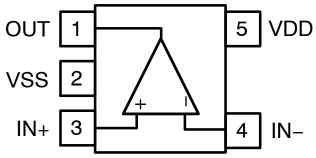
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

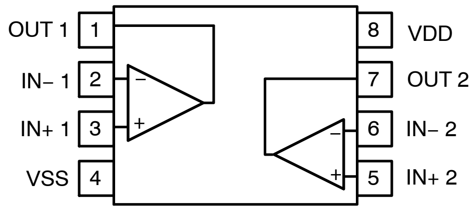
PIN CONNECTIONS

Single Channel
NCS325



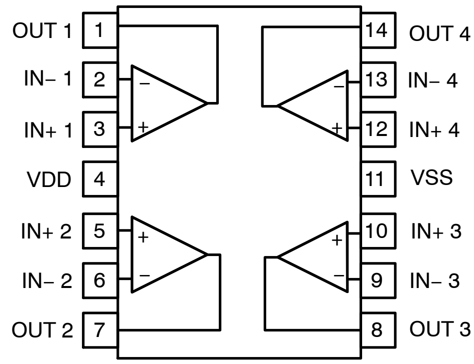
SOT23

Dual Channel
NCS2325



SOIC−8, MSOP−8

Quad Channel
NCS4325



SOIC14

ORDERING INFORMATION

Configuration	Device	Package	Shipping†
Single	NCS325SN2T1G	SOT23−5 / TSOP−5	3000 / Tape & Reel
Dual	NCS2325DR2G	SOIC−8	3000 / Tape & Reel
	NCS2325DMR2G	Micro8 / MSOP−8	4000 / Tape & Reel
Quad	NCS4325DR2G	SOIC−14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	6	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	(V_{SS}) − 0.3 to (V_{DD}) + 0.3	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	−40 to +150	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	+150	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	4000	V
Machine Model (MM)	200	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
4. Latch−up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION

Thermal Metric	Symbol	Package	Value	Unit
Junction to Ambient (Note 5)	θ_{JA}	SOT23−5 / TSOP−5	235	°C/W
		Micro8 / MSOP−8	298	
		SOIC−8	250	
		SOIC−14	216	

5. As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

OPERATING CONDITIONS

Parameter	Symbol	Range	Unit
Supply Voltage (V_{DD} − V_{SS})	V_S	1.8 to 5.5	V
Specified Operating Range	T_A	−40 to 125	°C
Input Common Mode Voltage Range	V_{ICMR}	V_{SS}−0.1 to V_{DD}+0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	NCS325: V_S = +5V		14	50	µV
		NCS2325, NCS4325: V_S = +5V		14	75	
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$	T_A = −40°C to 125°C		**0.02**	**0.25**	µV/°C
Input Bias Current	I_{IB}			±50		pA
Input Offset Current	I_{OS}			±100		pA
Common Mode Rejection Ratio	CMRR	NCS325: V_{SS}+0.3 < V_{CM} < V_{DD} − 0.3, V_S = 1.8 V	**85**	108		dB
		NCS325: V_{SS}+0.3 < V_{CM} < V_{DD} − 0.3, V_S = 5.5 V	**90**	110		
		NCS2325, NCS4325: V_{SS}+0.3 < V_{CM} < V_{DD} − 0.3, V_S = 5 V	**90**	110		
		V_{SS}−0.1 < V_{CM} < V_{DD} + 0.1, V_S = 1.8 V		80		
		V_{SS}−0.1 < V_{CM} < V_{DD} + 0.1, V_S = 5.5 V		92		
Input Resistance	R_{IN}			15		GΩ
Input Capacitance	C_{IN}	NCS325: Differential		1.8		pF
		NCS325: Common Mode		3.5		pF
		NCS2325, NCS4325: Differential		4.1		pF
		NCS2325, NCS4325: Common Mode		8.0		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	Output swing within V_{DD}		12	100	mV
Output Voltage Low	V_{OL}	Output swing within V_{SS}		8	100	mV
Short Circuit Current	I_{SC}			±5		mA
Open Loop Output Impedance	Z_{out-OL}	f = 350 kHz, I_O = 0 mA, V_S = 1.8 V		1.4		kΩ
		f = 350 kHz, I_O = 0 mA, V_S = 5.5 V		2.7		
Capacitive Load Drive	C_L		See Figure			
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f_{IN} = 1 kHz		100		nV / √Hz
Voltage Noise	e_{P-P}	f_{IN} = 0.01 Hz to 1 Hz		0.3		µV_{PP}
		f_{IN} = 0.1 Hz to 10 Hz		1		µV_{PP}
Current Noise Density	i_N	f_{IN} = 10 Hz		0.3		pA / √Hz
DYNAMIC PERFORMANCE						
Open Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, V_S = 5.5 V		114		dB
Gain Bandwidth Product	GBWP	NCS325: C_L = 100 pF, R_L = 10 kΩ		350		kHz
		NCS2325, NCS4325: C_L = 100 pF, R_L = 10 kΩ		270		
Phase Margin	ϕ_M	C_L = 100 pF		60		°
Gain Margin	A_M	C_L = 100 pF		20		dB
Slew Rate	SR	G = +1, C_L = 100 pF, Vs = 1.8 V		0.10		V/µs
		G = +1, C_L = 100 pF, Vs = 5.5 V		0.16		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR		100	107		dB
		T_A = −40°C to 125°C	**95**			
Turn−on Time	t_{ON}	V_S = 5 V		100		µs
Quiescent Current	I_Q	No load		21	**35**	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

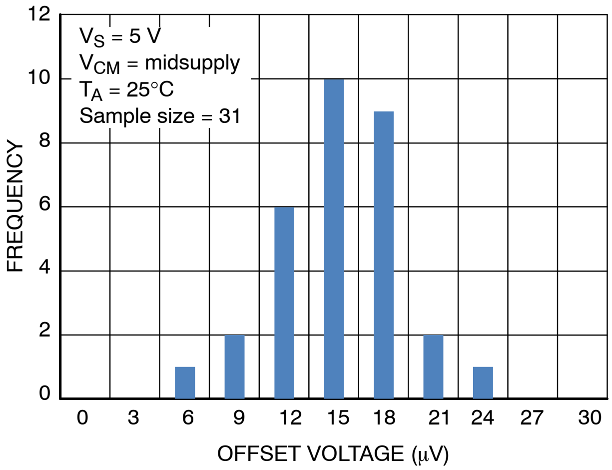


Figure 1. Offset Voltage Distribution

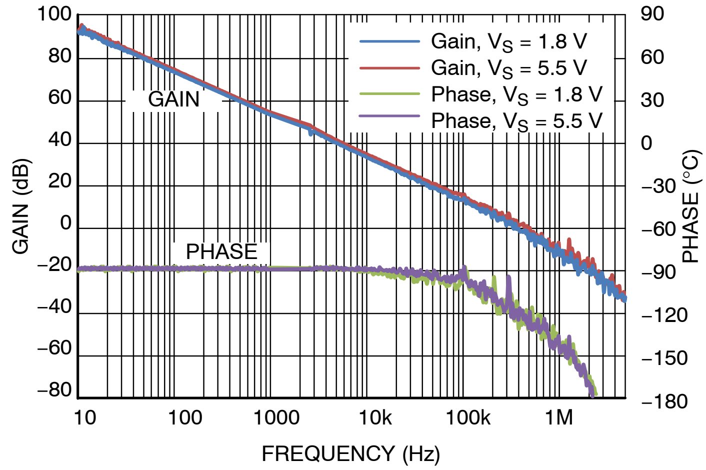


Figure 2. Gain and Phase vs. Frequency

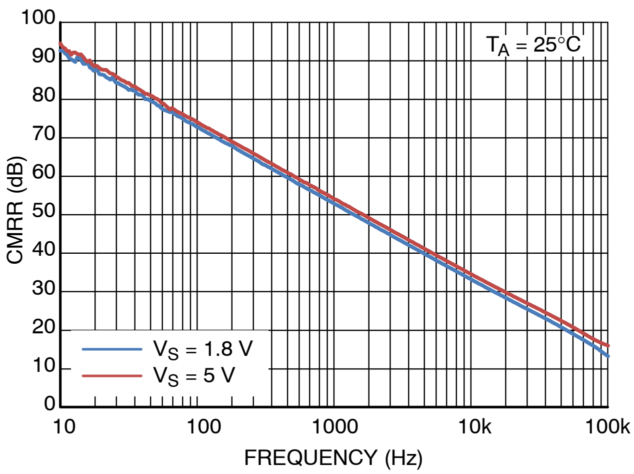


Figure 3. CMRR vs. Frequency

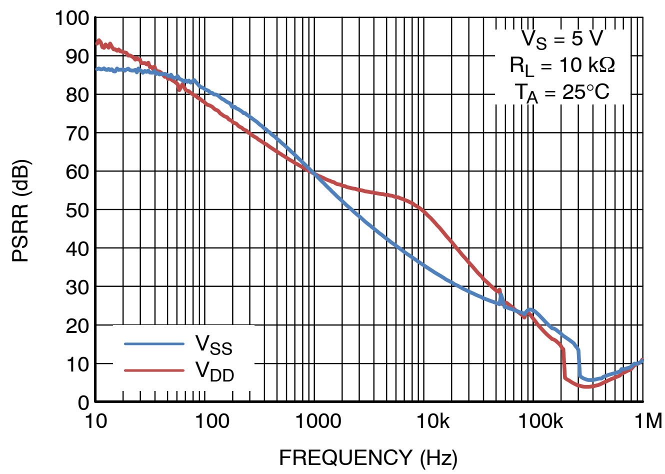


Figure 4. PSRR vs. Frequency

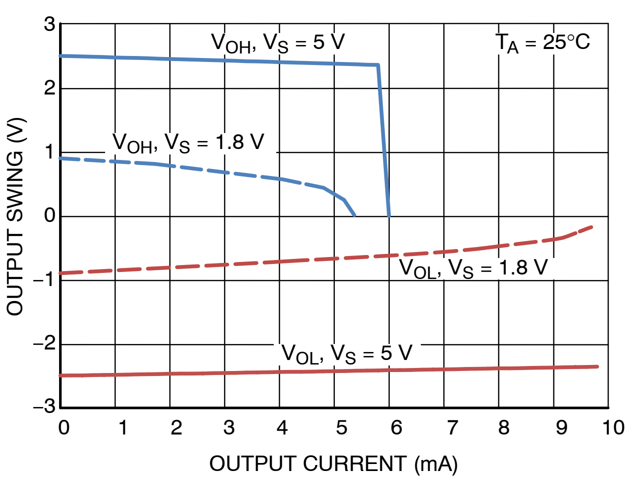


Figure 5. Output Voltage Swing vs. Output Current

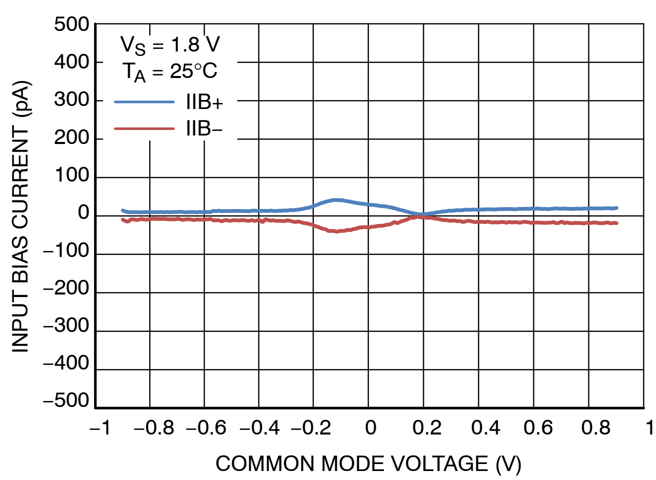


Figure 6. Input Bias Current vs. Common Mode Voltage, V_S = 1.8 V

TYPICAL CHARACTERISTICS (Continued)

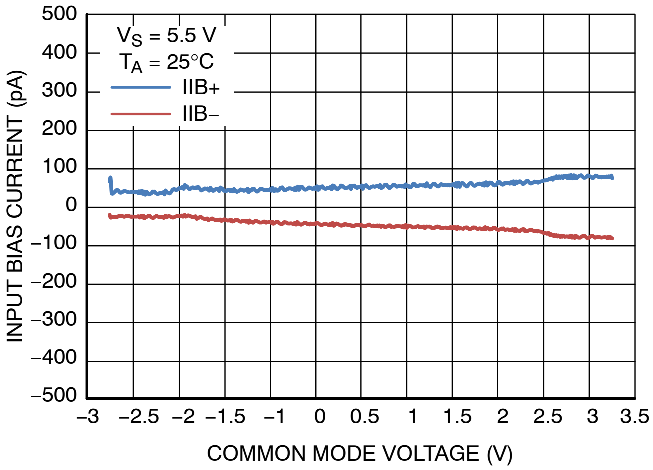


Figure 7. Input Bias Current vs. Common Mode Voltage, V_S = 5.5 V

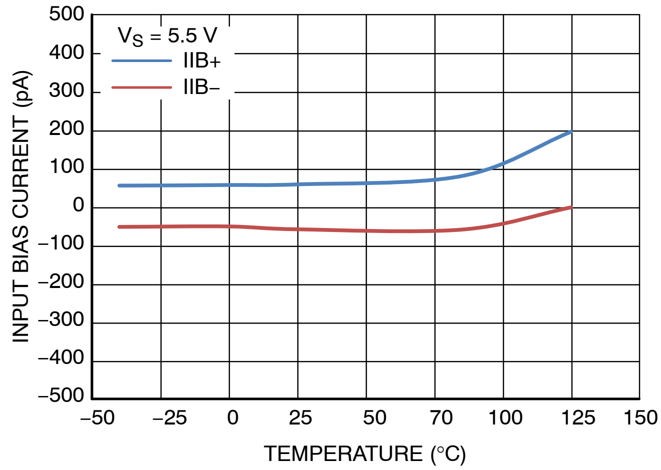


Figure 8. Input Bias Current vs. Temperature

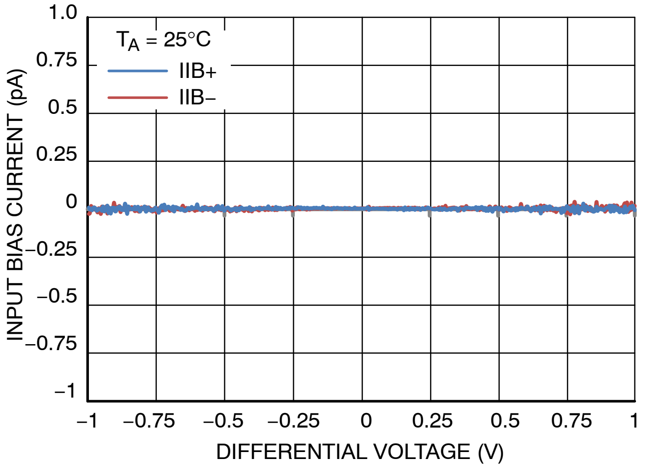


Figure 9. Input Bias Current vs. Input Differential Voltage

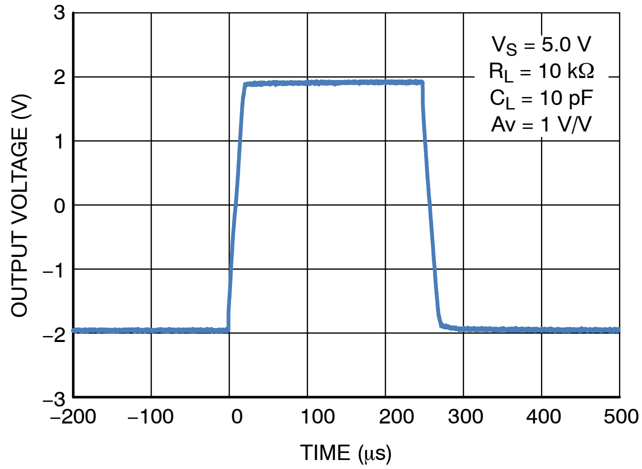


Figure 10. Large Signal Step Response

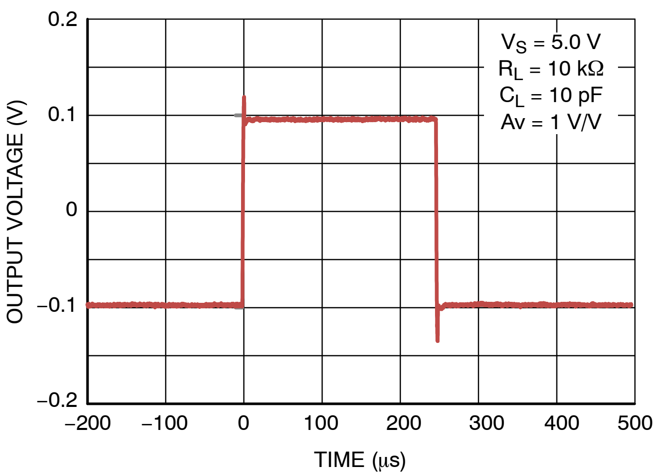


Figure 11. Small Signal Step Response

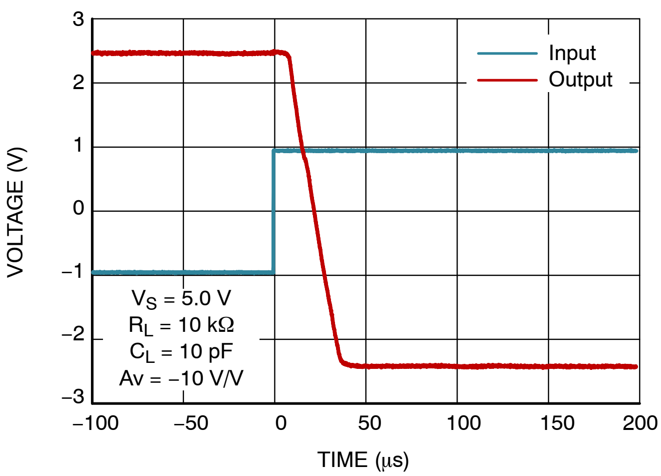


Figure 12. Positive Over Voltage Recovery

TYPICAL CHARACTERISTICS (Continued)

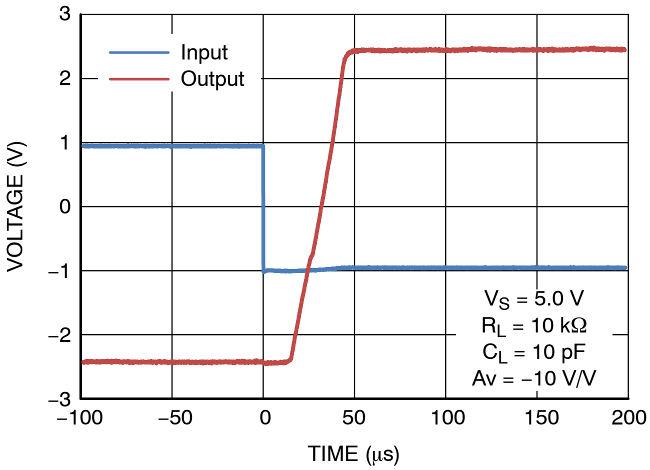


Figure 13. Negative Over Voltage Recovery

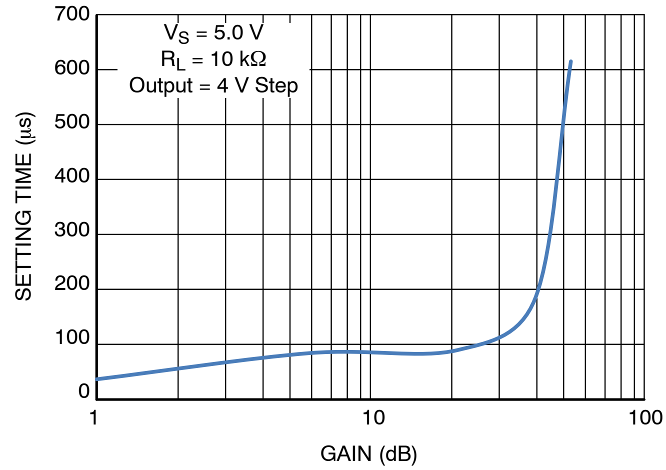


Figure 14. Setting Time vs. Closed Loop Gain

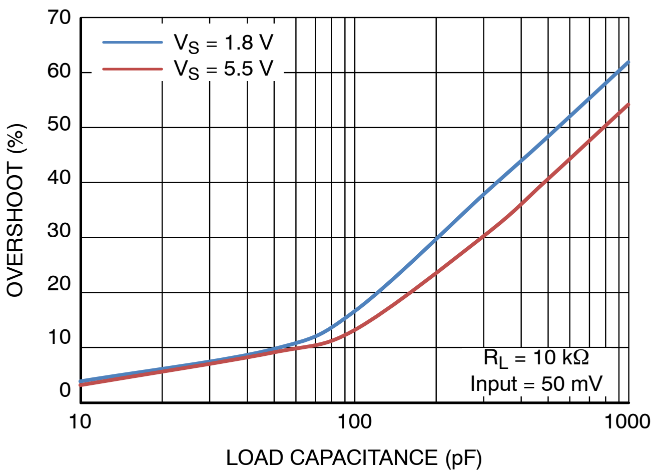


Figure 15. Small Signal Overshoot vs. Load Capacitance

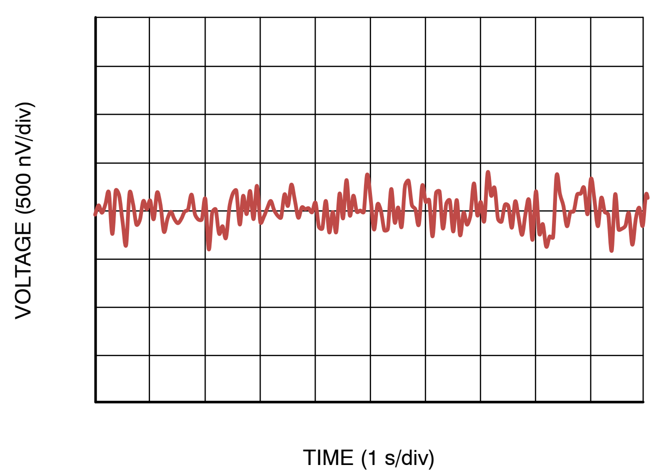


Figure 16. 0.1 Hz to 10 Hz Noise

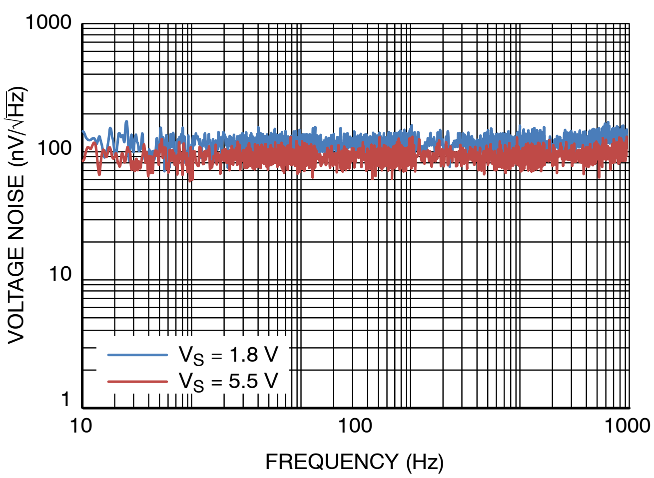


Figure 17. Voltage Noise Spectral Density vs. Frequency

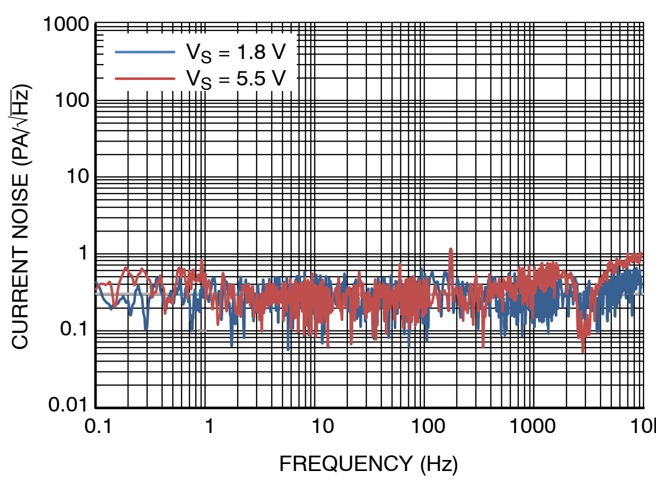


Figure 18. Current Noise Spectral Density vs. Frequency

TYPICAL CHARACTERISTICS (Continued)

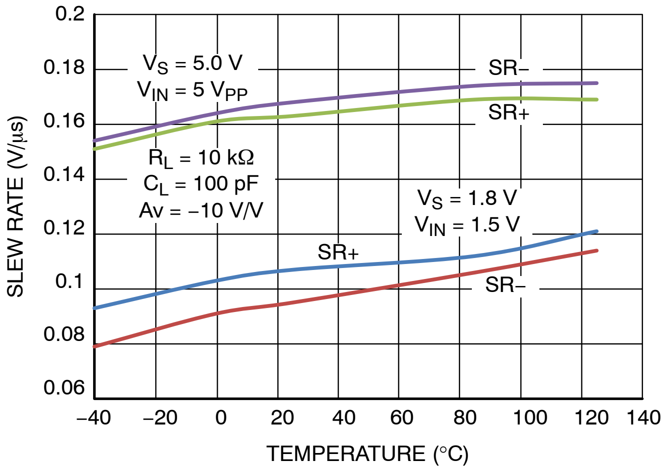


Figure 19. Slew Rate vs. Temperature

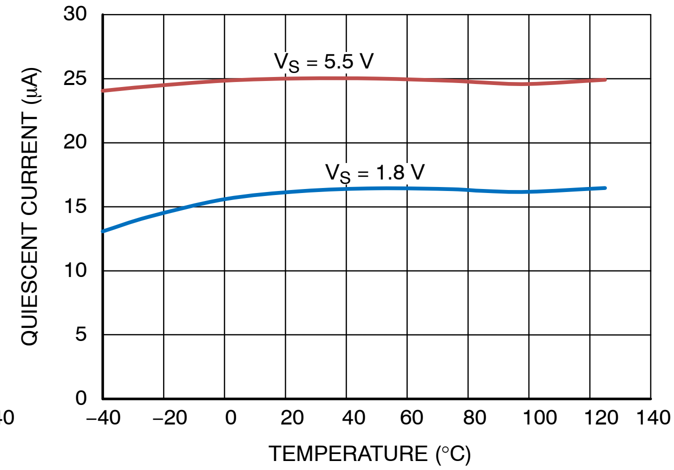


Figure 20. Quiescent Current vs. Temperature

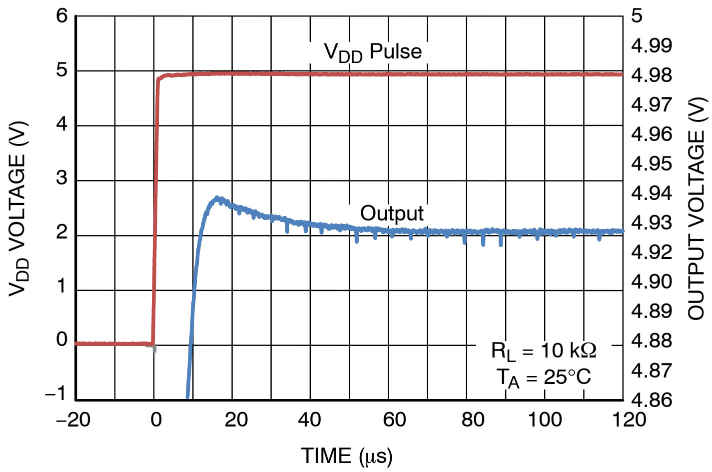


Figure 21. Turn−on Response

APPLICATIONS INFORMATION

INPUT VOLTAGE

The NCS325, NCS2325 and NCS4325 have rail−to−rail common mode input voltage range. Diodes between the inputs and the supply rails keep the input voltage from exceeding the rails.

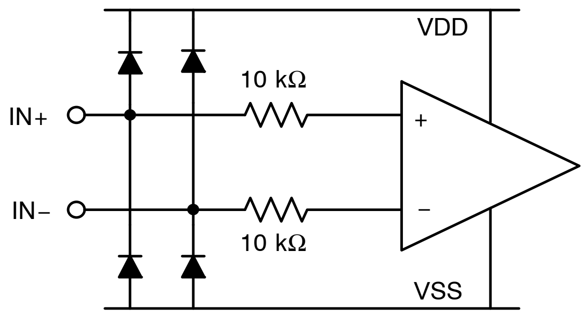


Figure 22. Equivalent Input Circuit

EMI SUSCEPTIBILITY AND INPUT FILTERING

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI−induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS325, NCS2325 and NCS4325 integrate a low−pass filter to decrease its sensitivity to EMI.

APPLICATION CIRCUITS

Low−Side Current Sensing

The goal of low−side current sensing is to detect over−current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

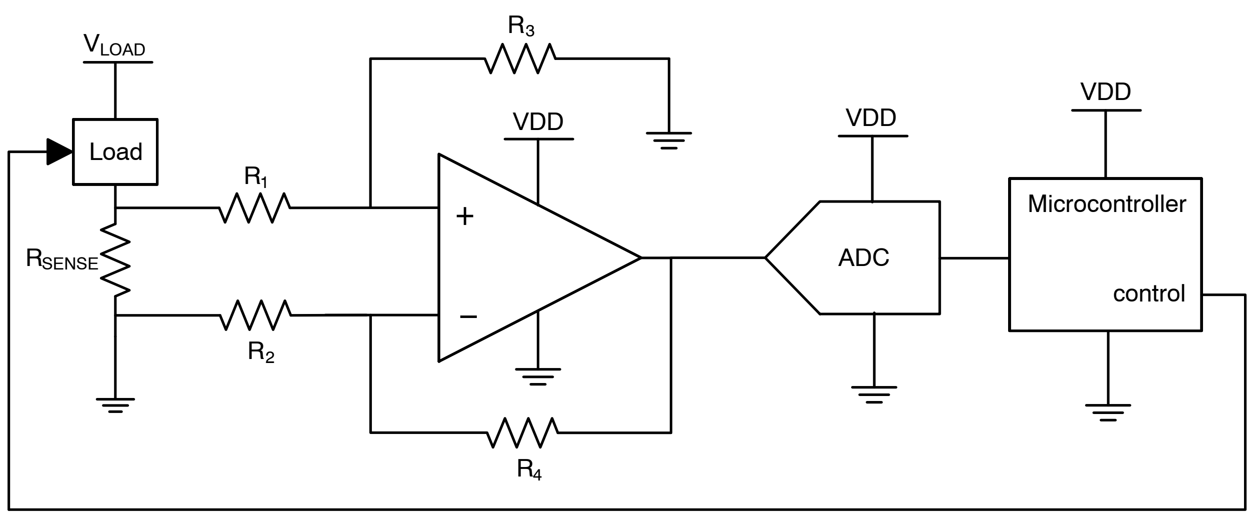


Figure 23. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 24. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

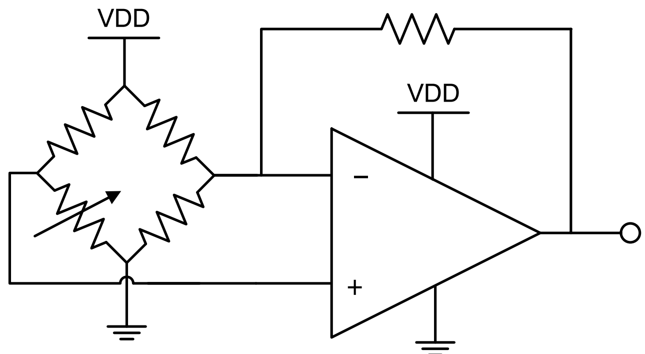
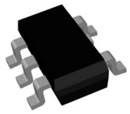


Figure 24. Bridge Circuit Amplification

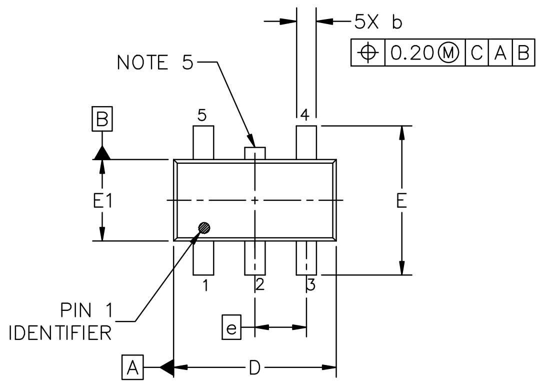
GENERAL LAYOUT GUIDELINES

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.

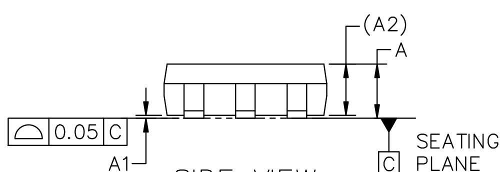


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

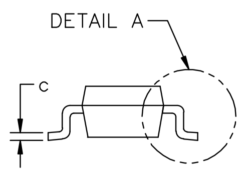
DATE 01 APR 2024



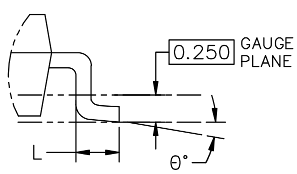
TOP VIEW



SIDE VIEW



END VIEW

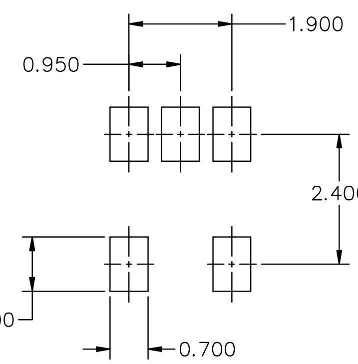


DETAIL "A"
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

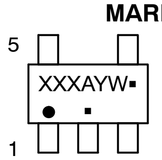
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



RECOMMENDED MOUNTING FOOTPRINT*

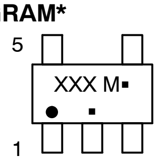
* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



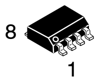
Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

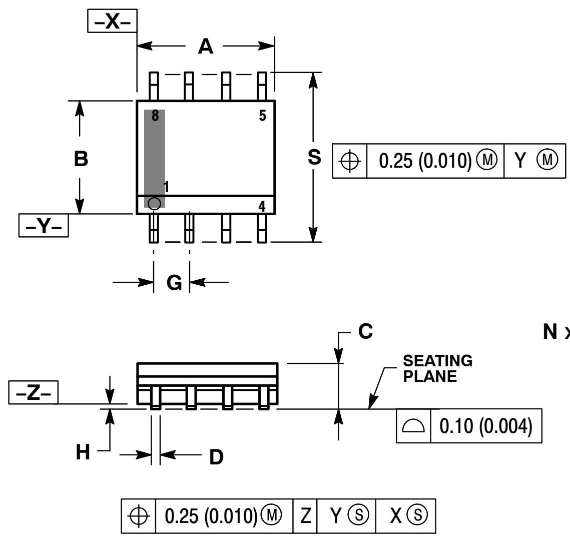
DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

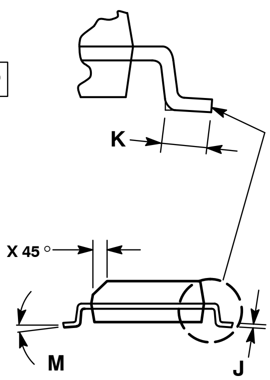


SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

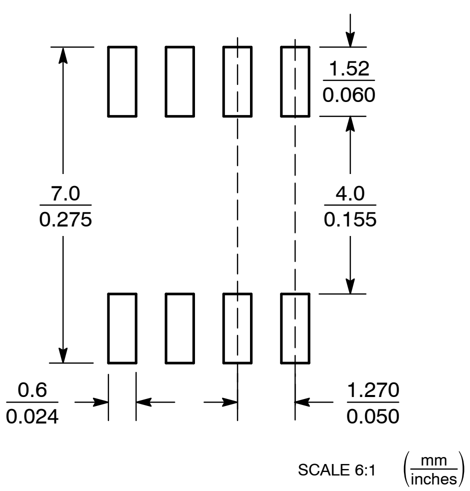




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

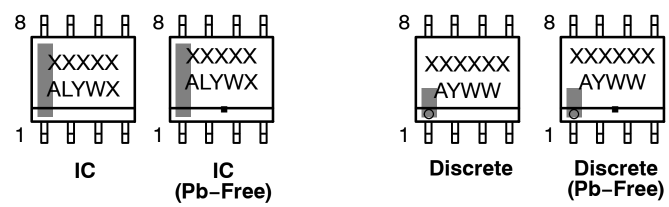
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

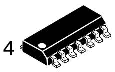
STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

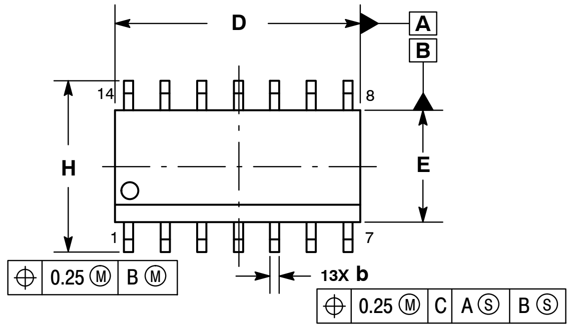
DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 2 OF 2

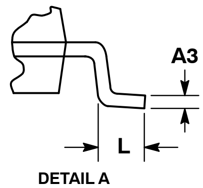


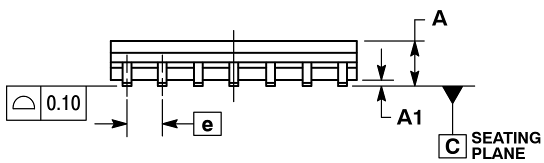
SCALE 1:1

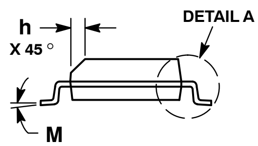
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016





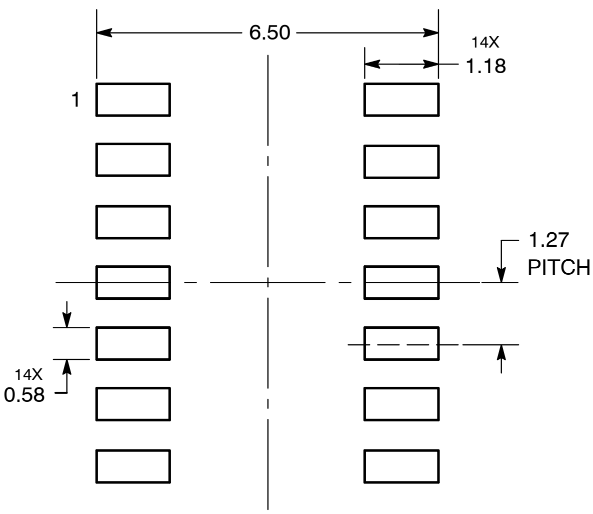




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

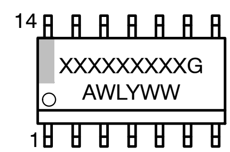
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−14 NB	PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

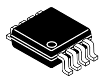
STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

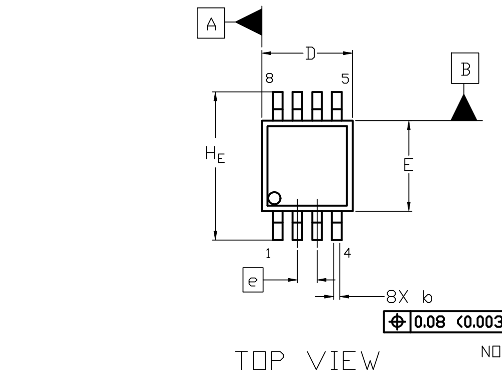
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

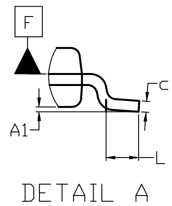


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

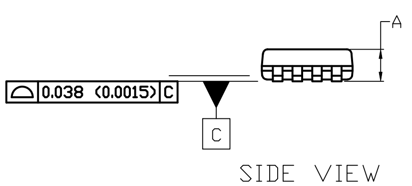
DATE 16 JUL 2020

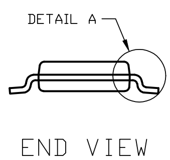


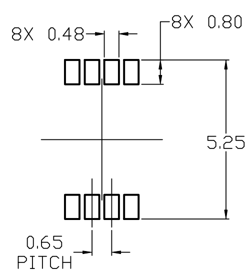


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.





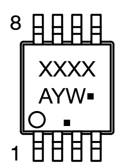


RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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