Inductive Position Sensor with Battery Backup

Resolution: Single−Turn 20−bit / Multi−Turn 24−bit

NCS32100

The NCS32100 is a full featured controller and sensor interface for high resolution, high accuracy angular sensing solutions when paired with a contactless PCB sensor. This device supports static to high−speed applications. The NCS32100 has flexible configuration capabilities allowing for connection to a variety of inductive sensor patterns and offers absolute serial digital output. Inductive sensing techniques have unique advantages over traditional position sensor solutions including but not limited to contaminant insensitivity, mechanical simplification, as well as providing an overall lower cost sensor solution.

Features

- Provides Absolute Position Output with Programmable Index
- Provides Temperature and Backup Battery Measurements
- Supports Connection to an RS−485 Driver (2.5 Mbps)
- Maximum Speed at Full Accuracy: 6000 rpm
- Maximum Speed at Reduced Accuracy: 60,000 rpm
- Supply Voltage Range: 2.75 V – 5.5 V
- Interface level shifting from 2.7 V to 5.5 V
- Low Power Battery Mode Consumption: 2 mA (Typical)*
- Full Operation Current Consumption 80 mA (Typical)
- Internal Programmable M0−ARM MCU Provides Data Interface, Configuration, NVM, and Calibration Features
- This Device is Pb−Free and is RoHS Compliant

Typical Applications

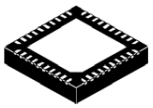
- Industrial Automation / Robotics
- Motor Control / Positioning
- Servo Applications

*Battery mode consumption is based on wakeup duty cycle timing defined by firmware

SENSOR DEPENDENT METRICS (Note 1)

Accuracy	PCB Sensor
±50 arcsec or better	OD: 37.5 mm ID: 8 mm

1. Overall accuracy can be increased by using larger diameter sensors; the NCS32100 supports up to 18 bits of accuracy.

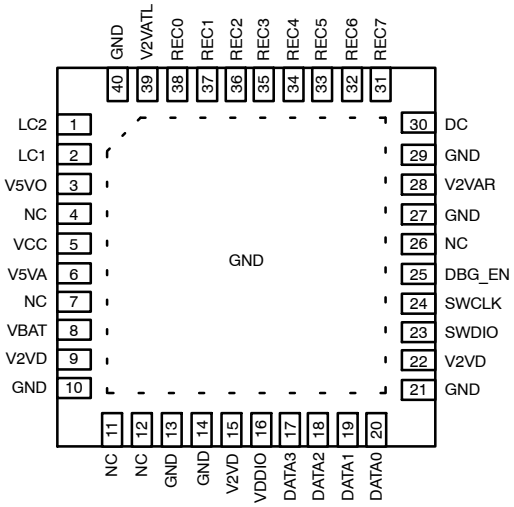


QFN40 5x5, 0.4P
CASE 485FW

MARKING DIAGRAM

22791132100	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
YY	= Year
WW	= Work Week

PIN CONFIGURATION

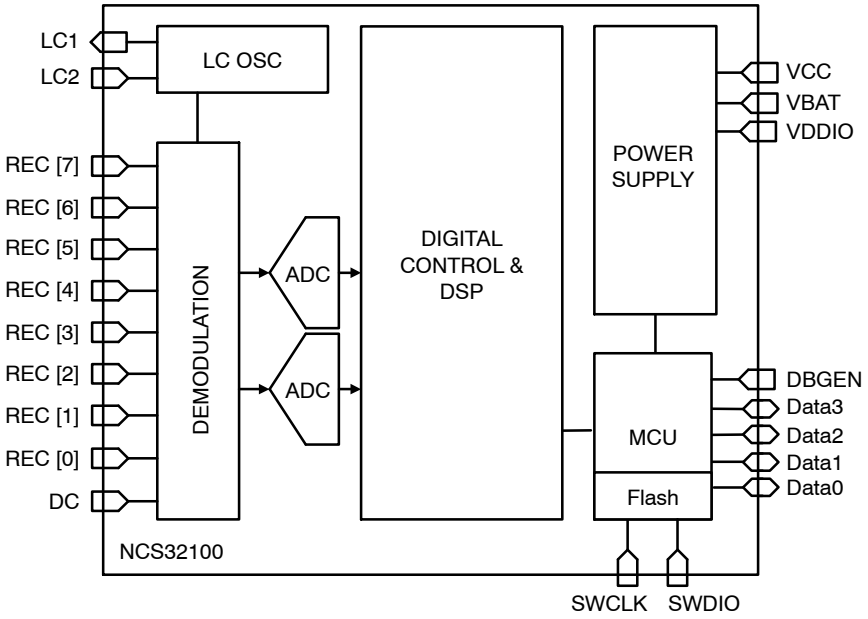


QFN40 5x5 mm (Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS32100XMNTXG	QFN40 (Pb−Free)	5000 / Tape & Reel
NCS32104XMNTBG		1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



NOTE: Internal power distribution lines from Power Supply block and bypass pin are not shown.

Figure 1. Block Diagram

Operating Description

The block diagram shown in figure 1 describes the basic contents of the NCS32100. The NCS32100 is a multichip module contained in a single 5 mm x 5 mm package. The NCS32100 contains an internal oscillator for driving the primary sensor excitation coil, as well as demodulation circuitry for receiving the inductively coupled sensor signals on the REC[n] pins. The applications section of this data sheet further defines connection to these pins. Two 12−bit ADCs digitize the demodulated signals. These digitized values are then passed to the DSP block for processing. Position information are then passed from the digital block to the internal MCU. Digital position data is then sent out on the Data[3:0] pins made available for external drive circuitry, such as an RS−485 driver. The protocol and timing of the commands and data on the data pins are defined by the internal MCU firmware. The MCU also handles calibration routines for maximizing accuracy when the NCS32100 is paired with a sensor. The NCS32100 houses power supply circuitry supporting a wide VCC range and battery backup capability. The internal MCU's non−volatile memory is included for the storage of calibration parameters and sensor front end configuration.

Table 1. NCS32100 PIN DESCRIPTION

Pin	Pin Name	Digital / Analog: I/O	Recommended Connection	Description
1, 2	LC2, LC1	Analog I/O	Connect to excitation coil and matching capacitors	Oscillator coil drive outputs
3	V5VO	Supply Output	Connect to V5VA	LC Oscillator Power
4, 7, 11, 12, 26	NC	NC	Connect to ground	NC
5	VCC	Supply Input	Connect to 5 V Supply and bypass capacitor (10 μF)	Primary 5 V Supply
6	V5VA	Supply Output	Connect to bypass capacitor (10 μF)	3 V/5 V Supply for internal LC oscillator (Connect to external local bypass capacitor).
8	VBAT	Supply Input	Connect to 3 V backup battery and bypass capacitor (100 μF)	Optional: Backup 3 V battery supply pin (Connect to external battery if using battery backup). Connect to ground through 20 kΩ if not using battery backup.
9, 22, 15	V2VD	Supply Output	Connect to bypass capacitor (1 μF)	Digital supply observation pin (Connected to local bypass capacitance for better noise performance)
10, 13, 14, 21, 27, 29, 40, 41	GND	Ground Returns	Connect to ground	0 V Return, connect to module ground
16	VDDIO	Supply Input	3 V to 5 V. Connect to External Driver Supply (RS−485 driver)	I/O power supply for Data[3:0] pins
17	Data3	Digital I/O	Connect to data input or output depending on configuration	RX → Data from External Master to NCS32100
18	Data2	Digital I/O	Connect to data input or output depending on configuration	TX → Data from NCS32100 to External Master
19	Data1	Digital I/O	Connect to data input or output depending on configuration	Available GPIO
20	Data0	Digital I/O	Connect to data input or output depending on configuration	TX_EN → Enable signal for RS485 External Transceiver
23	SWDIO	Digital Input	Connect to ground when not programming internal MCU	Serial Wire Data (MCU firmware data pin)
24	SWCLK	Digital Input	Connect to ground when not programming internal MCU	Serial Wire Clock (MCU firmware clock pin)
25	DBG_EN	Digital Input	Connect to ground when not programming internal MCU	MCU debug Enable pin (Assert high to program / debug internal MCU. Assert low when not in use.)
28	V2VAR	Supply Output	Connect to V2VATL (1 μF)	Analog Power (internally regulated)
30	DC	Analog Input	Connect DC to ground through a 0.1 μF capacitor.	Receiver Coil DC Bias
31, 32, 33, 34, 35, 36, 37, 38	REC[7:0]	Analog I/O	Connect to Fine and Coarse Receiver Coils, Configuration for Coarse versus Fine can be set via internal registers	Receiver Coils [7:0]
39	V2VATL	Supply Input	Connect to bypass capacitor (0.1 μF)	Supplied by connection to V2VAR externally

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
VBAT Voltage Range	V_{BAT}	−0.3 to 6	
Thermal Resistance, Junction−to−Ambient, Steady State (Note 2)	$R_{\theta JA}$	32	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	0.98	°C/W
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 Sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Mode (Note 3)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Mode (Note 3)	ESD_{CDM}	0.5	kV
Latch−up Current Immunity (Note 3)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JS−001−2017
   ESD Charged Device Model per JS−002−2018
   Latch−up Current tested per JESD78

Table 3. OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Excitation Frequency Range	F_{OSC}	3	4	6	MHz
VCC	V_{CC}	2.75	5.0	5.5	V
V_{BAT}	V_{IN}	2.75	3.3	4.2	V
VCC − V_{BAT} (Note 4)	V_{NOM}	0.3	0.7	5.5	V
GND Pins	V_{SS}	−	0	−	V
REC Pins Input Voltage Amplitude (Peak to Peak)	V_{REC}	0.015	−	0.120	Vpp
Ambient Temperature (Note 5)	T_A	−40	−	85	°C
Junction Temperature	T_J	−40	−	105	°C
Multi−turn Count Range	MT	−	−	24	bits
Position Resolution	ST	−	−	20	bits
Velocity Resolution	Vel	−	−	20	bits

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. VCC−V_{BAT} is the voltage difference between VCC and V_{BAT} required to stay in normal mode. Dropping below this voltage will enter the part into battery mode.
5. Minimum ambient temperature is qualified to −40°C. The maximum ambient temperature is dependent on the self−heating of the device, which is dominated by the excitation coil drive. Larger airgaps between rotor and stator induce larger excitation coil current drive and higher self−heating. The NCS32100 is qualified up to 85°C ambient operational temperature.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply Battery Mode Current (Note 6)	V_{CC} = 0 V, V_{BAT} = 3.3 V	I_{STBY}	0.2	2	5	mA
VBAT DC reverse current (Note 7)	V_{CC} = 5 V, V_{BAT} = 3.3 V, T = 85°C	I_{VBAT}	−	1	−	μA
Supply Dynamic Current	V_{CC} = 5.0 V	I_{DYN}	82	90	133	mA
Data[3:0] Pin Drive Strength	V_{CC} = 5.0 V		−	2	−	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Max battery current draw during battery mode assumes a 10 ms wakeup cycle. Min battery current draw during battery mode assumes no periodic wakeup cycles. The wakeup period controls how often the NCS32100 takes a measurement from the sensor coils to track turns count. Battery current during battery mode can be reduced by slowing down the wakeup period, but that will also reduce the rotor speed at which turn counts can be tracked. See the NCS32100 Reference Design Manual for more information on battery mode.
7. Typical reverse current on VBAT is on the order of nano amps. Under certain conditions transient reverse current may occur on VBAT, but will not exceed 100 nano coulumbs.

NCS32100 TIMING SPECIFICATIONS

The NCS32100 defaults to output ‘Position 1’, as described in figure 2. The actual position of the sensor shaft at the time the position is reported to the external RS485 driver will be different than what is reported if the shaft speed is not zero due to latency in the system. The time elapsed from initial angle sample on the REC pins of the NCS32100 to the falling edge of the start bit in the RS485 transmission of the digitized position data can be quantified as the signal processing delay plus the time it takes the MCU to acquire the digitized data and format it to the output protocol ($T_{SPD} + T_E$). The MCU acts as the internal master, and its communications with the signal processing block are synchronous with the timing of the signal processing. T_E defines the time required for communication between the signal processing and the MCU. The DSP offers a delay compensation feature, where the signal processing delay is compensated for and ‘Position 2’ position is reported. ‘Position 2’ is an extrapolation based on previous positions and the current velocity of the sensor. ‘Position3’ could be reported as the output if desired by configuring the extrapolation filter out even further. ‘Position 1’ will be reported by default, where the extrapolation is bypassed. Delay compensation can be configured with the proper internal register setting (detailed in the NCS32100 configuration section). Timing determination should always be referenced from the falling edge of the NCS32100 response start bit and not the master command, as the masters command is asynchronous with the internal signal processing, and the duration of the command is user defined through the MCU firmware. If the rotor is stationary, then position 1, position 2, and position 3 would all be the same value.

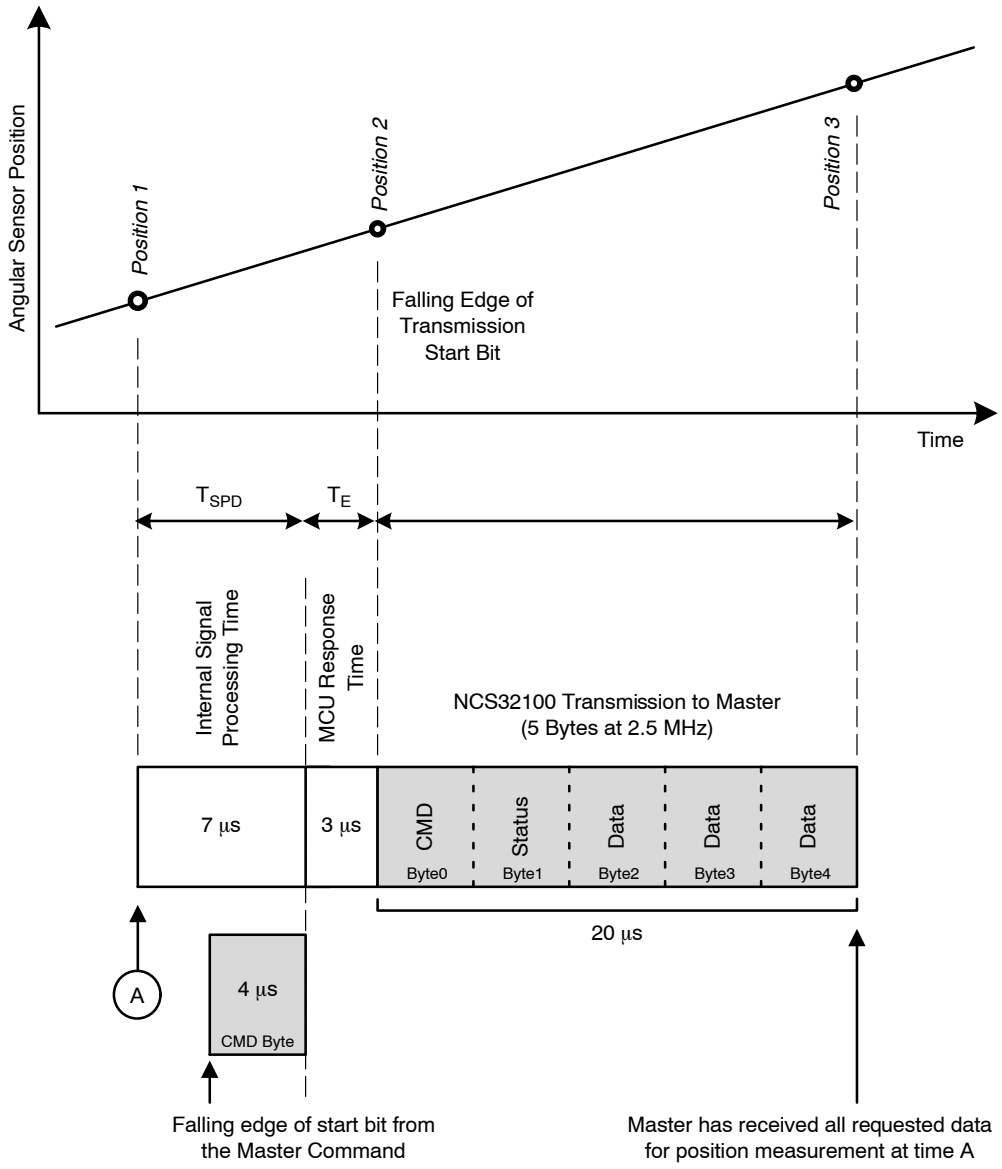


Figure 2. NCS32100 Interface Timing Diagram

Table 5. NCS32100 TIMING SPECIFICATIONS (T_J = 25°C, V_{CC} = 3 V – 5.5 V, unless otherwise specified)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Position Sample Throughput (Available to Internal MCU) (Note 8)	V_{CC} = 5.0 V	T_{TP}	500 ns	1	2	μs
Position Sample Latency (Un−compensated)	V_{CC} = 5.0 V	T_{SPD}	–	7	–	μs
MCU Latency (Note 9)	V_{CC} = 5.0 V	T_E	–	3	–	μs
Max Velocity (Note 10)	V_{CC} = 5.0 V	V_{MAX}	–	6000	45000	Rev/min
Max MCU to SFE Timing Jitter (Note 8)		Tjitter	0	0.25	0.5	μs
UART Transmission Rate			–	–	2.5	MHz
Power Up Ready Time			–	–	50	ms
Self Calibration Run Time (Note 11)			–	2	–	s
External Calibration Run Time	1 full revolution at 100 rpm max		2	–	–	s

8. Updated position data is available for acquisition by the internal MCU every T_{TP}. 500 ns can be achieved by enabling internal oversampling filter. If the digital filter is bypassed, then the updated position is available to the MCU every 2 μs.
9. T_E assumes direct MCU pass through. Any additional processing in the MCU will add latency.
10. Accuracy may exceed 50 arcsec beyond 6000 rpm due to the system sampling jitter of 500 ns. 45,000 RPM max rotor speed assumes fine sensor on stator has 64 periods. Faster speeds can be achieved with lower supported period options. See application section for details.
11. The calibration routine can be run on an external processor at much higher speeds (~2 seconds with high performance MCU), or it can be run directly by the NCS32100 (as implemented in the internal MCU firmware).

NCS32100 EXTERNAL COMPONENT SPECIFICATIONS

The NCS32100 requires a minimal number of external components to function as a system. This is comprised of bypass capacitors for the supply pins, tuning capacitors for the LC Oscillator pins, and the external sensor coils connected to the LC Oscillator pins and the Receiver pins. The excitation coil (connected from the LC1 pin to the LC2 pin) is used to provide the excitation field, which creates eddy currents in the rotor coils. The eddy currents in the rotor inductively couple to the receiver coils to induce voltages that are proportional to the position of the rotor (which is in close proximity). The receiver signals are connected to pins REC[7:0]. The orientation of the receiver coils and the excitation coil is discussed in more detail in the applications section. The diagram below shows the external components with their value definition found in Table 6. The excitation frequency is determined by the equation:

$$f_{PRIM} \approx \frac{1}{2\pi\sqrt{L \times C}} \text{ Where } C = \frac{C1 \times C2}{C1 + C2} \quad \text{(eq. 1)}$$

Where C is the equivalent capacitance of the two external capacitors as if they are connected in series. The excitation coil should be designed with the right value of capacitors to target 4.4 MHz for the excitation frequency.

The NCS32100 uses a divided, ratiometric value of the LC oscillator signal amplitude to subtract out the parasitic coupling from the LC coil to the stator receive coils. A capacitive divider is connected between LC1 and GND (C_{DIV1} and C_{DIV2}), and the divided value is supplied to REC[3:4] pins. The amplitude of the divided signal should be within 1/3 to 2/3 of the received signals. C_{DIV1} can be adjusted to provide the correct amplitude. ADC values of the REC[7:0] signals can be obtained from the MCU, and analyzed for assistance in tuning C_{DIV1}.

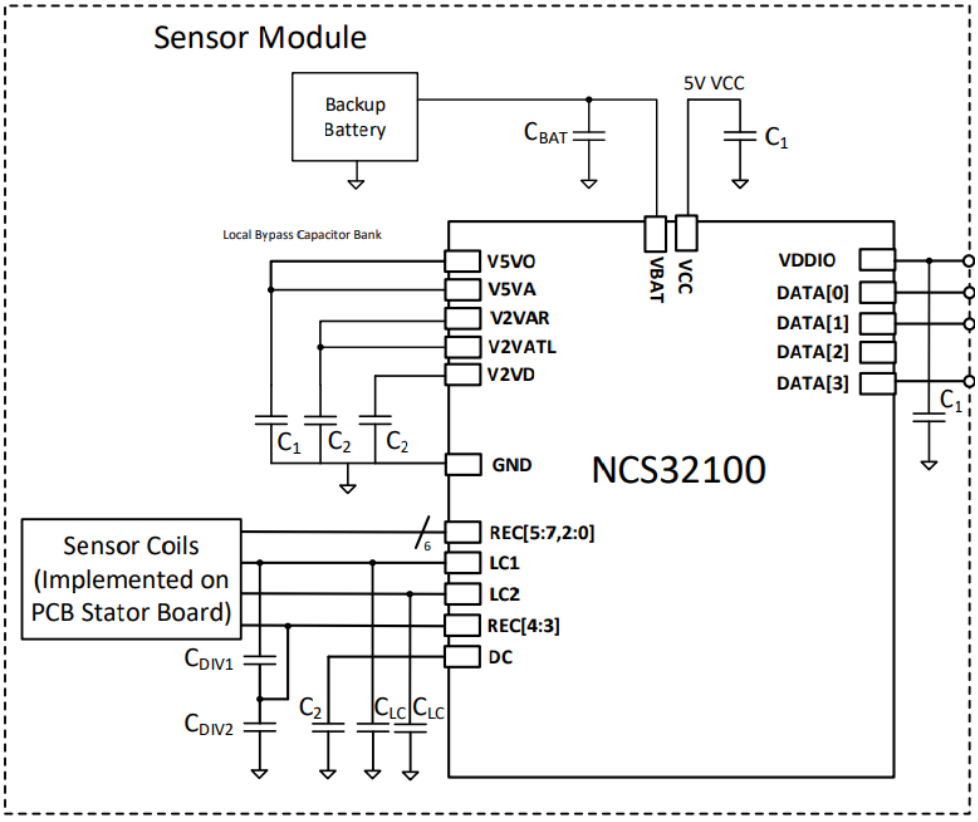


Figure 3. External Component Placement Diagram

Table 6. EXTERNAL COMPONENT DEFINITION (T_J = 25°C, VCC = 3 V – 5.5 V, unless otherwise specified)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Receiver Coil Series Resistance		ESR_{COIL}	–	4	–	Ω
LC Oscillator Coil Inductance		$L_{LC\_OCS\_COIL}$	0.5	1	4	μH
LC Oscillator Coil Series Resistance		$ESR_{LC\_OSC\_COIL}$	–	0.5	1.0	Ω
LC Oscillator Load Capacitance		C_{LC}	0.35	3.2	11.3	nF
LC Oscillator Capacitive Divider Top		C_{DIV1}	–	22	–	pF
LC Oscillator Capacitive Divider Bottom		C_{DIV2}	–	1	–	nF
Power Supply Decoupling Capacitors	Used for V2VATL, V2VAR, and V2VD	C_2	0.8	1.0	1.2	μF
Power Supply Decoupling Capacitors	Used for VCC, V5VA, and V5VO	C_1	8	10	12	μF
VBAT Decoupling Capacitors	VBAT supply decoupling capacitor	C_{BAT}	100	–	260	μF

NOTE: Refer to reference design manual for sensor design details. Table 6 is intended as preliminary guidance only.

CONFIGURATION

The analog front end internal to the NCS32100 communicates with the embedded MCU via a 16−bit 40 MHz parallel bus. The NCS32100 firmware includes subroutine functions that enable communication with the front end on this parallel bus. Data can be acquired such as position. The firmware allows access to the internal configuration registers that control the functionality of the part. These configuration registers are loaded from the MCU non−volatile memory as part of the start−up routine. Configuration can be changed after initial startup. The reference firmware allows for reading and writing these configuration registers, and any changes will be saved to the MCU non−volatile memory. Once the part is configured and data is received across the internal parallel bus, the embedded MCU can format the data and transmit it to an external master per request according to the protocol definition implemented in the firmware. Please refer to the NCS32100 reference design manual for a detailed description of the firmware functionality and the interface implementation. The NCS32100 is loaded with the reference design firmware by default, which properly handles the configuration during start−up.

NCS32100 Configuration Table

The table below details the configuration registers accessed by the embedded MCU. The purpose of each register is defined in Appendix A. These registers are all properly handled in the reference design firmware. Modification can be made by the user as needed. The NCS32100 is highly configurable. Application notes are provided upon request detailing advanced configuration options.

Table 7. NCS32100 SHADOW REGISTERS TO BE LOADED BY THE EMBEDDED MCU

Address	Access Type	Description	Default Value
0x00	R	LC Oscillator Gain DAC (Status only)	0x0000 (Note 12)
0x01	R	PGA Gain DAC (Status only)	0x0000 (Note 12)
0x03	R	Digital Control (Status only)	0x0000
0x04	R	Status	0x0000 (Note 12)
0x10	R/W	Selection Matrix for Coarse Block	0xF249
0x11	R/W	Selection Matrix for Fine Block	0x0B6D
The next 16 registers (0x12 through 0x21) hold the calibration coefficients used to calibrate out any asymmetries in the PCB sensor and the analog front−end. See the calibration section for more details.			
0x12	R/W	Clarke Transform Imaginary Coefficient 0 for Coarse Block	0x0000 (Note 12)
0x13	R/W	Clarke Transform Imaginary Coefficient 1 for Coarse Block	0x0000 (Note 12)
0x14	R/W	Clarke Transform Imaginary Coefficient 2 for Coarse Block	0x0000 (Note 12)
0x15	R/W	Clarke Transform Imaginary Coefficient 3 for Coarse Block	0x0000 (Note 12)
0x16	R/W	Clarke Transform Real Coefficient 0 for Coarse Block	0x0000 (Note 12)
0x17	R/W	Clarke Transform Real Coefficient 1 for Coarse Block	0x0000 (Note 12)
0x18	R/W	Clarke Transform Real Coefficient 2 for Coarse Block	0x0000 (Note 12)
0x19	R/W	Clarke Transform Real Coefficient 3 for Coarse Block	0x0000 (Note 12)
0x1A	R/W	Clarke Transform Imaginary Coefficient 0 for Fine Block	0x0000 (Note 12)
0x1B	R/W	Clarke Transform Imaginary Coefficient 1 for Fine Block	0x0000 (Note 12)
0x1C	R/W	Clarke Transform Imaginary Coefficient 2 for Fine Block	0x0000 (Note 12)
0x1D	R/W	Clarke Transform Imaginary Coefficient 3 for Fine Block	0x0000 (Note 12)
0x1E	R/W	Clarke Transform Real Coefficient 0 for Fine Block	0x0000 (Note 12)
0x1F	R/W	Clarke Transform Real Coefficient 1 for Fine Block	0x0000 (Note 12)
0x20	R/W	Clarke Transform Real Coefficient 2 for Fine Block	0x0000 (Note 12)
0x21	R/W	Clarke Transform Real Coefficient 3 for Fine Block	0x0000 (Note 12)
0x22	R/W	Velocity Coefficient MSB for Absolute Algorithm Extrapolation	0x0000
0x23	R/W	Velocity Coefficient LSB for Absolute Algorithm Extrapolation	0x7E75
0x26	R/W	Velocity Coefficient MSB for Digital Filter Extrapolation	0x0084
0x27	R/W	Velocity Coefficient LSB for Digital Filter Extrapolation	0x0561

Table 7. NCS32100 SHADOW REGISTERS TO BE LOADED BY THE EMBEDDED MCU (continued)

Address	Access Type	Description	Default Value
0x2A	R/W	Low Pass Filter for Digital Filter	0x003F
0x2B	R/W	Digital Control	0x0020
0x2F	R/W	Channel Select	0x0000
0x40	R/W	LC Oscillator Gain DAC Control	0x0000
0x41	R/W	LC Oscillator Gain Time Control	0x01F4
0x42	R/W	PGA Coarse Gain DAC Control	0x0000
0x43	R/W	PGA Fine Gain DAC Control	0x0000
0x44	R/W	PGA Gain Time Control	0x01F4
0x45	R/W	PGA Coarse Offset DAC Control	0x0000
0x46	R/W	PGA Fine Offset DAC Control	0x0000
0x47	R/W	PGA Offset Time Control	0x01F4
0x48	R/W	Angle Extrapolator Time Control	0x0000
0x4C	R/W	Normal Wakeup Delay	0x1000
0x4D	R/W	Startup Delay Time MSB	0x0006
0x4E	R/W	Startup Delay Time LSB	0x1A80
0x4F	R/W	DSP Wakeup Delay	0x1000
0x50	R/W	Autozero Angle MSB	0x0000
0x51	R/W	Autozero Angle LSB	0x0000
0x57	R/W	Input/Output Control	0x0008
0x5F	R/W	Sensor Selection	0x0013
0x80	R/W	Secondary Calibration Bin 0	0x0000
0x81	R/W	Secondary Calibration Bin 1	0x0000
0x82	R/W	Secondary Calibration Bin 2	0x0000
0x83	R/W	Secondary Calibration Bin 3	0x0000
0x84	R/W	Secondary Calibration Bin 4	0x0000
0x85	R/W	Secondary Calibration Bin 5	0x0000
0x86	R/W	Secondary Calibration Bin 6	0x0000
0x87	R/W	Secondary Calibration Bin 7	0x0000
0x88	R/W	Secondary Calibration Bin 8	0x0000
0x89	R/W	Secondary Calibration Bin 9	0x0000
0x8A	R/W	Secondary Calibration Bin 10	0x0000
0x8B	R/W	Secondary Calibration Bin 11	0x0000
0x8C	R/W	Secondary Calibration Bin 12	0x0000
0x8D	R/W	Secondary Calibration Bin 13	0x0000
0x8E	R/W	Secondary Calibration Bin 14	0x0000
0x8F	R/W	Secondary Calibration Bin 15	0x0000
0x90	R/W	Battery Mode Wakeup Period Setting	0X0100

12. NCS32100 will determine values based on sensor characteristics.

Internal Data Format (As Received across the 16−bit Interface)

The position and turns count as received from the data acquisition functions are shown in the table below.

Table 8. NCS32100 DATA FORMAT DESCRIPTION

Data	Bits	Sign	Scale	Description
Angle	20	Unsigned	2^{20}	Angle is an unsigned 20 bits measurement of the absolute angle in 1 revolution. In other words, the angle is represented as 1 to 1,048,576 in one revolution.
Turn	24	Signed	1	Turn is a signed 24 bits measurement of the complete revolutions. Turn is increment by +1 for every clockwise rotation and by −1 for every counterclockwise rotation.

Below are examples that show how these formats can be converted to radians and degrees.

Angle Conversion

Example: Received Angle hex value of 0x62626 (Decimal value is 402,982)

Table 9. POSITION CONVERSION EXAMPLE

To Convert to Radians	
Received Position from NCS32100: 402,982	
1. Divide received value by scale (2^20).	402,982/1,048,576 = 0.384314 rotations
2. Multiply by 2π to get radians	0.384314 * 2π = *2.41471 radians*
Convert to Degrees	
1. Divide received value by scale (2^20).	402,982/1,048,576 = 0.384314 rotations
2. Multiply by 360 to get degrees	0.384314 * 360 = *138.353 Degrees*

OTHER NCS32100 FEATURES

Open Coil Detect

The NCS32100 device has an open coil detect feature that can be used to detect if any sensor coils are not connected to the RECx pins (open circuit). If there is a break in one of the sensor coils, or if it is not connected, then running this test will result in a 0b'1 in the status register (register 0x04 bit 13). The Open Coil Detect test is run by writing the USER_OPENCOILDET_RUN bit to a 1 in Digital Control register (0x03 bit 13). This will start an Open Coil Detect test immediately. The USER_OPENCOILDET_RUN bit will stay high until the test has finished. The OPENCOILDET_AT_POR_DIS bit in Digital Control register controls whether the Open Coil Detect test is run during startup. A value of 0b'1 in the bit will cause the test to not be run during startup. A value of 0b'0 will cause the test to be run at startup.

Extrapolation Tuning

The NCS32100 device provides an extrapolation feature that can be used to cancel the effect of data reporting latency. When a request for the position is made, the data response comes with some latency. If the sensor is moving, then the position at the time the data is received will be different than it was at the time the request was made. Extrapolation can be used to predict where the sensor will be post latency so that the data readout will be the position at the time the data is received. The extrapolated angle relies on the current position and the current velocity. The extrapolation uses low pass filters on the velocity to make the future position prediction. The extrapolation calculation takes the form of:

$$\theta_{EXT} = \theta_{LPF} + K_v v_{LPF} + K_a a_{LPF} \quad \text{(eq. 2)}$$

Where is the angular velocity coefficient. is a programmable coefficient. The optimal value needs to be calibrated by the user.

The objective of setting the Kv constant is to effectively time shift angular measurements forward in time. From the perspective of the system, this time shift can cancel system delay to effectively create a zero delay system. From the perspective of the encoder, this is done by extrapolating the angular position forward in time using measured speed. However, no two systems are identical. Therefore, the Kv constant need to be determined for the given system using lab measurements. K_A is the angular acceleration coefficient. It is also programmable and should be set in the same fashion as the K_V coefficient. Please refer to the NCS32100 advanced configuration application note for details on calibrating these coefficients. The extrapolation feature can be disabled by setting the USER_ABSALGO_EXTRP_DIS bit in the Digital Control register (0x03 bit 15). The extrapolation is bypassed by default in the NCS32100 firmware, and needs to be configured by the user if the extrapolation feature is needed.

Sensor Calibration

Each PCB sensor design will include some systematic asymmetries that need to be calibrated for in both Fine and Coarse sensors. Calibration needs to take place to compensate for PCB mismatch, rotor air gap, tilt and eccentricity. The NCS32100 default firmware contains a self−calibration routine that allows for calibration independent of a reference. Calibration can be initiated from a master by command. The NCS32100 can also deliver raw samples that allow for external calibration with a reference encoder. For more information on the sensor calibration method, please refer to the NCS32100 Reference Design Manual.

For external calibration options, please request further documentation. Testing shows that re−calibration is not necessary to maintain 50 arcsec accuracy or less if the eccentricity and air gap do not vary by more than ±250 μm from center. The rotor must be centered to within 50 μm to the shaft to allow for proper calibration. The reference design firmware includes the calibration routine and a method for secondary calibration allowing for the cancellation of 360 degree rotation single period fundamental or low spatial frequency error.

Battery Backup

The NCS32100 supports a battery backup mode where VBAT can be tied to a 3.3V nominal external battery. The current draw from the battery during normal operation is <1 μA. When the VCC voltage drops below the VBAT voltage, the NCS32100 will switch over to draw current from the battery. During this time, the firmware running on the internal MCU puts the sensor front end to sleep to conserve power. The firmware periodically wakes up the sensor front end to take a position reading and to update the multi−turn count. The amount of current that is drawn from the battery depends on the wakeup period. The NCS32100 will be able to track turns count at higher speeds with shorter wakeup periods, but it will also consume more amortized current from the battery in battery mode. The NCS32100 Reference Design firmware allows the user to select the wakeup period to control the current draw and the turns count proficiency.

APPLICATIONS INFORMATION

MCU Capabilities

The internal MCU allows for the addition of several features defined by the MCU firmware. The embedded MCU firmware is ultimately responsible for defining the output protocol and timing. Once the data is available in the MCU, it can be manipulated by the firmware for output. Possibilities for additional features include (but are not limited to):

Flexible Protocols

The internal MCU firmware can be written to change the protocols used for communication in absolute encoder mode.

Error Reporting

Error reporting can be implemented by writing the MCU firmware to recognize and handle specific errors. The MCU has access to registers in the digital control block, including the calibration coefficients and the gain settings for the coil drivers. The MCU can be programmed to monitor gain settings to detect if the sensor signal strength is too weak, or too strong, indicative of a sensor coil failure. The MCU could be programmed to report errors for unexpected position readings based on the current speed.

Battery Voltage Monitoring

The MCU is equipped with an internal ADC. One of the ADC input channels is internally connected to a divided down (by 3) version of the VBAT voltage. This allows the MCU to digitize and monitor the battery voltage if a battery is connected. The user can program the MCU to report the battery voltage, and report errors if a battery voltage falls below acceptable levels.

Temperature Monitoring

The internal MCU can report its own die temperature. The MCU can be programmed to report the internal temperature if desired.

MCU Programming

The NCS32100 comes with default firmware providing the functionality and performance outlined in the NCS32100 Reference Design Users Guide. An NCS32100 SDK Starter Guide is also available which describes how to setup a project in an Eclipse based IDE for programming and debugging firmware. MCU registers and hardware available to the user are all documented in the NCS32100 Reference Design Manual. The SDWIO and SKCLK, and DEBUG_EN pins are used exclusively for the programming of the embedded NCS32100 MCU using an SWD J−Link programmer.

Sensor Speed

The NCS32100 internally calculates the rotor velocity every 2 μs. The device can be configured with a velocity low pass filter to help reject noise and velocity jitter. Available filter coefficients are detailed in the configuration register section of this datasheet. The maximum sensor speed at which full accuracy is maintained is specified as 6000 rpm. Higher speeds are possible at reduced accuracy, up to 45000 rpm. These speed limitations are based on the electrical speed defined by the number of periods in the coarse and fine coils. The table below shows the mechanical speeds achievable for different fine coil period settings. The coil period configuration takes place in register 0x5F.

Table 10.

Fine Coil Period Setting	Maximum Achievable Mechanical Speed (RPM)
8	360,000
16	180,000
32	90,000
64	45,000
128	22,500
256	10,000

If higher mechanical speed capability is needed, then the PCB sensor can be designed with fewer fine coil periods. Position accuracy and PCB size also are affected by the fine coils period selection.

Output Modes

The NCS32100 has four data pins for supporting any interface that can be programmed in firmware. The Data[3:0] pins support any signal between 2.7 V to 5.5 V using internal level shifters where the output voltage levels are powered by the VDDIO. The NCS32100 reference firmware is programmed to support a 2.5 MHz UART over RS485 interface. The Data[3:0] also supports SPI, and direct GPIO control. The content and organization of the interface frames are defined by firmware. This flexibility allows for modifications to fit the application of the end user.

TYPICAL APPLICATION

The following application example presents an angular position sensor application. The internal signal processing is highly configurable. Configuration registers are loaded into the digital logic registers by the internal MCU at power−up. The configuration is thus firmware defined. The design of the coils on the PCB can cater to specific resolution, accuracy, and mechanical envelope constraints. A wide range of applications can thus be targeted by the NCS32100 utilizing different numbers of coil sets to fit different sizes of sensor and accuracies. The diagram below shows the connections needed for a rotary sensor application where the NCS32100 provides the sensor excitation and the sensor receive circuitry.

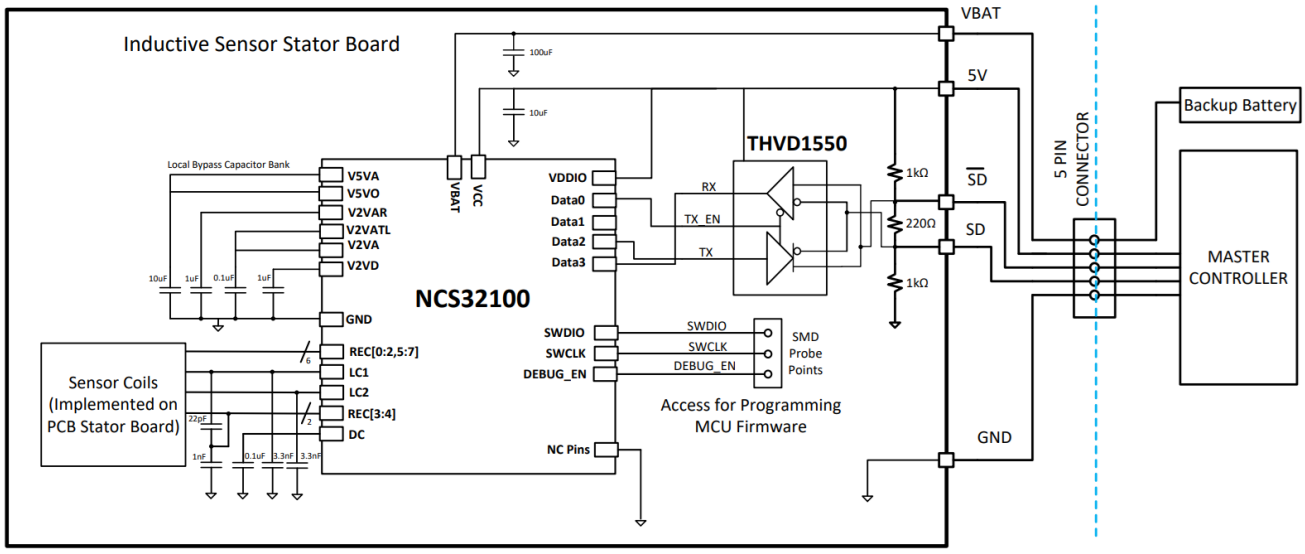


Figure 4. Typical NCS32100 Application

In this application, an RS−485 driver is used to send the UART data from the NCS32100 out to a twisted differential pair. No other circuitry is needed. The entire encoder module electronics can easily fit on the stator PCB for a lean, low−cost, solution.

Typical Sensor Configuration

The figures below show the sensor coil configuration used in the NCS32100 reference design. It is one of many possible sensor designs that will work with the NCS32100 device. This sensor design uses two separate coil sets to achieve high accuracy position readings. Sensor coils are connected to the REC pins on the NCS32100, which supports up to 8 coils.

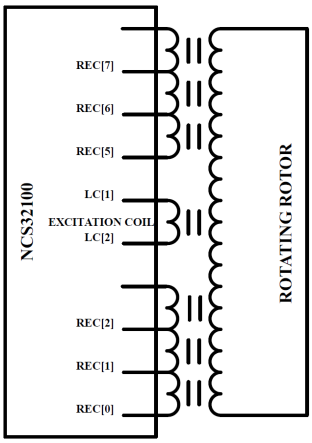


Figure 5. Sensor Electrical Model

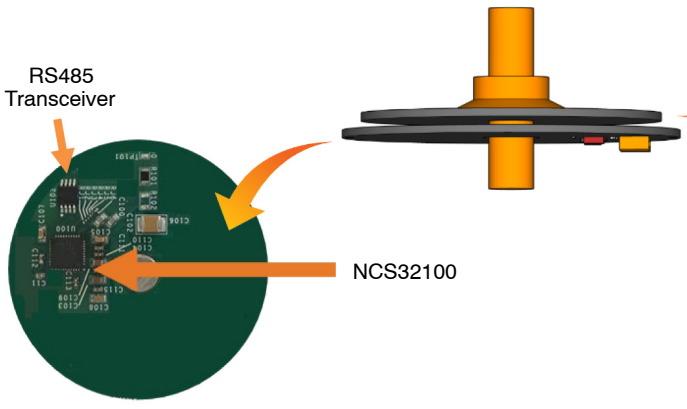


Figure 6. Example of Inductive Encoder 4 Layer PCB Stator with NCS32100 Package and External Components on the Back of the Board (Contains Transmitter Loop and Receiver)

Figure 7. Example of Inductive 1 Layer PCB Rotor (With a 64 Period Fine Loop and a 5 Period Coarse Loop)

PCB Considerations

The layout of the sensor design and its connection to the NCS32100 must be symmetric to avoid unwanted parasitic coupling. Please refer to the NCS32100 Reference design for an example of correct sensor to NCS32100 interface. The back paddle of the NCS32100 can be used to decrease the thermal resistance and lower the self heating of the part. If a heat spreader plane is connected to the back paddle of the NCS32100, it must not be a solid plane, but rather a series of lines that connect to the back paddle and run out perpendicular to the excitation coil.

Typical Sensor Module (Utilizing the NCS32100)

The NCS32100 can be used with a several configurations and sensors. The example below shows a rotational sensor application, where the NCS32100 is mounted on the stator PCB board and interfaces with the stator coils. Keep out regions and size of the stator / rotor board can change based on application needs regarding design, resolution needs, and accuracy needs.

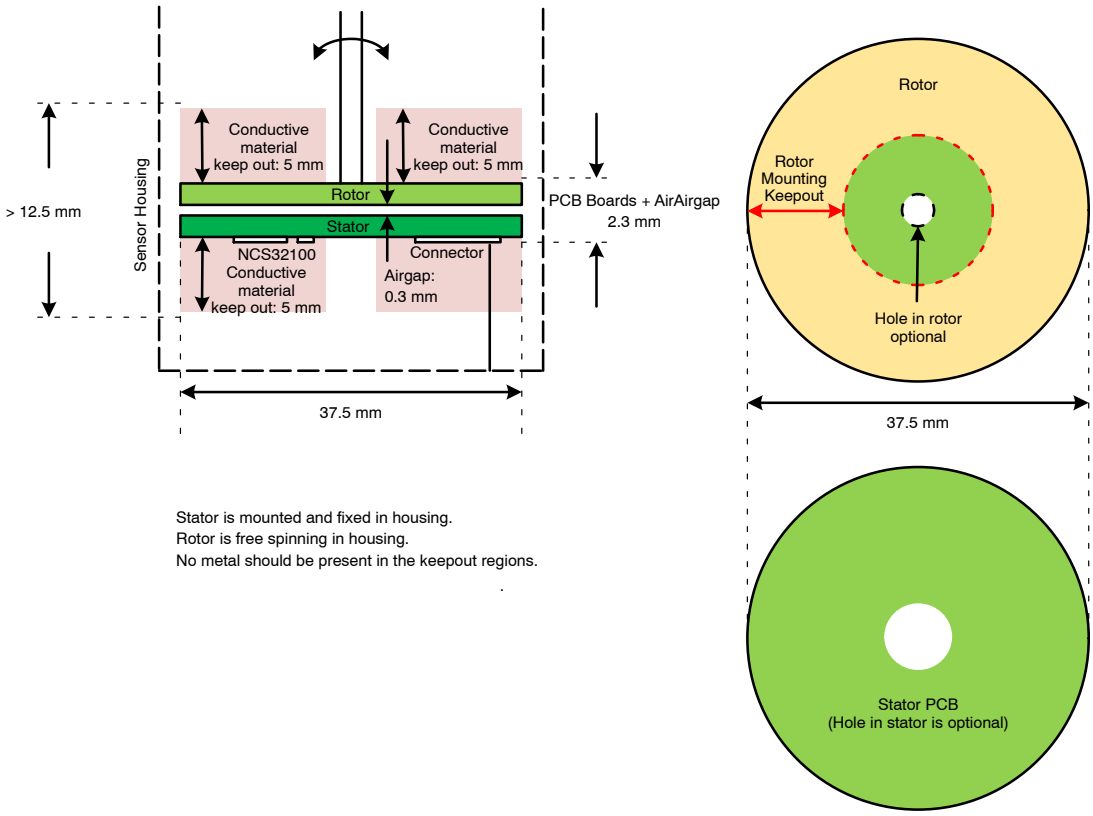


Figure 8. Mechanical Housing Example

Effects of Air Gap and Eccentricity and Tilt

The effects of the airgap and misalignment between the rotor and stator in an inductive angular position sensor are highly dependent on the systems mechanical dimensions. The system above is composed of multiple receiver coils on a stator to interface with the NCS32100, and multiple coils on a rotor. The sensors outer diameter is 37.5 mm with a 0.3 mm air−gap between rotor and stator. In this system, the 50 arcsec specification was maintained with ±0.25 mm variation on eccentricity, and ±0.2 mm variation on the air gap. For sensors with a different diameter and coil configuration, this sensitivity will be different. For assistance with sensor stator and rotor design, application engineering support is available. Please consult your **onsemi** sales contact.

APPENDIX A: INTERNAL CONFIGURATION REGISTER DEFINITIONS

LC OSCILLATOR GAIN DAC

Address 0x00 – Default Value 0x0000

This register shows the excitation coil oscillator gain. It is a read only register. It is periodically updated by the NCS32100 to get the desired receiver coil magnitudes.

Bit	Name	Description
15:8		Reserved.
7:0	USER_LC_GAIN_DAC_FSM[7:0]	LC Oscillator Gain drive strengths. The current LC Oscillator Gain DAC value. *Code Gain Calculation* 0b'00xxxxxx 0.4 + (0.05 * N) mA 0b'01xxxxxx 3.6 + (0.1 * N) mA 0b'10xxxxxx 10 + (0.2 * N) mA 0b'11xxxxxx 22.8 + (0.4 * N) mA where 'N' is the 'xxxxxx' portion of the code

RECEIVER PIN AMPLIFIER GAIN (DAC SETTINGS)

Address 0x01 – Default Value 0x0000

This register shows the programmable amplifier gain setting. It is a read only register. The programmable gain amplifier is used to amplify the receiver coil signals before they are digitized. The programmable gain amplifier settings are periodically updated by the NCS32100 to get the best possible dynamic range on the sensor receiver signals.

Bit	Name	Description
15:14		Reserved.
13:8	USER_PGA_GAIN_DAC_FSM_COARSE[5:0]	Programmable Amplifier Gain settings for Coarse Coils Block. The current PGA Gain DAC value used by the Coarse block. NOTE: The PGA Gain G_{PGA} is related to USER_PGA_GAIN_DAC_COARSE[5:0] by the equation: G_{PGA} = (1.189^USER_PGA_GAIN_DAC_COARSE[5:0]) * 10.
7:6		Reserved.
5:0	USER_PGA_GAIN_DAC_FSM_FINE[5:0]	Programmable Amplifier Gain settings for Fine Coils Block. The current PGA Gain DAC value used by the Fine block. NOTE: The PGA Gain G_{PGA} is related to USER_PGA_GAIN_DAC_FINE[5:0] by the equation: G_{PGA} = (1.189^USER_PGA_GAIN_DAC_FINE[5:0]) * 10.

DIGITAL CONTROL

Address 0x03 – Default 0x0000

The Digital Control Register allows the user to turn the angle extrapolation feature on or off. It also allows the user to run the open coil detect check.

Bit	Name	Description
15	USER_ABSALGO_EXTRP_DIS	User Absolute Algorithm Extrapolation Disable. Disable the angle extrapolation in the absolute algorithm when the LC oscillator gain, PGA gain or PGA offset are updated
14		Reserved.
13	USER_OPENCOILDET_RUN	USER Open Coils Detection Run. Run the open coils detection FSM. The bit is reset to 0 when the FSM is finished.
12		Reserved.
11	USER_TURN_RST	Turn Counter Reset. Reset the Turn counter to 0. The register bit is automatically reset to 0
10:0		Reserved.

STATUS

Address 0x04 – Default 0x0000

The status register holds the results of the open coil detect test.

Bit	Name	Description
15:14		Reserved.
13	USER_OPENCOILDET_FLAG	User Open Coil Detection Flag. A 1 signifies that there is an unconnected coil.
12:0		Reserved.

SELECTION MATRIX FOR COARSE BLOCK

Address 0x10 – Default 0xF249

This register holds the setting for the connection between the REC pins and the sensor coarse loops. For more details, see advanced configuration note.

Bit	Name	Description
15:14	SEL_MATRIX_RECT3P_COARSE[1:0]	Selection Matrix for Rectifier3 Positive Input on Coarse block. See table below for decode.
13:12	SEL_MATRIX_RECT3N_COARSE[1:0]	Selection Matrix for Rectifier3 Negative Input on Coarse block. If SEL_MATRIX_RECT3N_COARSE[1:0] = SEL_MATRIX_RECT3P_COARSE[1:0] then the rectifier3 negative input of the Coarse block is connected to DC. Otherwise see table below for decode.
11:10	SEL_MATRIX_RECT2P_COARSE[1:0]	Selection Matrix for Rectifier2 Positive Input on Coarse Block. See table below for decode.
9:8	SEL_MATRIX_RECT2N_COARSE[1:0]	Selection Matrix for Rectifier2 Negative Input on Coarse Block. If SEL_MATRIX_RECT2N_COARSE[1:0] = SEL_MATRIX_RECT2P_COARSE[1:0] then the rectifier2 negative input of the Coarse block is connected to DC. Otherwise see table below for decode.
7:6	SEL_MATRIX_RECT1P_COARSE[1:0]	Selection Matrix for Rectifier1 Positive Input on Coarse Block. See table below for decode.
5:4	SEL_MATRIX_RECT1N_COARSE[1:0]	Selection Matrix for Rectifier1 Negative Input on Coarse Block. If SEL_MATRIX_RECT1N_COARSE[1:0] = SEL_MATRIX_RECT1P_COARSE[1:0] then the rectifier1 negative input of the Coarse block is connected to DC. Otherwise see table below for decode.
3:2	SEL_MATRIX_RECT0P_COARSE[1:0]	Selection Matrix for Rectifier0 Positive Input on Coarse Block. See table below for decode.
1:0	SEL_MATRIX_RECT0N_COARSE[1:0]	Selection Matrix for Rectifier0 Negative Input on Coarse Block. If SEL_MATRIX_RECT0N_COARSE[1:0] = SEL_MATRIX_RECT0P_COARSE[1:0] then the rectifier0 negative input of the Coarse block is connected to DC. Otherwise see table below for decode.

Table 11. COARSE BLOCK RECTIFIER CONTROL SELECTION

Coarse Register Input	Channel Select	Pin
00	0	REC0
00	1	REC4
01	0	REC1
01	1	REC5
10	0	REC2
10	1	REC6
11	0	REC3
11	1	REC7

SELECTION MATRIX FOR FINE BLOCK

Address 0x11 – Default 0x0B6D

This register holds the setting for the connection between the REC pins and the sensor fine loops. For more details, see advanced configuration note.

Bit	Name	Description
15:14	SEL_MATRIX_RECT3P_FINE[1:0]	Selection Matrix for Rectifier3 Positive Input on Fine Block. See table below for decode.
13:12	SEL_MATRIX_RECT3N_FINE[1:0]	Selection Matrix for Rectifier3 Negative Input on Fine Block. If SEL_MATRIX_RECT3N_FINE[1:0] = SEL_MATRIX_RECT3P_FINE[1:0] then the rectifier3 negative input of the fine block is connected to DC. Otherwise see table below for decode.
11:10	SEL_MATRIX_RECT2P_FINE[1:0]	Selection Matrix for Rectifier2 Positive Input on Fine Block. See table below for decode.
9:8	SEL_MATRIX_RECT2N_FINE[1:0]	Selection Matrix for Rectifier2 Negative Input on Fine Block. If SEL_MATRIX_RECT2N_FINE[1:0] = SEL_MATRIX_RECT2P_FINE[1:0] then the rectifier2 negative input of the fine block is connected to DC. Otherwise see table below for decode.
7:6	SEL_MATRIX_RECT1P_FINE[1:0]	Selection Matrix for Rectifier1 Positive Input on Fine Block. See table below for decode.
5:4	SEL_MATRIX_RECT1N_FINE[1:0]	Selection Matrix for Rectifier1 Negative Input on Fine Block. If SEL_MATRIX_RECT1N_FINE[1:0] = SEL_MATRIX_RECT1P_FINE[1:0] then the rectifier1 negative input of the fine block is connected to DC. Otherwise see table below for decode.
3:2	SEL_MATRIX_RECT0P_FINE[1:0]	Selection Matrix for Rectifier0 Positive Input on Fine Block. See table below for decode.
1:0	SEL_MATRIX_RECT0N_FINE[1:0]	Selection Matrix for Rectifier0 Negative Input on Fine Block. If SEL_MATRIX_RECT0N_FINE[1:0] = SEL_MATRIX_RECT0P_FINE[1:0] then the rectifier0 negative input of the fine block is connected to DC. Otherwise see table below for decode.

Table 12. FINE BLOCK RECTIFIER CONTROL SELECTION

Fine Register Input	Channel Select	Pin
00	0	REC4
00	1	REC0
01	0	REC5
01	1	REC1
10	0	REC6
10	1	REC2
11	0	REC7
11	1	REC3

The next 16 registers hold the calibration coefficients used to calibrate out any sensor non−linearity. See the calibration section for more details.

CLARKE TRANSFORM IMAGINARY COEFFICIENT 0 FOR COARSE BLOCK

Address 0x12 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_IM_A[15:0]	Filter 0 Clarke Transform Imaginary Coefficient for Coarse Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 0 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 1 FOR COARSE BLOCK

Address 0x13 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_IM_B[15:0]	Filter 1 Clarke Transform Imaginary Coefficient for Coarse Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 1 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 2 FOR COARSE BLOCK

Address 0x14 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_IM_C[15:0]	Filter 2 Clarke Transform Imaginary Coefficient for Coarse Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 2 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 3 FOR COARSE BLOCK

Address 0x15 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_IM_D[15:0]	Filter 3 Clarke Transform Imaginary Coefficient for Coarse Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 3 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 0 FOR COARSE BLOCK

Address 0x16 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_RE_A[15:0]	Filter 0 Clarke Transform Real Coefficient for Coarse Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 0 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 1 FOR COARSE BLOCK

Address 0x17 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_RE_B[15:0]	Filter 1 Clarke Transform Real Coefficient for Coarse Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 1 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 2 FOR COARSE BLOCK

Address 0x18 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_RE_C[15:0]	Filter 2 Clarke Transform Real Coefficient for Coarse Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 2 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 3 FOR COARSE BLOCK

Address 0x19 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_COARSE_RE_D[15:0]	Filter 3 Clarke Transform Real Coefficient for Coarse Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 3 output of the Coarse Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 0 FOR FINE BLOCK

Address 0x1A – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_IM_A[15:0]	Filter 0 Clarke Transform Imaginary Coefficient for Fine Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 0 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 1 FOR FINE BLOCK

Address 0x1B – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_IM_B[15:0]	Filter 1 Clarke Transform Imaginary Coefficient for Fine Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 1 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 2 FOR FINE BLOCK

Address 0x1C – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_IM_C[15:0]	Filter 2 Clarke Transform Imaginary Coefficient for Fine Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 2 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM IMAGINARY COEFFICIENT 3 FOR FINE BLOCK

Address 0x1D – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_IM_D[15:0]	Filter 3 Clarke Transform Imaginary Coefficient for Fine Block. An Imaginary Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 3 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 0 FOR FINE BLOCK

Address 0x1E – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_RE_A[15:0]	Filter 0 Clarke Transform Real Coefficient for Fine Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 0 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 1 FOR FINE BLOCK

Address 0x1F – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_RE_B[15:0]	Filter 1 Clarke Transform Real Coefficient for Fine Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 1 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 2 FOR FINE BLOCK

Address 0x20 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_RE_C[15:0]	Filter 2 Clarke Transform Real Coefficient for Fine Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 2 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

CLARKE TRANSFORM REAL COEFFICIENT 3 FOR FINE BLOCK

Address 0x21 – Default 0x0000

Bit	Name	Description
15:0	CLARKE_FINE_RE_D[15:0]	Filter 3 Clarke Transform Real Coefficient for Fine Block. A Real Coefficient of the Clarke Transform. This coefficient is applied to the Filter/Rectifier 3 output of the Fine Block. This register is a fixed point number with 14 sign bits, in Q format as Q2.14

VELOCITY COEFFICIENT MSB FOR ABSOLUTE ALGORITHM EXTRAPOLATION

Address 0x22 – Default 0x0000

This register allows for the tuning of the extrapolation algorithm. Please refer to the extrapolation tuning section for more details.

Bit	Name	Description
15:8		
7:0	ABSALGO_EXTRP_KV[23:16]	Velocity Coefficient MSBs for Absolute Algorithm Extrapolation. The coefficient used in the velocity portion in the angle extrapolation algorithm.

VELOCITY COEFFICIENT LSB FOR ABSOLUTE ALGORITHM EXTRAPOLATION

Address 0x23 – Default 0x7E75

This register allows for the tuning of the extrapolation algorithm. Please refer to the extrapolation tuning section for more details.

Bit	Name	Description
15:0	ABSALGO_EXTRP_KV[15:0]	Velocity Coefficient LSBs for Absolute Algorithm Extrapolation. The coefficient used in the velocity portion in the angle extrapolation algorithm.

VELOCITY COEFFICIENT MSB FOR DIGITAL FILTER EXTRAPOLATION

Address 0x26 – Default 0x0084

This register allows for the tuning of the extrapolation algorithm. Please refer to the extrapolation tuning section for more details.

Bit	Name	Description
15:8		
7:0	DIG_FILTERS_EXTRP_KV[23:16]	Velocity Coefficient MSBs for the Delay Extrapolator. The coefficient used in the velocity portion of the Delay extrapolator.

VELOCITY COEFFICIENT LSB FOR DIGITAL FILTER EXTRAPOLATION

Address 0x27 – Default 0x0561

This register allows for the tuning of the extrapolation algorithm. Please refer to the extrapolation tuning section for more details.

Bit	Name	Description
15:0	DIGFILTERS_EXTRP_KV[15:0]	Velocity Coefficient LSBs for Digital Filter Extrapolation. The coefficient used in the velocity portion of the Delay extrapolator.

LOW PASS FILTER FOR DIGITAL FILTER

Address 0x2A – Default 0x003F

This register allows for the tuning of the digital low pass filter that is applied to the digitized receiver coil samples.

Bit	Name	Description
15:6		Reserved.
5:4	LPF_K_ANG[1:0]	Low Pass Filter Coefficient for Angle = 00 then the angle LPF coefficient is 16(default); = 01 then the angle LPF coefficient is 32; = 10 then the angle LPF coefficient is 64; = 11 then the angle LPF coefficient is 128.
3:2	LPF_K_VEL[1:0]	Low Pass Filter Coefficient for Velocity = 00 then the velocity LPF coefficient is 16 (default); = 01 then the velocity LPF coefficient is 32; = 10 then the velocity LPF coefficient is 64; = 11 then the velocity LPF coefficient is 128.
1:0	Reserved	Reserved.

DIGITAL CONTROL

Address 0x2B –Default 0x0020

This register allows the user to control the source of the output data. Below is a graphical representation of the MUX options

Bit	Name	Description
15:6		Reserved.
5:4	ANGLE_OUTPUT_MUX	Angle Output Mux The angle coming out of the DSP block is the 00 = Delay Extrapolated angle 01 = Delay Extrapolated angle 10 = Digital LPF angle 11 = Absolute Algorithm angle
3		Reserved.
2	CAL_TURN_DIRECTION	0 = Position set to increasing for clockwise rotation in calibration routine. 1 = Position set to increasing for counter clockwise rotation in calibration routine
1	ADCCAL_AT_POR_DIS	ADC Calibration at POR Disable (default) ADC calibration is not run during startup routine
0	OPENCOILDET_AT_POR_DIS.	Open Coil Detection at POR Disable. Open Coil Detection FSM is not run during startup routine.

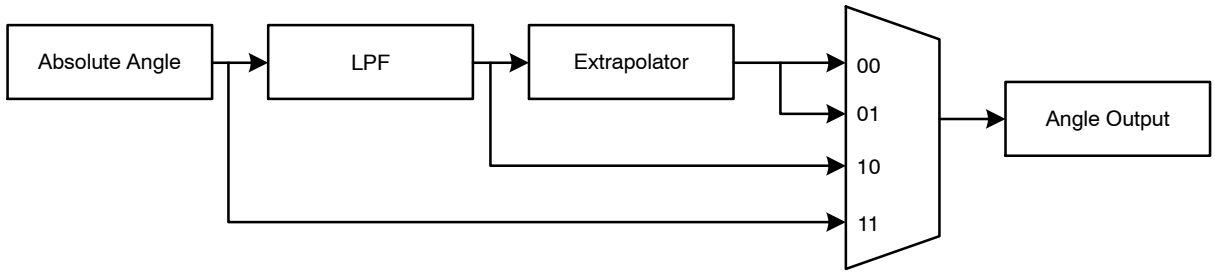


Figure 9.

CHANNEL SELECT

Address 0x2F – Default 0x0000

This register controls where the outputs of each ADC go. There are two ADCs, and their mapping to the fine and coarse coils is as follows:

Bit	Name	Description
15:1		Reserved.
0	FINE_CHANB_SEL	When 1, Receiver pins 0−3 are mapped to the Fine block. When 0, Receiver pins 0−3 are mapped to the Coarse block. Receiver pins 4−7 are mapped to the opposite block.

LC OSCILLATOR GAIN DAC CONTROL

Address 0x40 – Default 0x0000

This register allows the user to bypass the automatically calculated value for the LC oscillator gain setting. In order to force a gain setting, the user must set bit 15 and put the desired gain value in bit 7:0. This will turn off the automatic periodic gain adjustment and instead use the value set in bits 7:0.

Bit	Name	Description
15	SHDW_LC_GAIN_DAC_EN	LC Oscillator Gain DAC Enable. The LC Oscillator is forced to use the SHDW_LC_GAIN_DAC register value.
14:8		Reserved.
7:0	SHDW_LC_GAIN_DAC[7:0]	LC Oscillator Gain DAC. The LC Oscillator current $I_{LC,OSC}$ is related to the DAC value from the equation: *Code Gain Calculation* 0b'00xxxxxx 0.4 + (0.05 * N) mA 0b'01xxxxxx 3.6 + (0.1 * N) mA 0b'10xxxxxx 10 + (0.2 * N) mA 0b'11xxxxxx 22.8 + (0.4 * N) mA where 'N' is the 'xxxxxx' portion of the code

LC OSCILLATOR GAIN TIME CONTROL

Address 0x41 – Default 0x01F4

This register allows the user to change the periodic update timing for the LC oscillator gain.

Bit	Name	Description
15:0	SHDW_LC_GAIN_TIME[15:0]	LC Oscillator Gain Time Control. The LC Oscillator Gain controller updates the LC Oscillator Gain DAC value every SHDW_LC_GAIN_TIME[15:0] * 2 μs (2 μs = 80 clock periods at 40 MHz). If SHDW_LC_GAIN_TIME[15:0]=0 then the FSM does NOT update the LC Oscillator Gain DAC value.

PGA COARSE GAIN DAC CONTROL

Address 0x42 – Default 0x0000

This register allows the user to bypass the automatically calculated value for the coarse PGA gain setting. In order to force a gain setting, the user must set bit 15 and put the desired gain value in bit 5:0. This will turn off the automatic periodic gain adjustment and instead use the value set in bits 5:0.

Bit	Name	Description
15	SHDW_PGA_COARSE_GAIN_DAC_EN	PGA Gain DAC Enable Coarse Block. The Coarse block PGA Gain DAC is forced to use the SHDW_PGA_COARSE_GAIN_DAC register value.
14:6		Reserved.
5:0	SHDW_PGA_COARSE_GAIN_DAC[5:0]	PGA Gain DAC Coarse Block. The PGA Gain G_{PGA} is related to SHDW_PGA_GAIN_DAC[5:0] by the equation: G_{PGA} = (1.189^SHDW_PGA_GAIN_DAC[5:0]) * 10, for codes 0 to 22.

PGA FINE GAIN DAC CONTROL

Address 0x43 – Default 0x0000

This register allows the user to bypass the automatically calculated value for the fine PGA gain setting. In order to force a gain setting, the user must set bit 15 and put the desired gain value in bit 5:0. This will turn off the automatic periodic gain adjustment and instead use the value set in bits 5:0.

Bit	Name	Description
15	SHDW_PGA_FINE_GAIN_DAC_EN	PGA Gain DAC Enable Fine Block. The Fine block PGA Gain DAC is forced to use the SHDW_PGA_FINE_GAIN_DAC register value.
14:6		Reserved.
5:0	SHDW_PGA_FINE_GAIN_DAC[5:0]	PGA Gain DAC Fine Block. The PGA Gain G_{PGA} is related to SHDW_PGA_FINE_GAIN_DAC[5:0] by the equation: G_{PGA} = (1.189^SHDW_PGA_GAIN_DAC[4:0]) * 10, for codes 0 to 22.

PGA GAIN TIME CONTROL

Address 0x44 – Default 0x01F4

This register allows the user to change the periodic update timing for the PGA gain.

Bit	Name	Description
15:0	SHDW_PGA_GAIN_TIME[15:0]	PGA Gain Time Control Both blocks update the PGA Gain DAC value every SHDW_PGA_FINE_GAIN_TIME[15:0] * 2 μs (2 μs = 80 clock periods at 40 MHz). If SHDW_FINE_PGA_GAIN_TIME[15:0]=0 then the controllers do NOT update the PGA Gain DAC values.

PGA COARSE OFFSET DAC CONTROL

Address 0x45 – Default 0x0000

This register allows the user to bypass the automatically calculated value for the coarse PGA offset setting. In order to force a gain setting, the user must set bit 15 and put the desired gain value in bit 7:0. This will turn off the automatic periodic gain adjustment and instead use the value set in bits 7:0.

Bit	Name	Description
15	SHDW_PGA_COARSE_OFFSET_DAC_EN	PGA Offset DAC Enable Coarse Block. The Coarse block PGA Offset DAC is forced to use the SHDW_PGA_COARSE_OFFSET_DAC register value.
14:8		Reserved.
7:0	SHDW_PGA_COARSE_OFFSET_DAC[7:0]	PGA Offset DAC. SHDW_PGA_COARSE_OFFSET_DAC[7:0] is a 2 μs complement value covering an offset range of [−32mV, 32mV]. The DAC LSB is equivalent to 250 μV.

PGA FINE OFFSET DAC CONTROL

Address 0x46 – Default 0x0000

This register allows the user to bypass the automatically calculated value for the fine PGA offset setting. To force a gain setting, the user must set bit 15 and put the desired gain value in bit 7:0. This will turn off the automatic periodic gain adjustment and instead use the value set in bits 7:0.

Bit	Name	Description
15	SHDW_PGA_FINE_OFFSET_DAC_EN	PGA Offset DAC Enable Fine Block. The Fine block PGA Offset DAC is forced to use the SHDW_PGA_FINE_OFFSET_DAC register value.
14:8		Reserved.
7:0	SHDW_PGA_FINE_OFFSET_DAC[7:0]	PGA Offset DAC. SHDW_PGA_FINE_OFFSET_DAC[7:0] is a 2 μs complement value covering an offset range of [−32 mV, 32 mV]. The DAC LSB is equivalent to 250 μV.

PGA OFFSET TIME CONTROL

Address 0x47 – Default 0x01F4

This register allows the user to change the periodic update timing for the PGA offset.

Bit	Name	Description
15:0	SHDW_PGA_COARSE_OFFSET_TIME[15:0]	PGA Offset Time Control x Fine/Coarse Block. Both blocks update the PGA Offset DAC value every SHDW_PGA_COARSE_OFFSET_TIME[15:0] * 2 μs (2 μs = 80 clock periods at 40 MHz). If SHDW_PGA_COARSE_OFFSET_TIME[15:0]=0 then the controllers do NOT update the PGA Offset DAC values.

ANGLE EXTRAPOLATOR TIME CONTROL

Address 0x48 – Default 0x0000

This register controls the update rate of the angle extrapolation feature.

Bit	Name	Description
15:0	SHDW_LC_GAIN_EXTRP_TIME[15:0]	Angle Extrapolation Time Control. The Angle Extrapolation runs for SHDW_LC_GAIN_EXTRP_TIME [15:0] * 2 μs (2 μs = 80 clock periods at 40 MHz) after a qualifying event. If SHDW_LC_GAIN_EXTRP_TIME [15:0]=0 then the Angle Extrapolator does NOT run.

NORMAL WAKEUP DELAY

Address 0x4C – Default 0x1000

This register controls the number of clock cycles used to wait for the analog to settle after transitioning to the Functional state from the sleep state.

Bit	Name	Description
15:0	LP_Normal_Delay_Time[15:0]	Number of clock cycles used to wait for the analog to settle after coming out of sleep mode.

STARTUP DELAY TIME MSB

Address 0x4D – Default 0x0006

This register controls the startup timing of analog blocks in the NCS32100. This is the amount to time that the digital sequencing is held in reset to allow settling time for the analog front end circuitry to settle during the initial startup routine.

Bit	Name	Description
15:3		Reserved
2:0	STARTUP_SETTLE[18:16]	Startup Settle MSB Number of clock cycles used to wait for the analog to settle during startup.

STARTUP DELAY TIME LSB

Address 0x4E – Default 0x1A80

This register controls the startup timing of analog blocks in the NCS32100. This is the amount to time that the digital sequencing is held in reset to allow settling time for the analog front end circuitry to settle during the initial startup routine.

Bit	Name	Description
15:0	STARTUP_SETTLE[15:0]	Startup Settle LSB Number of clock cycles used to wait for the analog to settle during startup.

DSP WAKEUP DELAY

Address 0x4F Default: 0x1000

This register controls the startup timing of the DSP block in the NCS32100. This is the amount to time that the digital sequencing is held in reset to allow settling time for the analog front−end circuitry to settle during battery mode when the device transitions between a sleep state and a low power.

Bit	Name	Description
15:0	DSP_WAKEUP_DLY_TIME[15:0]	Number of clock cycles used to wait for the analog to settle after transitioning to the Low power state from the Sleep state.

AUTOZERO ANGLE MSB

Address 0x50 – Default 0x0000

This register holds the most significant bits that define the encoder 0 index position. It is an offset from the true index that is applied to the position output so that the user can set a custom index. This value is held in non−volatile memory.

Bit	Name	Description
15:4		Reserved.
3:0	SHDW_AUTOZERO_ANGLE[19:16]	Autozero Angle MSB. Value used to offset the Mechanical angle from the Absolute Angle algorithm

AUTOZERO ANGLE LSB

Address 0x51 – Default 0x0000

This register holds the least significant bits that define the encoder 0 index position. It is an offset from the true index that is applied to the position output so that the user can set a custom index. This value is held in non−volatile memory.

Bit	Name	Description
15:0	SHDW_AUTOZERO_ANGLE[15:0]	Autozero Angle LSB. Value used to offset the Mechanical angle from the Absolute Angle algorithm

INPUT/OUTPUT CONTROL

Address 0x57 – Default 0x0008

This register allows the user to select the direction of the external Data pins.

Bit	Name	Description
15:4		Reserved.
3	DATA3_OUT_EN	DATA3 Output Enable. = 0 then the package pin DATA3 is configured to be an output; = 1 then the package pin DATA3 is configured to be an input.
2	DATA2_OUT_EN	DATA2 Output Enable. = 0 then the package pin DATA2 is configured to be an output; = 1 then the package pin DATA2 is configured to be an input.
1	DATA1_OUT_EN	DATA1 Output Enable. = 0 then the package pin DATA1 is configured to be an output; = 1 then the package pin DATA1 is configured to be an input.
0	DATA0_OUT_EN	DATA0 Output Enable. = 0 then the package pin DATA0 is configured to be an output; = 1 then the package pin DATA0 is configured to be an input.

SENSOR SELECTION

Address 0x5F – Default 0x0013

This register should be set based on the number of coarse and fine loops that exist in the sensor.

Bit	Name	Description
15:5		Reserved.
4	SENSOR_COARSE_SEL	Sensor Coarse Selection = 0 then the Coarse sensor period is 3 times the mechanical angle period; = 1 then the Coarse sensor period is 5 times the mechanical angle period;
3		Reserved.
2:0	SENSOR_FINE_SEL[2:0]	Sensor Fine Selection = 000 then the Fine sensor period is 8 times the mechanical angle period; = 001 then the Fine sensor period is 16 times the mechanical angle period; = 010 then the Fine sensor period is 32 times the mechanical angle period; = 011 then the Fine sensor period is 64 times the mechanical angle period; = 100 then the Fine sensor period is 128 times the mechanical angle period; = 101 then the Fine sensor period is 256 times the mechanical angle period;

SECONDARY CALIBRATION COEFFICIENTS

Address 0x80 through 0x8F – Default 0x0000

These registers hold the 16 secondary calibration coefficients that are used to offset the output position in each of 16 bins respectively. These values are position offsets.

Bit	Name	Description
0x80	Bin0[15:0]	Bin0 position offset (covers position from 348.75 – 11.25 degrees)
0x81	Bin1[15:0]	Bin1 position offset (covers position from 11.25 – 33.75 degrees)
0x82	Bin2[15:0]	Bin2 position offset (covers position from 33.75 – 56.25 degrees)
0x83	Bin3[15:0]	Bin3 position offset (covers position from 56.25 – 78.75 degrees)
0x84	Bin4[15:0]	Bin4 position offset (covers position from 78.75 – 101.25 degrees)
0x85	Bin5[15:0]	Bin5 position offset (covers position from 101.25 – 123.75 degrees)
0x86	Bin6[15:0]	Bin6 position offset (covers position from 123.75 – 146.25 degrees)
0x87	Bin7[15:0]	Bin7 position offset (covers position from 146.25 – 168.75 degrees)
0x88	Bin8[15:0]	Bin8 position offset (covers position from 168.75 – 191.25 degrees)
0x89	Bin9[15:0]	Bin9 position offset (covers position from 191.25 – 213.75 degrees)
0x8A	Bin10[15:0]	Bin10 position offset (covers position from 213.75 – 236.25 degrees)
0x8B	Bin11[15:0]	Bin11 position offset (covers position from 236.25 – 258.75 degrees)
0x8C	Bin12[15:0]	Bin12 position offset (covers position from 258.75 – 281.25 degrees)
0x8D	Bin13[15:0]	Bin13 position offset (covers position from 281.25 – 303.75 degrees)
0x8E	Bin14[15:0]	Bin14 position offset (covers position from 303.75 – 326.25 degrees)
0x8F	Bin15[15:0]	Bin15 position offset (covers position from 326.25 – 348.75 degrees)

BATTER MODE WAKEUP PERIOD

Address 0x90 – Default 0x0100

This register allows the user to set the wakeup period during battery mode. The NCS32100 goes into battery mode anytime VCC < VBAT. In battery mode the NCS32100 wakeup periodically to check the position and update the multi−turn count if a full revolution has passed. The shorter the wakeup period, the more current will be pulled from VBAT.

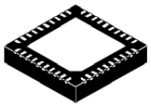
Bit	Name	Description			
15:0	WAKEUP_PER	WAKUP_PER	Period Timing (ms)	Average current draw on VBAT (mA)	Max speed at which turns count will be tracked (rpm)
		3	3	10	6600
		4	5	5	4000
		21	16	1.45	1250
		31	24	1	830
		42	31	0.8	650
		55	41	0.6	487
		72	53	0.5	370
		100	73	0.4	270
		200	140	0.3	140

This data sheet provides a high−level description of the NCS32100 features and use cases. Additional documentation will be available to further define key aspects of NCS32100 configuration and use cases. Additional documentation includes:

NCS32100 Reference Design Manual – Details the reference design system used to prove < 20arcsec accuracy with a 37.5 mm diameter PCB sensor.

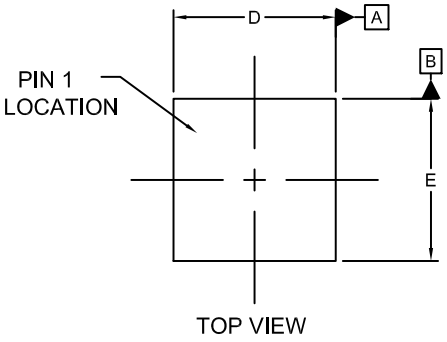
NCS32100 Sensor Design Application Note – Details the considerations and variable trade space involved in designing a rotary inductive PCB sensor.

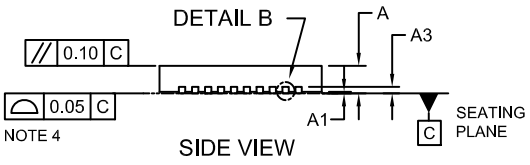
NCS32100 Advanced Configuration Manual – Gives examples and additional content for sensor interface configuration, filtering configuration, extrapolation configuration, and gain control configuration.

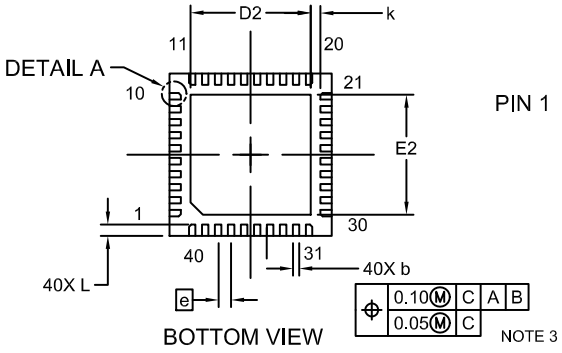


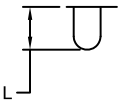
QFN40 5x5, 0.4P
CASE 485FW
ISSUE O

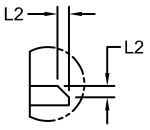
DATE 17 JAN 2019





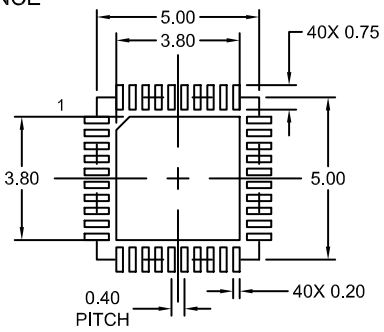






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	1.00
A1	—	—	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e		0.40 BSC	
K	0.25	—	---
L	0.30	0.35	0.40
L2		0.118 REF	



RECOMMENDED LANDPATTERN*

*For additional information on our Pb-Free strategy and soldering details, please download the On Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN40 5x5, 0.4P**	**PAGE 1 OF 1**

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