NCS2552

750 MHz Voltage Feedback Op Amp with Fast Enable Feature

NCS2552 is a 750 MHz voltage feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The voltage feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

Features

- −3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 V_{p-p}) 750 MHz Typ
- Slew Rate 1700 V/μs
- Fast Enable Time 5.0 ns
- Supply Current 13 mA
- Input Referred Voltage Noise 5.0 nV/$\sqrt{Hz}$
- THD −64 dBc (f = 5.0 MHz, V_O = 2.0 V_{p-p})
- Output Current 100 mA
- Pin Compatible with EL5157, AD8057
- This is a Pb−Free Device

Applications

- Line Drivers
- Radar/Communication Receivers

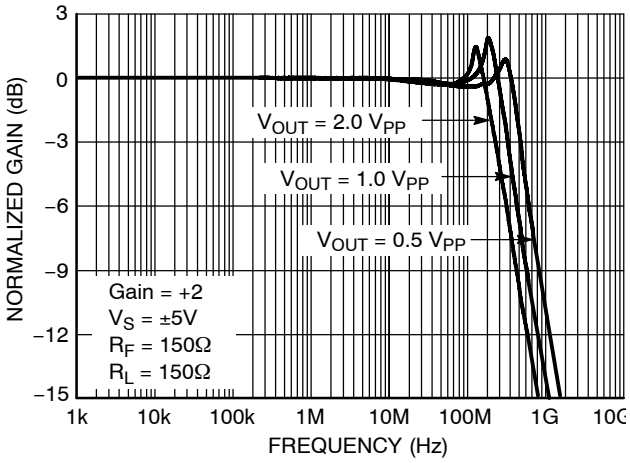


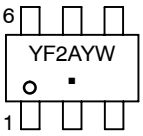
Figure 1. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

ON Semiconductor®

http://onsemi.com

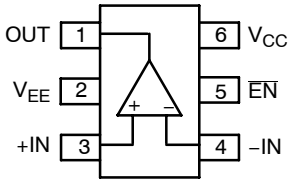
MARKING DIAGRAM

SOT23−6 (TSOP−6) SN SUFFIX CASE 318G



YF2, N2552	= NCS2552
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

SOT23−6 PINOUT

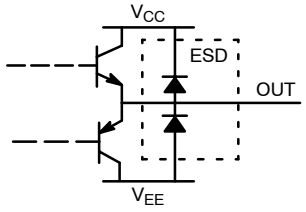
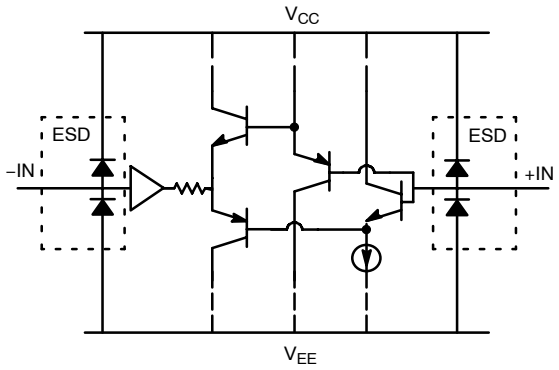
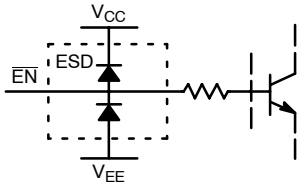


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin (SOT23/SC70)	Symbol	Function	Equivalent Circuit
1	OUT	Output	
2	V_{EE}	Negative Power Supply	
3	+IN	Non−inverted Input	
4	−IN	Inverted Input	See Above
6	V_{CC}	Positive Power Supply	
5	$\overline{EN}$	Enable	

ENABLE PIN TRUTH TABLE

	High	Low*
Enable	Disabled	Enabled

*Default open state

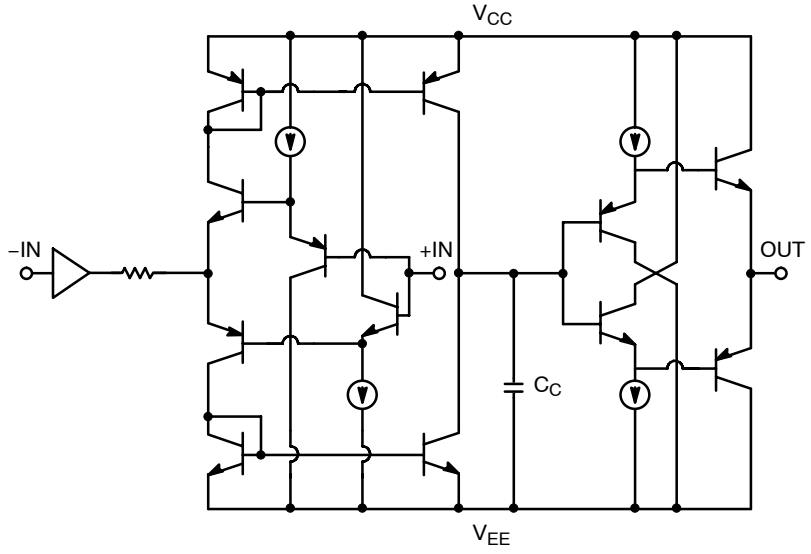


Figure 2. Simplified Device Schematic

ATTRIBUTES

Characteristics	Value
ESD Human Body Model Machine Model Charged Device Model	 2.0 kV 200 V 1.0 kV
Moisture Sensitivity (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_S	11	Vdc
Input Voltage Range	V_I	$\leq V_S$	Vdc
Input Differential Voltage Range	V_{ID}	$\leq V_S$	Vdc
Output Current	I_O	100	mA
Maximum Junction Temperature (Note 2)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	158	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device damage.

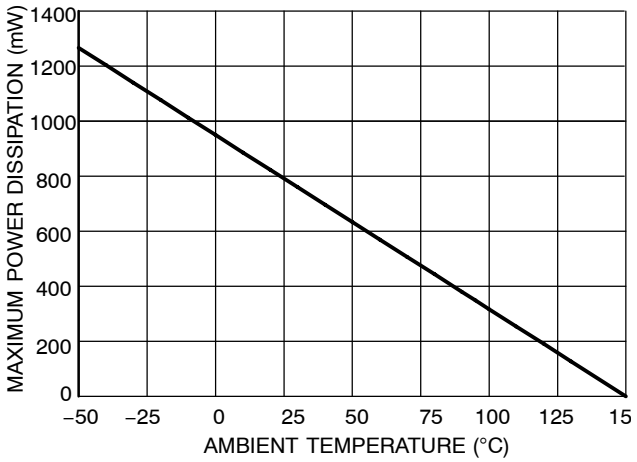


Figure 3. Power Dissipation vs. Temperature

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 750 350		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		40		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		1700		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 2.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		2.0		ns
t_{ON}	Turn−on Time			5.0		ns
t_{OFF}	Turn−off Time			15		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−64		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−75		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		40		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		55		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		4.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).Closed Loop
Open Loop

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 3)		3.0			V
V_{IL}	Input Low Voltage (Enable) (Note 3)				1.0	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 3)		±3.0	±3.2		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.1 13		Ω
V_O	Output Voltage Range		±3.0	±4.0		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			10		V
$I_{S,ON}$	Power Supply Current – Enabled		5.0	13	17	mA
$I_{S,OFF}$	Power Supply Current – Disabled			0.5	0.8	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	56		dB

3. Guaranteed by design and/or characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 550 200		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		35		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.02		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		900		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 1.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		1.7		ns
t_{ON}	Turn−on Time			5.0		ns
t_{OFF}	Turn−off Time			15		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−60		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−63		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 0.5 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		63		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		4.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 3)		1.5			V
V_{IL}	Input Low Voltage (Enable) (Note 3)				0.5	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 3)		±1.1	±1.6		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.1 13		Ω
V_O	Output Voltage Range		±1.1	±1.6		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			5.0		V
$I_{S,ON}$	Power Supply Current – Enabled		5.0	11.5	17	mA
$I_{S,OFF}$	Power Supply Current – Disabled			0.5	0.8	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	56		dB

4. Guaranteed by design and/or characterization.

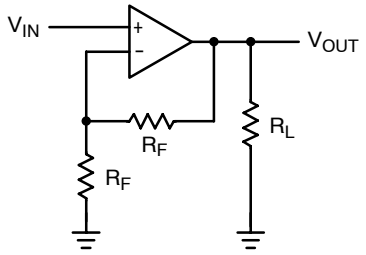


Figure 4. Typical Test Setup (A_V = +2.0, R_F = 1.0 kΩ, R_L = 100 Ω)

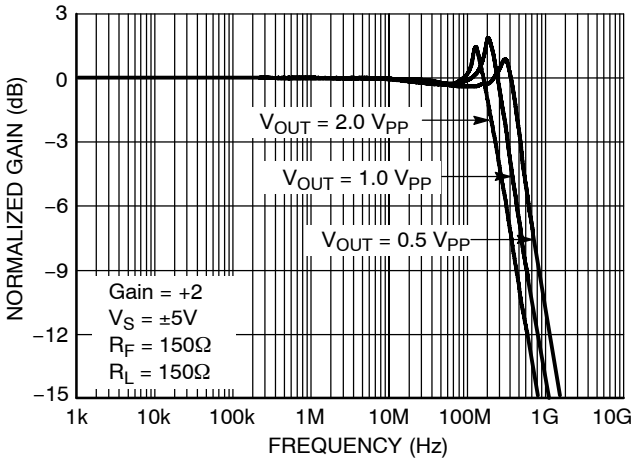


Figure 5. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

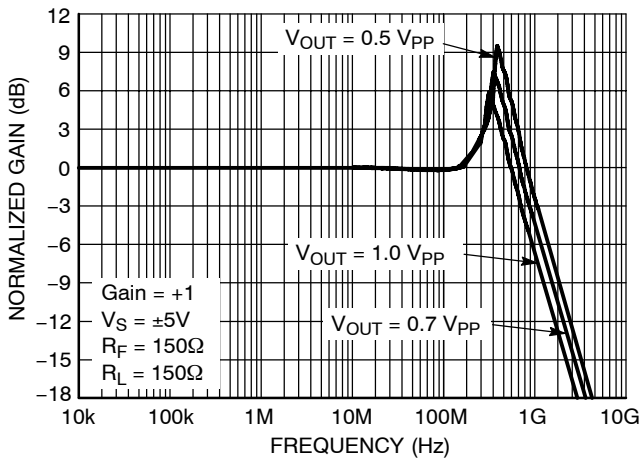


Figure 6. Frequency Response: Gain (dB) vs. Frequency Av = +1.0

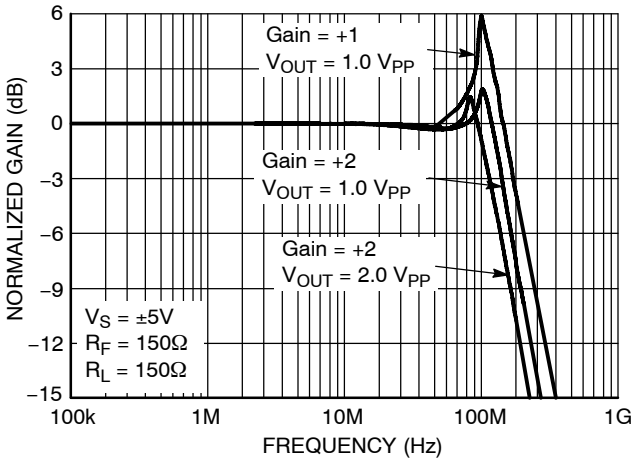


Figure 7. Large Signal Frequency Response Gain (dB) vs. Frequency

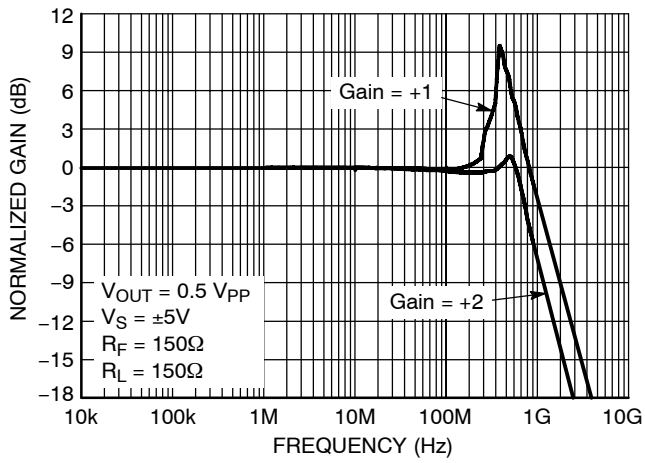


Figure 8. Small Signal Frequency Response Gain (dB) vs. Frequency

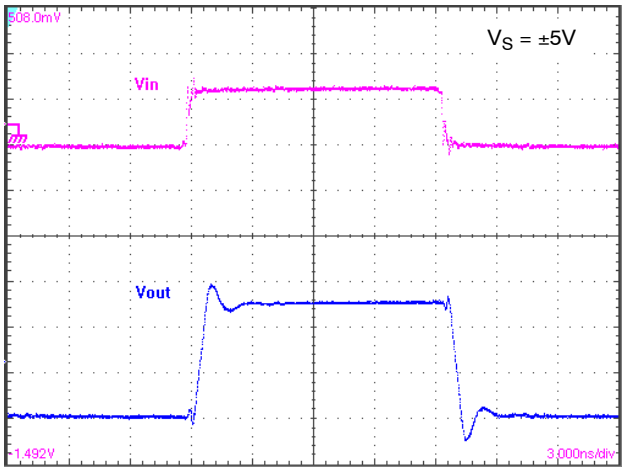


Figure 9. Small Signal Step Response Vertical: 20 mV/div Horizontal: 3 ns/div

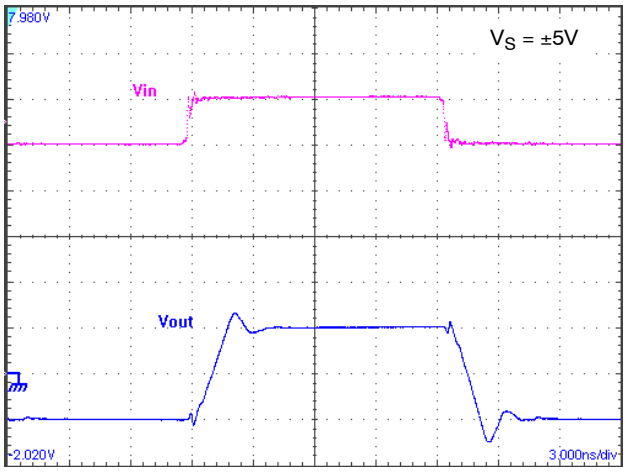


Figure 10. Large Signal Step Response Vertical: 1 V/div Horizontal: 3 ns/div

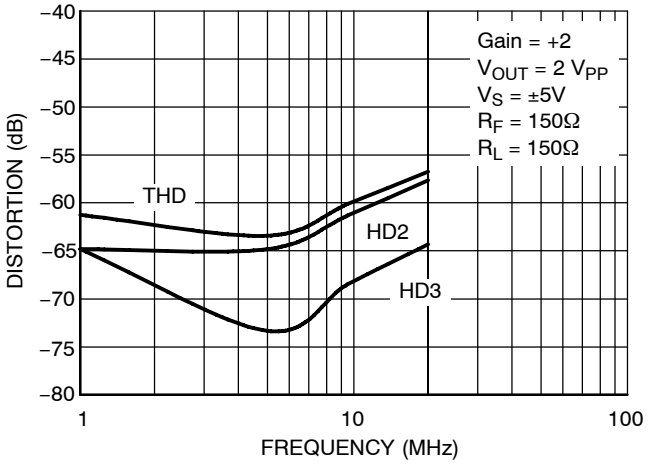


Figure 11. THD, HD2, HD3 vs. Frequency

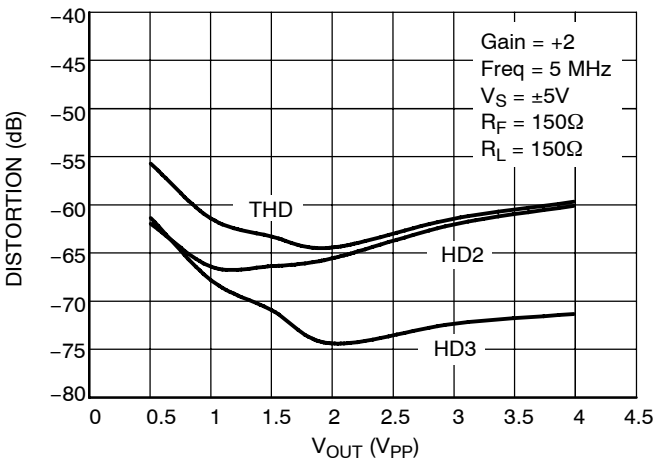


Figure 12. THD, HD2, HD3 vs. Output Voltage

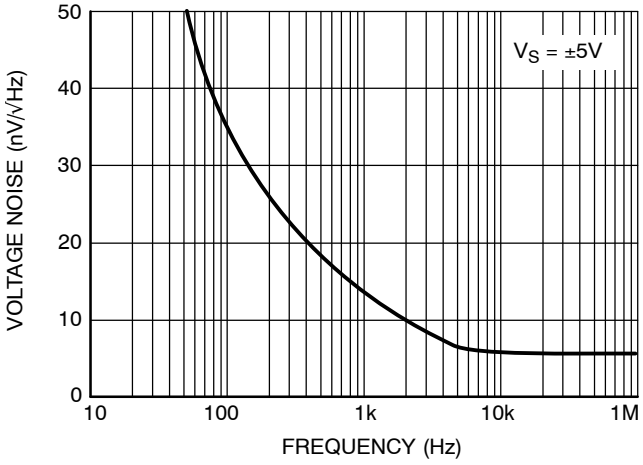


Figure 13. Input Referred Voltage Noise vs. Frequency

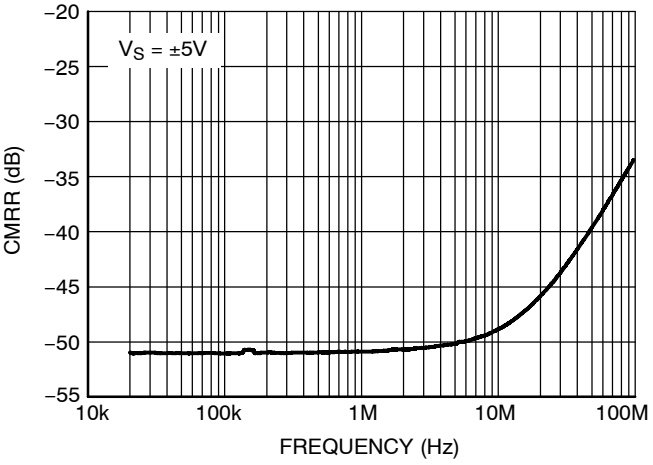


Figure 14. CMRR vs. Frequency

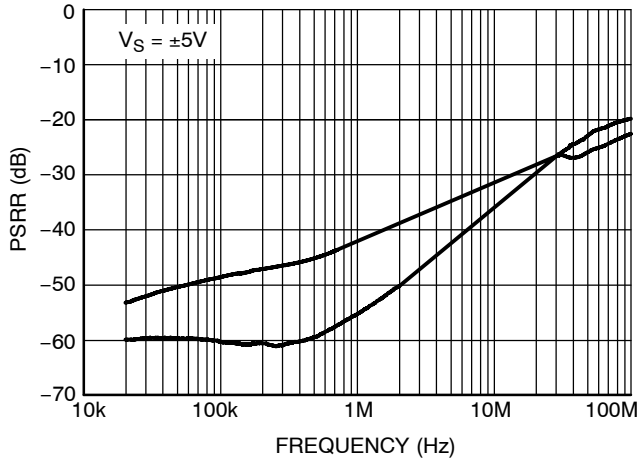


Figure 15. PSRR vs. Frequency

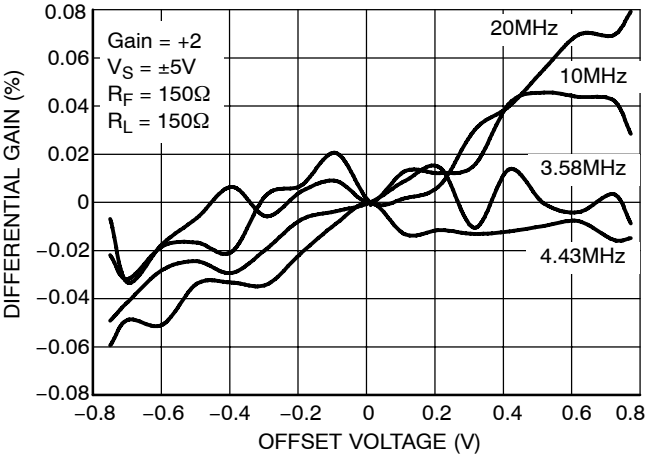


Figure 16. Differential Gain

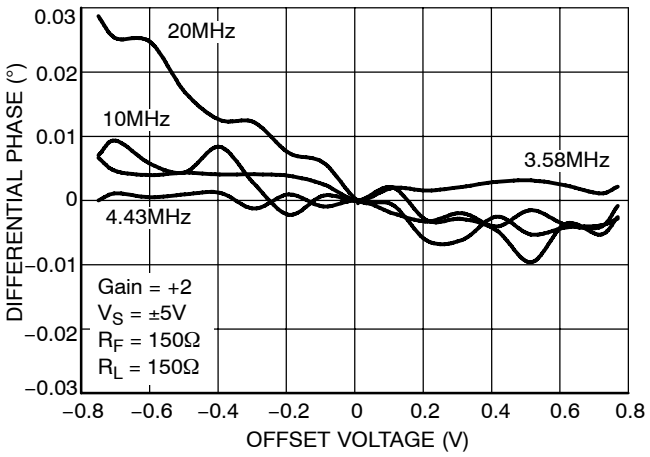


Figure 17. Differential Phase

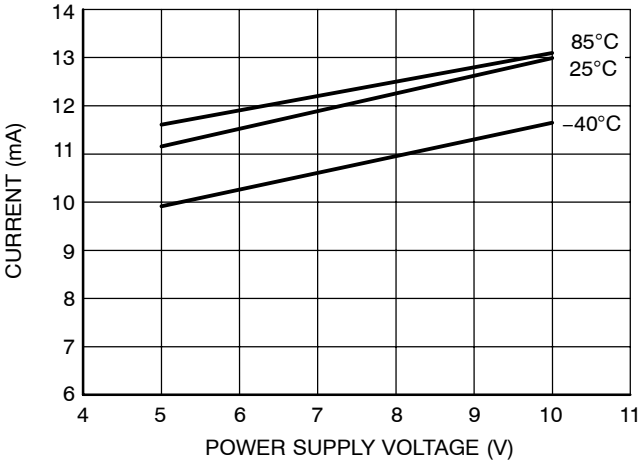


Figure 18. Supply Current vs. Power Supply (Enabled)

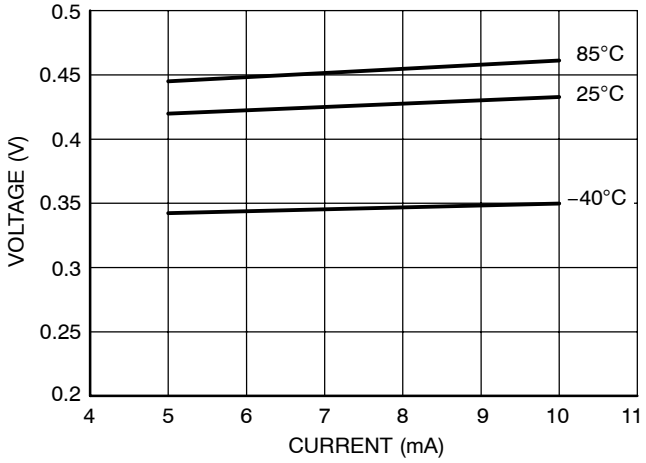


Figure 19. Supply Current (Disabled)

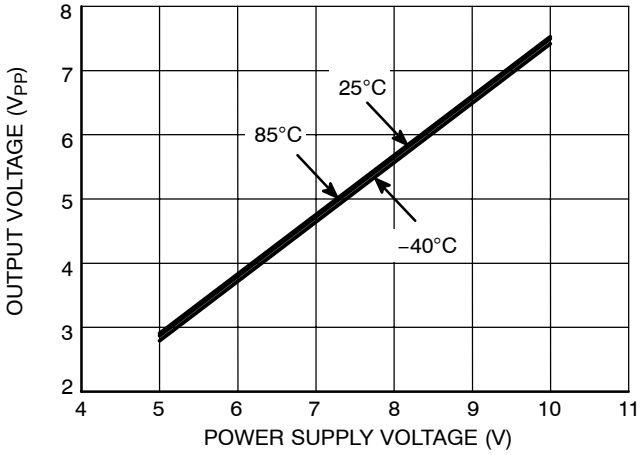


Figure 20. Output Voltage Swing vs. Supply Voltage

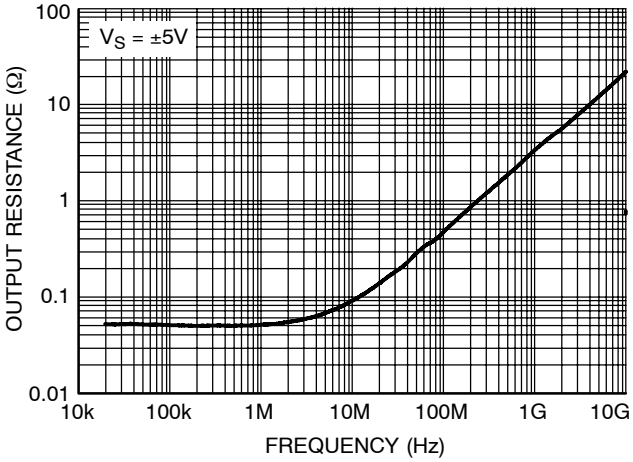


Figure 21. Closed Loop Output Resistance vs. Frequency

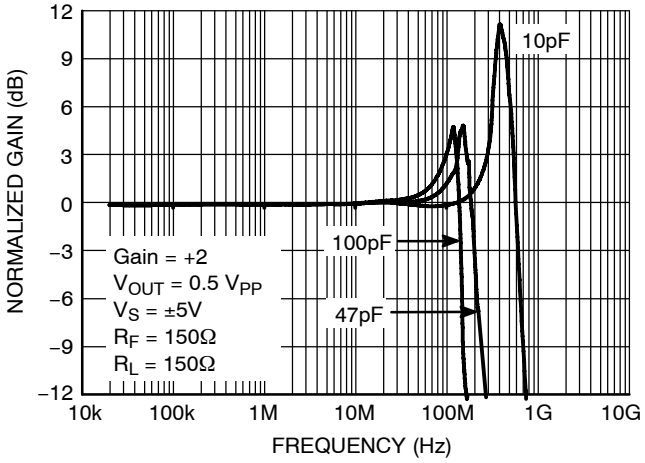


Figure 22. Frequency Response vs. Capacitive Load

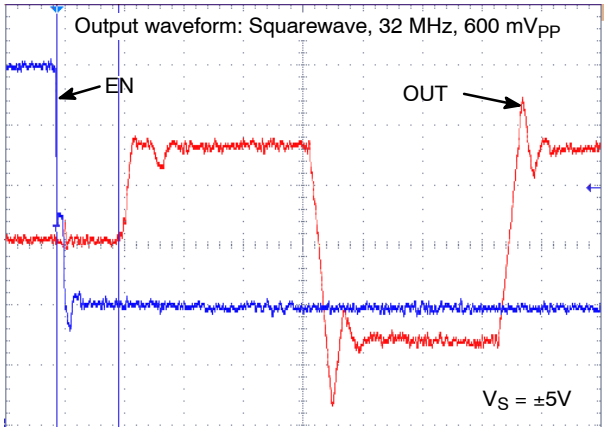


Figure 23. Turn ON Time Delay
Vertical: 500 mV/div (Enable), 200 mV/div (Output)
Horizontal: 5 ns/div

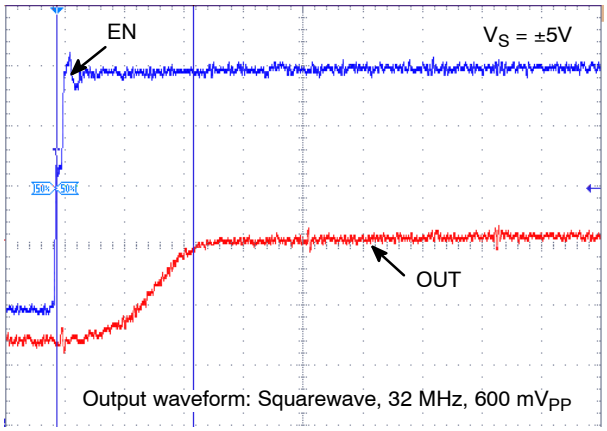


Figure 24. Turn OFF Time Delay
Vertical: 500 mV/div (Enable), 200 mV/div (Output)
Horizontal: 5 ns/div

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 25). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed−loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed−loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.

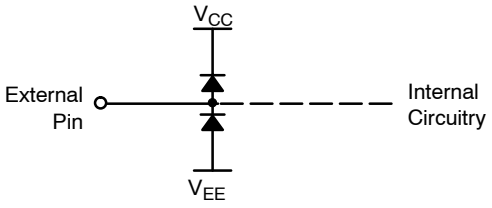
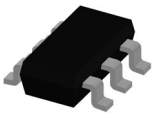


Figure 25. Internal ESD Protection

ORDERING INFORMATION

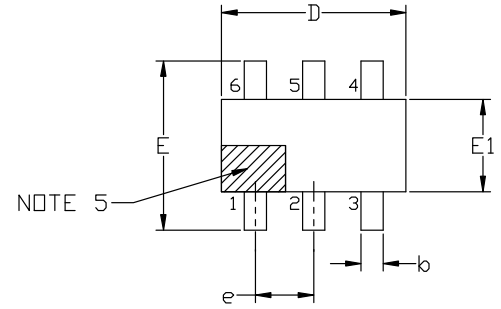
Device	Package	Shipping†
NCS2552SNT1G	SOT23−6 (TSOP−6) (Pb−Free)	3000 Tape & Reel

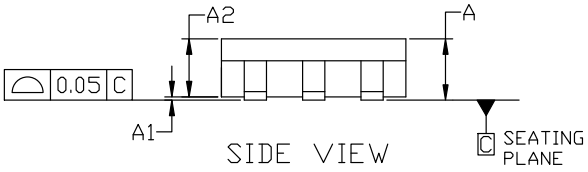
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

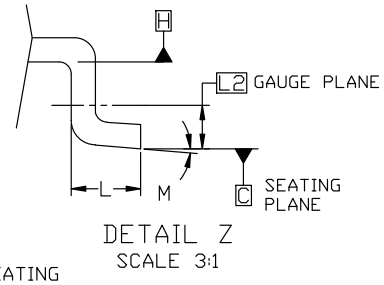


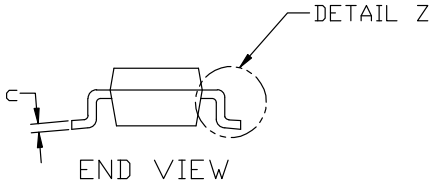
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024



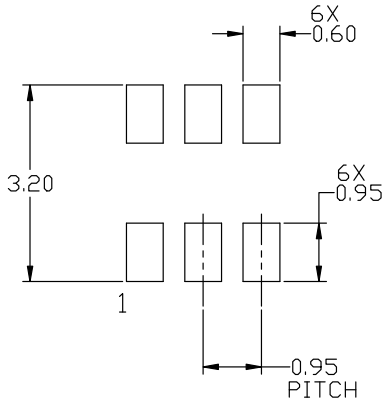






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



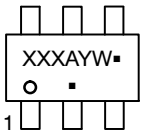
RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

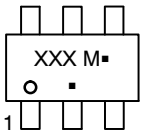
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales