Single-Phase Voltage Regulator for Computing Applications

NCP81561

QFN20
CASE 485EE

The NCP81561 is a high−performance, low−bias current, single−phase regulator with integrated power MOSFET driver. Operating in high switching frequency up to 600 kHz allows employing small size inductor and capacitors. The controller makes use of **onsemi**'s patented high performance RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous−frequency−scaling operation and continuous−mode full−power operation. The NCP81561 has an ultra−low offset current monitor amplifier with programmable offset compensation for high−accuracy current monitoring.

Features

- Auto DCM Operation
- High Performance RPM Control System
- 2−Bit VID Selects 0 V and Three Preset Voltages
- Ultra Low Offset I_{OUT} Monitor with DCR Current Sense
- Differential Remote Output Voltage Sensing
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Dynamic VID Feed−forward
- Externally Programmable Droop Gain
- Automatic Power Saving Mode
- Input Supply Voltage Feed−forward Control
- Built−in Over−voltage, Under−voltage and Pin Programmable Over−current Protection
- Power Good Output
- Zero Droop Capable
- Ultrasonic Operation
- Programmable Operating Frequency
- QFN20 4 mm x 4 mm Package

Applications

- Notebooks, Desktops & Servers
- I/O Supplies
- System Power Supplies
- Graphic Cards

MARKING DIAGRAMS

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP81561MNTXG	QFN20 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

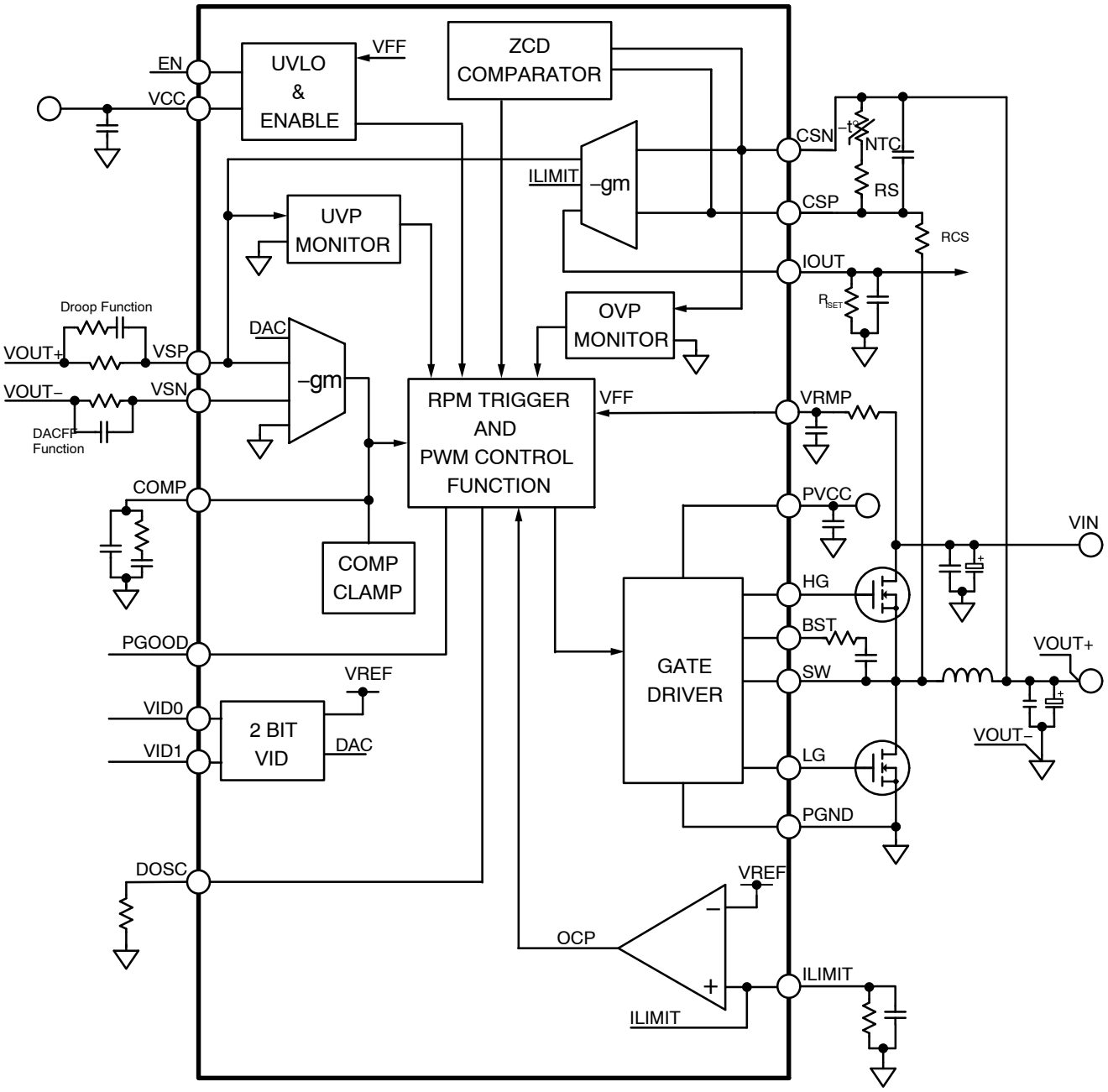


Figure 1. Block Diagram

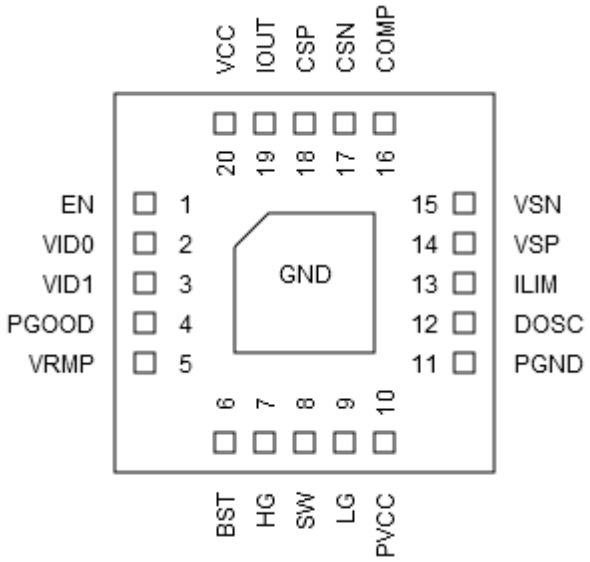


Figure 2. Pin Configuration

Table 1. PIN DESCRIPTION

Pin	Name	Description
1	EN	Logic control to enable the part.
2	VID0	Logic input for reference voltage selector. Use in conjunction with the VID1 pin to select among four set−point reference voltages.
3	VID1	Logic input for reference voltage selector. Use in conjunction with the VID0 pin to select among four set−point reference voltages.
4	PGOOD	Power good indicator of the output voltage. Open−drain output
5	VRMP	Feed−forward input of Vin for the ramp slope compensation. The voltage on this pin is used to control of the ramp of PWM slope. This pin should be filtered to GND using a 10 nF capacitor and connected to Vin via a 1 kΩ resistor.
6	BST	Provides bootstrap voltage for the HS gate driver. A cap is required from this pin to SW.
7	HG	Gate driver output for the top N−channel MOSFET.
8	SW	Switching node between the external top MOSFET and bottom MOSFET
9	LG	Gate driver output for bottom N−channel MOSFET.
10	PVCC	Power supply for MOSFET gate drivers. Place a 4.7 μF or larger ceramic capacitor between this pin and PGND.
11	PGND	Power ground for MOSFET gate drive
12	DOSC	Select the switching frequency by connecting a resistor from this pin to ground.
13	ILIM	Current−limit programming
14	VSP	Differential output voltage sense positive
15	VSN	Differential output voltage sense negative
16	COMP	Compensation return for single phase regulator
17	CSN	Differential current sense negative
18	CSP	Differential current sense positive
19	IOUT	IOUT gain programming
20	VCC	Power supply input pin of control circuits. A 1 μF or larger ceramic capacitor bypasses this input to ground, placed close to the controller
21	GND	Analog ground. Bottom thermal pad.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Switch node to PGND	V_{SW}	−0.3 −7 (< 5 ns)	30 33 (< 40 ns)	V
VCC to GND	V_{CC}	−0.3	6	V
PVCC to PGND	PV_{CC}	−0.3	6	V
VRMP to PGND	V_{RMP}	−0.3	25	V
BST to PGND	BST_PGND	−0.3	33	V
BST to SW	BST_SW	−0.3	6 7 (< 100 ns)	V
HG to SW	HG	−0.3 −2 (<200 ns)	BST + 0.3	V
LG to GND	LG	−0.3 −2 (<200 ns)	PV_{CC} + 0.3	V
VSN to GND	VSN	−0.3	0.3	V
PGND to GND	PGND	−0.3	0.3	V
Other Pins		−0.3	V_{CC} + 0.3	V
Latch Up Current: (Note 1) – All pins, except digital pins – Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Moisture Sensitivity Level	MSL	1		
ESD Human Body Model	HBM	2000		V
ESD Charged device model	CDM	1000		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Latch up Current per JEDEC standard: JESD78 Class II.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Board	$R_{\theta JB}$	8.2	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	21.8	°C/W

Table 4. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
VCC Voltage Range	V_{CC}	4.75	5.25	V
PVCC Voltage Range	PV_{CC}	4.75	5.25	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC}= 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Quiescent Current	EN = high		8	12	mA
	EN = high, VID[0..1] = 00		70		μA
	EN = low		400		μA
VCC UVLO Threshold	VCC rising			4.6	V
	VCC falling	3.9			V
VCC UVLO Hysteresis			150		mV
VRMP UVLO Threshold	VIN rising			4.25	V
	VIN falling	3			V
VRMP UVLO Hysteresis			870		mV
DRIVE SUPPLY					
PVCC Quiescent Current	EN = low		2		μA
ENABLE INPUT					
Enable High Input Leakage Current	Enable = 0	−1.0	0	1.0	μA
Upper Threshold		0.8			V
Lower Threshold				0.3	V
Enable Hysteresis			300		mV
Enable Delay Time	Measure time from Enable transitioning HI, to PGOOD high		200	500	μs
OSCILLATOR					
Switching Frequency Range	RDOSC = 2 kΩ ±1%	270	300	330	kHz
	RDOSC = 6 kΩ ±1%	360	400	440	
	RDOSC = 15 kΩ ±1%	540	600	660	
Switching Frequency Accuracy		−10		10	%
PGOOD OUTPUT					
Output Low Saturation Voltage	I_{PGOOD} = 4 mA			0.3	V
Rise Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%			150	ns
Fall Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%			150	ns
Output Voltage at Power−up	PGOOD pulled up to 5 V via 2 kΩ			1.2	V
Output Leakage Current When High	PGOOD = 5.0 V	−1.0		1.0	μA
Power Good Startup Delay	Measured from VCC > $VCC_{UVLO(rising)}$ to PGOOD rising, with EN = High		1.2	1.9	ms
2−Bit VID					
VID0, VID1 High Threshold Voltage		0.72			V
VID0, VID1 Low Threshold Voltage				0.34	V
VID0, VID1 Input Bias Current			1		nA
VID0, VID1 Pull Down Current			2.5		μA
VID Delay time		200			ns

Table 5. ELECTRICAL CHARACTERISTICS Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC}= 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
2−Bit VID					
VOUT	VID1 = 0, VID0 = 0		0.00		V
	VID1 = 0, VID0 = 1	1.07	1.10	1.13	V
	VID1 = 1, VID0 = 0	1.60	1.65	1.70	V
	VID1 = 1, VID0 = 1	1.75	1.80	1.85	V
VOUT Slew Rate	VID UP		24		mV/μs
	VID Down		24		
DIFFERENTIAL VOLTAGE SENSE AMPLIFIER					
Input Bias Current	VID0,1 = 0 V, VOUT = 0 V	−2		2	μA
VSP Input Voltage Range				2	V
VSN Input Voltage Range		−0.15		0.15	V
gm	VSP = 1.65 V, VSN = 0 V	1.29	1.6	1.95	mS
Open loop Gain	Load = 1 nF in series with 1 kΩ in parallel with 10 pF to ground		73		dB
−3 dB Bandwidth			15		MHz
Source Current	Input Differential −200 mV		280		μA
Sink Current	Input Differential 200 mV		280		μA
IOUT					
Analog Gain Accuracy	0 V < CSP − CSN < 0.1 V	−5		5	%
Gm		0.95	1.0	1.05	mS
IOUT Offset Current	0 V < VOUT < 2.5 V	−150		150	nA
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Absolute Overvoltage Threshold	VCSN − VGND	2.4	2.5	2.6	V
Over Voltage Delay	CSN rising to LG high		200		ns
Over Voltage PGOOD Delay	CSN rising to PGOOD low		400		ns
Under Voltage Threshold	VSP−GND falling	200	290	400	mV
Under Voltage Hysteresis	VSP−GND falling/rising		25		mV
Under Voltage Blanking Delay	VSP−GND falling to PGOOD falling		5		μs
DROOP					
Gm		0.94	1.0	1.04	mS
Offset Accuracy		−1.6		1.6	μA
Common mode rejection	CSP input at 1.1 V, 1.65 V and 1.8 V		60		dB
OVERCURRENT PROTECTION					
ILIM Threshold		1.275	1.3	1.325	V
ILIM Delay			280		ns
ILIM Gain	I_{ILIM}/(CSP−CSN) CSP−CSN = 20 mV		1.0		mS
CSP−CSN ZCD COMPARATOR					
Offset Accuracy		−1.75	−0.25	1.25	mV
HIGH−SIDE GATE DRIVE					
Pull−High Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V R_{DRV_HH}		1	2.5	Ω
Pull−Low Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V R_{DRV_HG}		0.8	2.0	Ω

Table 5. ELECTRICAL CHARACTERISTICS Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC}= 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
HIGH−SIDE GATE DRIVE					
HG Propagation Delay Time	From LG falling to HG rising T_{HG_d}	7	13	30	ns
HG Rise Time	THG_R	4		27	ns
HG Fall Time	THG_F		9	20	ns
HG Pulldown Resistance	$V_{BST} - V_{SW}$ = 0 V		300		kΩ
LOW−SIDE GATE DRIVE					
Pull−High Drive On Resistance	$PV_{CC} - V_{PGND}$ = 5 V R_{DRV_LH}		0.9	2.5	Ω
Pull−Low Drive On Resistance	$PV_{CC} - V_{PGND}$ = 5 V R_{DRV_LL}		0.6	1.25	Ω
LG Propagation Delay Time	From HG falling to LG rising T_{LG_d}	2	8	20	ns
LG Rise Time	TLG_R		18	27	ns
LG Fall Time	TLG_F		12	25	ns
SW to PGND RESISTANCE					
SW to PGND Pull−Down Resistance	R_{SW}		2		kΩ
BOOTSTRAP RECTIFIER SWITCH					
Output Low Resistance	EN=L or EN=H and LG=H R_{on_BST}	5	13	21	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by design, not tested in production.

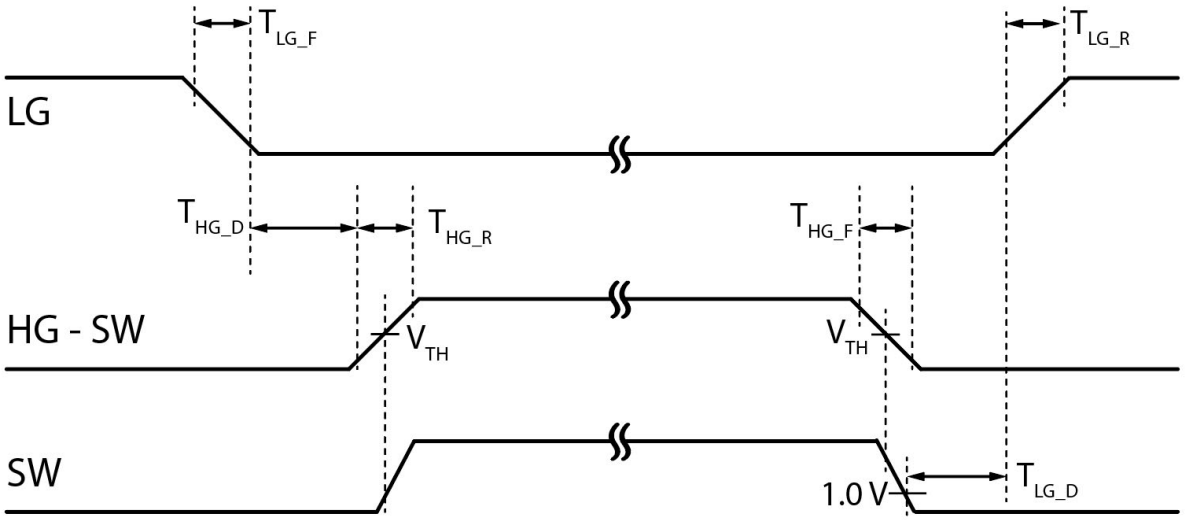


Figure 3. Driver Timing Diagram

NOTE: Timing is referenced to the 90% and the 10% points, unless otherwise stated.

General

The NCP81561 is a single phase controller with a built in gate driver. The controller makes use of a digitally enhanced high performance current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions. At light load the NCP81561 automatically transitions into DCM operation to save power.

Switching Frequency Programming

A fixed precision oscillator is provided. The actual switching frequency is set at 300 kHz, 400 kHz or 600 kHz by the resistor on the DOSC pin. The resistor and frequency can be referred to in the table below.

DOSC Resistor	2 kΩ	6 kΩ	15 kΩ
Switching Frequency	300 kHz	400 kHz	600 kHz

After the NCP81561 is enabled, but before the soft−start ramp up, the oscillator frequency is detected on the DOSC pin. A current is sourced out of the DOSC pin, and at the end of the detection time, the voltage on the DOSC pin is measured and use to set the switching frequency.

Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks describe in the Droop Compensation and DAC Feedforward Compensation sections. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm \cdot \left[V_{DAC} - \left(V_{VSP} - V_{VSN}\right)\right] \quad \text{(eq. 1)}$$

This current is applied to a standard Type II compensation network.

VR Voltage Compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF.

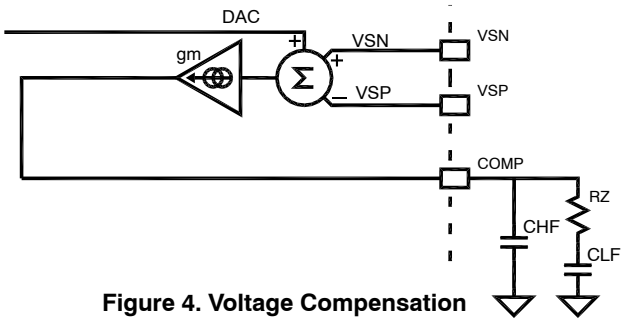


Figure 4. Voltage Compensation

Differential Current Feedback Amplifier

The NCP81561 controller has a low offset, differential amplifier to sense output inductor current. An external low pass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The low pass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_Z = \frac{DCR@25^\circ C}{2 \cdot \pi \cdot L} \quad \text{(eq. 2)}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{PH} \cdot \left(Rth + R_{CS}\right)}{R_{PH} + Rth + R_{CS}}\right) \cdot C_{CS}}$$

Forming the low pass filter with an NTC thermistor (Rth) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of R_{PH} and R_{CS} are set based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the low pass filter resistance not exceed 10 kΩ in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 mΩ for sufficient current accuracy. Recommended values for the external filter components are:

$$C_{CS} = \frac{L}{\frac{R_{PH} \cdot \left(Rth + R_{CS}\right)}{R_{PH} + Rth + R_{CS}} \cdot DCR} \quad \text{(eq. 3)}$$

For an NTC with an Rth of 100 kΩ at 25°C and a typical Beta of 4300, an R_{PH} = 7.68 kΩ and an R_{CS} = 13.8 kΩ provide the optimum DCR compensation in the temperature range of 0°C to 75°C.

Using 2 parallel capacitors in the low pass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{Rth + R_{CS}}{R_{PH} + Rth + R_{CS}} \cdot Iout \cdot DCR \quad \text{(eq. 4)}$$

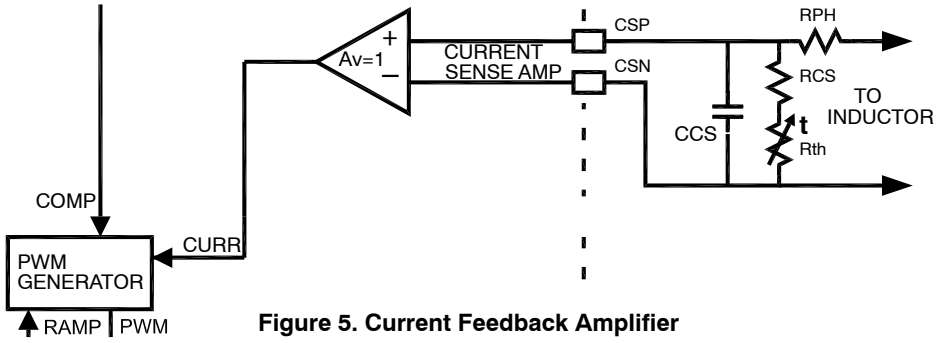


Figure 5. Current Feedback Amplifier

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

2−Bit VID Interface

Intel® proprietary. Contact Intel Corporation for details on 2−Bit VID interface.

Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP}, proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81561, a loadline is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.

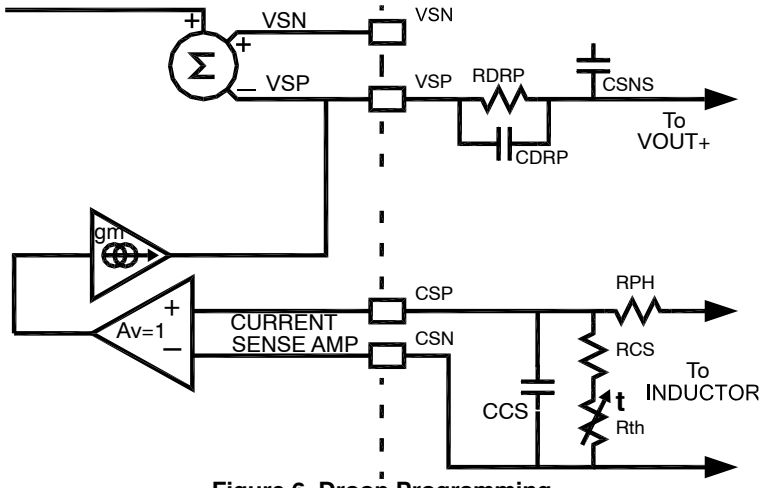


Figure 6. Droop Programming

$$V_{DROOP} = R_{DRP} \cdot gm \cdot \frac{Rth + R_{CS}}{R_{PH} + Rth + R_{CS}} \cdot I_{OUT} \cdot DCR \quad \text{(eq. 5)}$$

The loadline is programmed by choosing R_{DRP} such that the ratio of voltage produced across R_{DRP} to output current is equal to the desired loadline.

$$R_{DRP} = \frac{Loadline}{gm \cdot DCR} \cdot \frac{R_{PH} + Rth + R_{CS}}{Rth + R_{CS}} \quad \text{(eq. 6)}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIM sink current. The voltage on the IOUT pin should be scaled with an external resistor to ground.

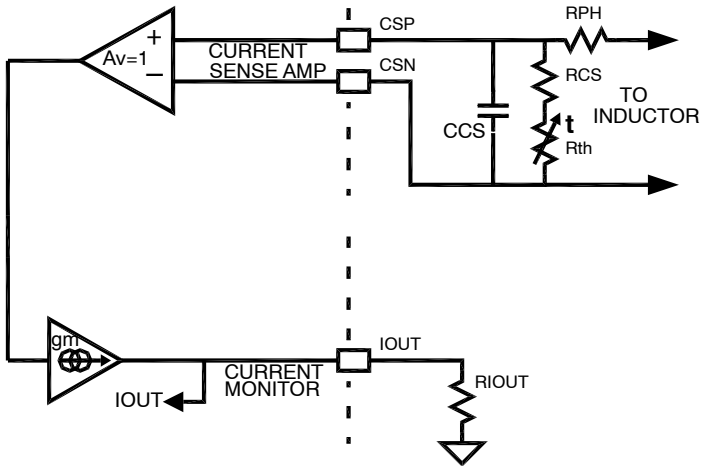


Figure 7. V_{IOUT} Programming

$$R_{IOUT} = \frac{2.5\ V}{gm \cdot \frac{Rth + R_{CS}}{R_{PH} + Rth + R_{CS}} \cdot IccMax \cdot DCR} \quad \text{(eq. 7)}$$

Programming the DAC Feed-Forward Filter

The NCP81561 outputs a pulse of current from the VSN pin upon each increment of the internal DAC when the 2−bit VID is programmed to a higher voltage. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during a VID change to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. RFF sets the gain of the DAC feed-forward and CFF provides the time constant to cancel the time constant of the system per the following equations. C_{OUT} is the total output capacitance of the system.

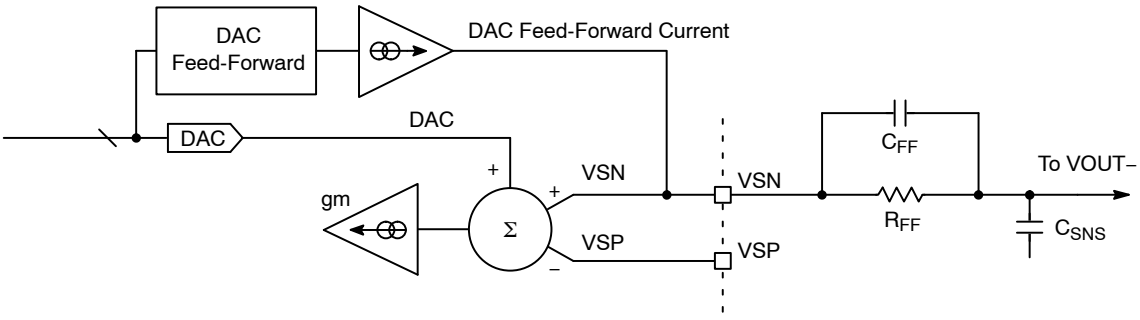


Figure 8. DAC Feed−Forward

$$R_{FF} = \frac{Loadline \cdot C_{OUT}}{1.35 \cdot 10^{-9}}\ (\Omega) \qquad C_{FF} = \frac{200}{R_{FF}}\ (nF) \quad \text{(eq. 8)}$$

Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIM}) from the ILIM pin to ground. The current limit latches the single−phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the current limit resistor based on the equation shown below. A capacitor can be placed in parallel with the programming resistor to slightly delay activation of the latch if some tolerance of short overcurrent events is desired.

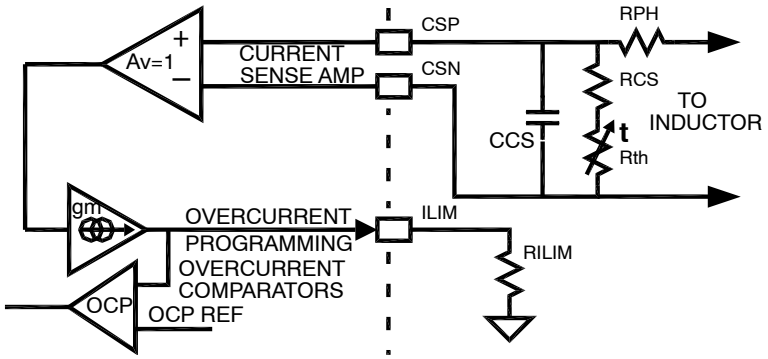


Figure 9. ILIM Programming

$$R_{ILIM} = \frac{1.3\ V}{gm \cdot \frac{Rth + R_{CS}}{R_{PH} + Rth + R_{CS}} \cdot Iout_{Limit} \cdot DCR} \quad \text{(eq. 9)}$$

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

Input Under−Voltage Protection

The controller is protected against under−voltage on the VCC and VRMP pins.

Under Voltage Protection

Under voltage protection will shut off the output similar to OCP to protect against short circuits. The threshold is specified in the parametric spec tables and is not adjustable.

Over Voltage Protection (OVP)

The NCP81561 has an absolute OVP feature which generates an OVP fault when the voltage on the CSN pin (VCSN) pin exceeds 2.5 V.

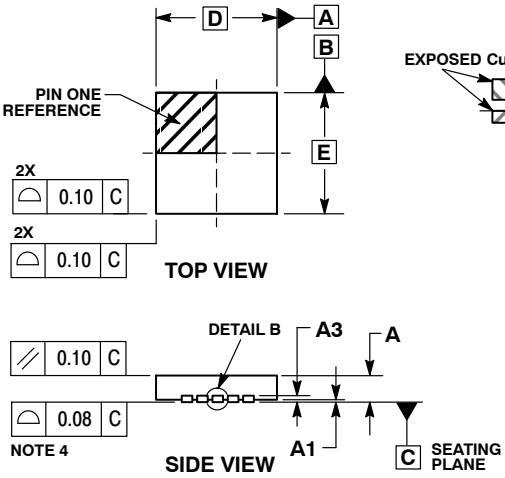
When an OVP fault occurs, the HG driver is turned off and the LG driver is turned on to discharge the output. The internal output voltage control DAC also begins to ramp down at a rate of 1.6 mv/μs. The LG driver turns off when VCSN drops below the dac voltage and continues to pulse on so that VOUT tracks the internal DAC voltage down to 0 V. To exit an OVP fault condition, the EN pin must be toggled low or the controller must be power cycled. OVP is disabled during VID changes and when VOUT = 0 V.

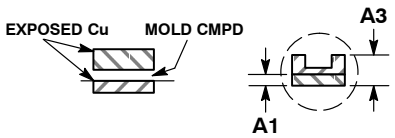
Over Current Protection (OCP)

The current limit is set with a resistor between the ILIM pin and ground. The voltage on this pin is compared to the ILIM threshold voltage (V_{CL}). If the voltage at the ILIM pin exceeds the threshold voltage, the controller shuts down immediately. To recover from an OCP fault, the EN pin or V_{CC} voltage must be cycled low. A 10 nf filter capacitor must be added between the ILIM pin and GND (in parallel with the ILIM resistor), to reduce the chance of spurious overcurrent trips.

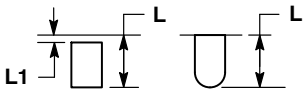
PACKAGE DIMENSIONS

QFN20 4x4, 0.5P
CASE 485EE
ISSUE A



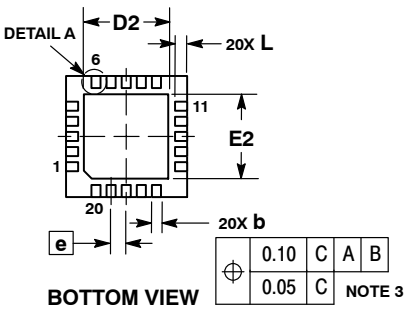


DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

SIDE VIEW

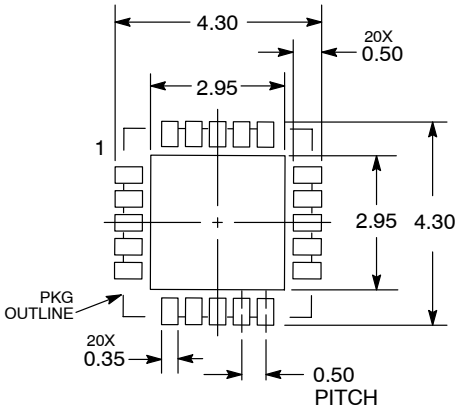


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	2.75	2.85
E	4.00 BSC	
E2	2.75	2.85
e	0.50 BSC	
L	0.25	0.35
L1	0.00	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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