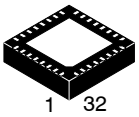
Hot Swap, Slave-Only Smart Fuse

18 V, 0.65 mΩ, 50 A, LQFN32

Product Preview

NCP81418



LQFN32 5x5, 0.5P
CASE 487AA

General Description

The NCP81418 is a slave−only, 50 A, electronically resettable, in−line fuse used in server−based, high current 12 V hot−swap applications, where NCP81428 serves as the Master. The NCP81418 consists of a very low 0.65 mΩ NMOS FET, a high performance Hot−Swap Controller, all co−packaged into a LQFN32 package. The low RDSon MOSFET ensures minimal conduction losses and the leadframe around the FET efficiently couples heat away.

Power Features

- Up to 80 A Peak Output Current, 50 A Continuous
- VIN Operating Range: 5 to 18 V
- Up to 30 V Standby (PowerFet Off) Operation
- 0.65 mΩ Path Resistance

Control Features

- Programmable OCP via NCP81428 Master
- Programmable Soft−start with External Capacitor
- Soft Start Current Balancing between Parallel Units

Other Features

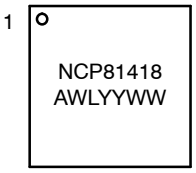
- Co−packaged Power Switch, Hotswap Controller
- TWI (Two Wire Interface) Communication between Master and Slave
- ±2% IMON Accuracy at 30 A and Higher
- Parallel Operation for High Current Applications
- Excellent Current Balancing in Parallel Operations
- Over−temperature Shutdown
- FAULT#_C & FAULT#_D Multi−purpose Pins
- Soft−start Current Limiting for SOA Protection
- Excessive Soft−start Duration Protection
- 5 mm x 5 mm LQFN32 Package
- Operating Temperature: −40°C to +125°C

Applications

- Servers
- Data Storage
- Base Stations
- Industrial Applications

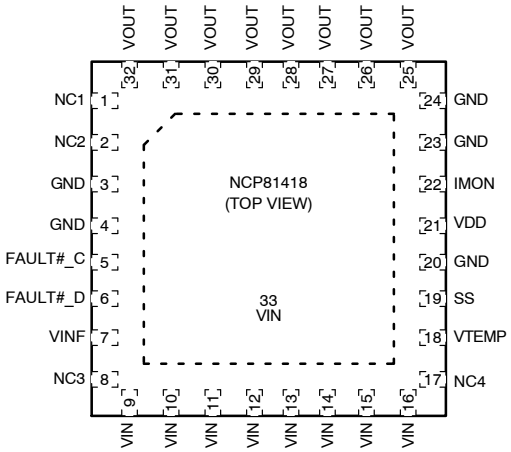
This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



NCP81418 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

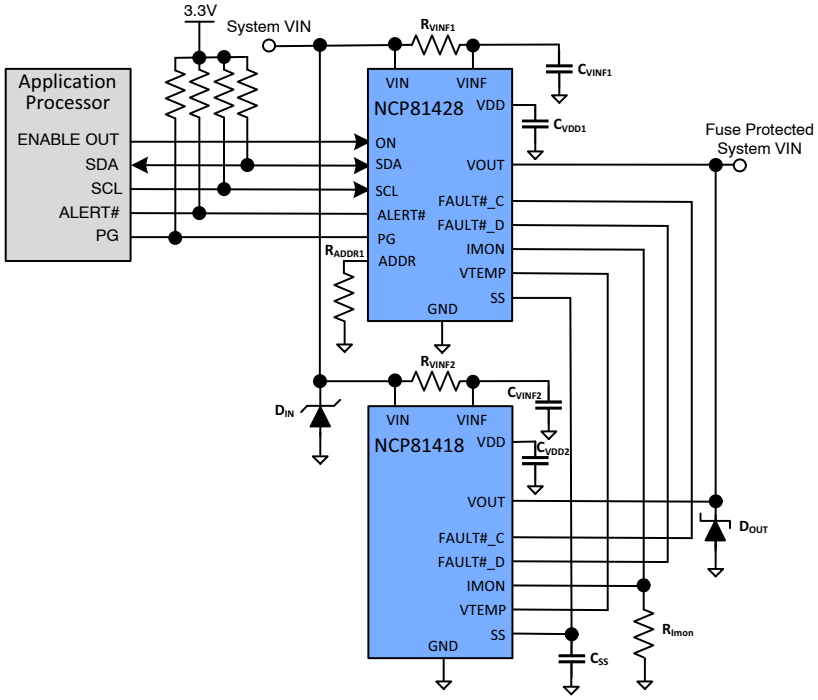


Figure 1. Application Diagram

Pin Connections

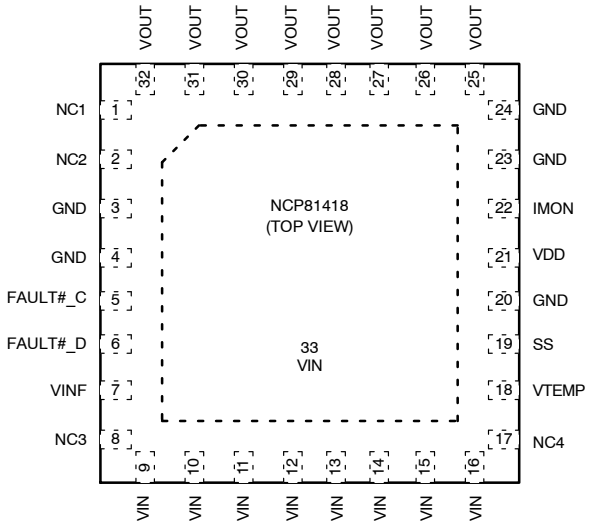


Figure 2. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	NC1	This pin is a no−connect within the device.
2	NC2	This pin is a no−connect within the device.
3	GND	Ground
4	GND	Ground
5	FAULT#_C	Active low Fault communication pin in parallel application between master and slave devices. Connect FAULT#_C pins together in parallel applications. This pin is an output on the master and an input on the slave.
6	FAULT#_D	Active low Fault communication pin in parallel application between master and slave devices. Connect FAULT#_D pins together in parallel application.
7	VINF	Control circuit power supply input. Connect to VIN pins through an RC filter.
8	NC3	Do not connect to this pin. Leave floating.
9	VIN09	Input of high current output switch (MOSFET drain connection).
10	VIN10	Input of high current output switch (MOSFET drain connection).
11	VIN11	Input of high current output switch (MOSFET drain connection).
12	VIN12	Input of high current output switch (MOSFET drain connection).
13	VIN13	Input of high current output switch (MOSFET drain connection).
14	VIN14	Input of high current output switch (MOSFET drain connection).
15	VIN15	Input of high current output switch (MOSFET drain connection).
16	VIN16	Input of high current output switch (MOSFET drain connection).
17	NC4	Do not connect to this pin. Leave floating.
18	VTEMP	Analog temperature monitoring. Connect all VTEMP pins together in parallel applications.
19	SS	Soft−start time programming pin. Connect a capacitor to this pin to set the soft−start time. The internal circuit controls the slew rate of the output voltage at turn−on. Connect all SS pins together in parallel applications.
20	GND	Ground
21	VDD	Internal linear regulated supply output. Place a capacitor with a value of 4.7 μF or greater on this pin to maintain accuracy.
22	IMON	Analog current monitor output, Connect a 2 kΩ resistor between pin and ground. A proportional current to the output current develops a voltage across the resistor. Connect all IMON pins together in parallel applications.
23	GND	Ground
24	GND	Ground
25	VOUT25	Output of high current output switch (MOSFET source connection).
26	VOUT26	Output of high current output switch (MOSFET source connection).
27	VOUT27	Output of high current output switch (MOSFET source connection).
28	VOUT28	Output of high current output switch (MOSFET source connection).
29	VOUT29	Output of high current output switch (MOSFET source connection).
30	VOUT30	Output of high current output switch (MOSFET source connection).
31	VOUT31	Output of high current output switch (MOSFET source connection).
32	VOUT32	Output of high current output switch (MOSFET source connection).
33	VIN33	Input of high current output switch (MOSFET drain connection).

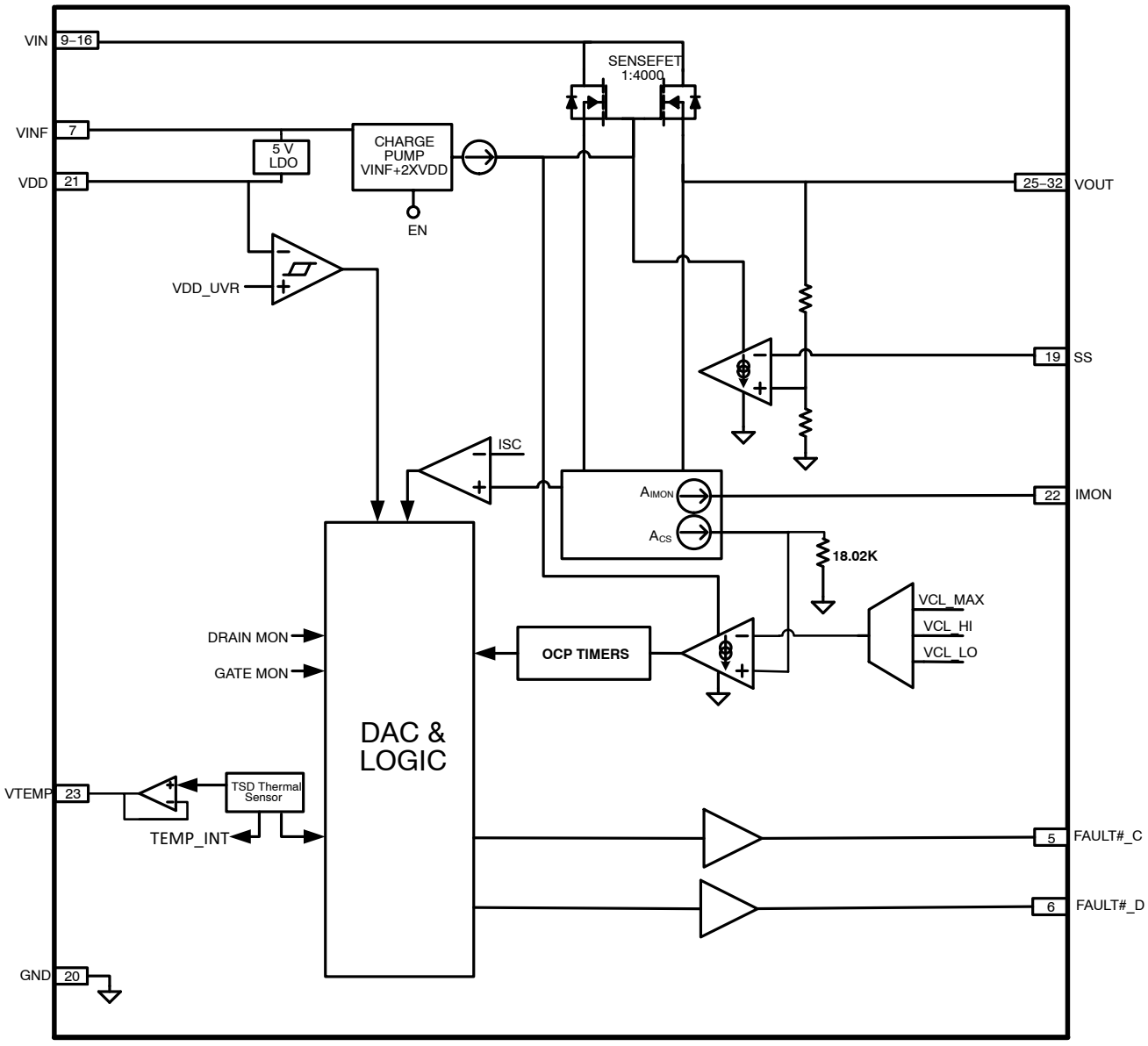


Figure 3. Block Diagram

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VINx, VINF	Input Voltage (Notes 1, 3)		−0.3	–	20.0	V
	Input Voltage (Notes 1, 2)		−0.3	–	30	
VOUTx	VOUT Pin Voltage Range (Note 1)		−0.3, −1.0 V (<500 ms)	–	20	V
VDD	LDO Output (Note 1)		−0.3	–	6.0	V
All Other Pins	Pin Voltage Range (Note 4)		−0.3	–	VDD + 0.3	V
$T_{J(MAX)}$	Operating Junction Temperature		–	–	+150	°C
T_{STG}	Storage Temperature Range		−55	–	+150	°C
T_{SLD}	Lead Temperature Soldering Reflow (SMD Styles Only) Pb−Free Versions (Note 5)		–	–	+260	°C
ESD_{CDM}	Electrostatic Discharge − Charged Device Model	Charged Device Model	–	–	2.0	kV
ESD_{HBM}	Electrostatic Discharge − Human Body Model	Human Body Model	–	–	3.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to ground unless noted otherwise.
2. Vout disabled is when the internal Power FET has turned off by disabling the device or after triggering a fault event.
3. Vout enabled is when the internal Power FET has turned on either by enabling the device or after restart fault event.
4. The ratings of Pins referenced to VDD, only apply when VDD is within the recommended Voltage Range.
5. For information, please refer to **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction−to−Ambient Thermal Resistance (Note 6)		–	30	–	°C/W
$R_{\theta JCT}$	Junction−to−Top−Case Thermal Resistance		–	50	–	°C/W
$R_{\theta JCB}$	Junction−to−Bottom−Case Thermal Resistance		–	1.5	–	°C/W
$R_{\theta JB}$	Junction−to−Board Thermal Resistance (Note 7)		–	1.5	–	°C/W
$R_{\theta JAC}$	Junction−to−Case Thermal Resistance (Note 8)		–	1.5	–	°C/W

6. Theta JA is obtained by simulating the device mounted on a 500 mm^2, 1−oz Cu pad on a 80 mm x 80 mm, 1.6 mm 8 layer FR4 board.
7. Theta JB value based on hottest board temperature within 1 mm of the package.
8. Theta JC ~ = Theta JCT // Theta JCB (Two−Resistor Compact Thermal Model, JESD15−3).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	VIN, VINF Pin Voltage Range		5	–	18	V
I_{AVE}	Minimum Continuous Output Current		–	–	50	A
I_{PEAK}	Peak Output Current		–	–	80	A
C_{VDD}	VDD Output Load Capacitance Range		4.7	–	10	μF
C_{OUT}	Output Capacitance Range		100	–	10000	μF
T_{SS}	Soft Start Duration		10	–	110	ms
R_{IMON}	IMON Resistor		1.98	2	2.02	kΩ
$T_{J(OP)}$	Junction Temperature		−40	–	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Typical values are at T_J = 25°C, VIN = VINF = 12.0 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 100 nF. Min/Max values are valid for 6 V ≤ VIN ≤ 18 V, −40°C ≤ T_J ≤ +125°C, unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VINF INPUT						
I_{q_OP}	Operating Current	Device Enabled, No Load	–	9.5	14	mA
VDD REGULATOR						
V_{DD_NL}	VDD Output Voltage	1 mA < I_{VINF} < 10 mA, 6 V < V_{INF} < 18 V	4.7	5.0	5.3	V
V_{DD_UVR}	UVLO Threshold – Rising		4.1	4.3	4.5	V
V_{DD_UVF}	UVLO Threshold – Falling		3.5	3.7	3.9	V
I_{DD_CL}	VDD Current Limit	6 V < V_{INF} < 18 V, V_{DD} – 100 mV	20	25	50	mA
I_{DD_FLD}	VDD Short Circuit Current Limit	6 V < V_{INF} < 18 V, V_{DD} = 0 V	5	13	25	mA
SS PIN						
AV_{SS}	DC Gain at VOUT	V_{SS} = 1.0 V	9.7	10	10.3	V/V
V_{OL_SS}	SS PullDown Voltage	0.1 mA into pin during ON delay	–	3.5	7.5	mV
IMON OUTPUT						
TOL_{IMON}	Accuracy (Single eFuse)	IOUT = 8 A, VIN = 12 V, T_J = 25°C	−4	–	+4	%
		IOUT = 15 A (Note 9), VIN = 12 V, T_J = 25°C	−2.5	–	+2.5	
		IOUT = 30 A (Note 9), VIN = 12 V, T_J = 25°C	−2	–	+2	
		IOUT = 50 A (Note 9), VIN = 12 V, T_J = 25°C	−2	–	+2	
V_{IMON_CLMP}	IMON Current Source Clamp Voltage	Max pullup voltage of current source	2.4	3.0	–	V
CURRENT LIMIT at SOFTSTART						
VIN < 13.2 V						
I_{CS_LO}	Current Limit Clamp Voltage, Low VIN (Note 9)	V_{OUT} < 0.4 x V_{IN}, V_{IN} < 13.2 V	6	7.5	9	A
I_{CS_HI}	Current Limit Clamp Voltage, Low VIN (Note 9)	0.4 x V_{IN} < V_{OUT} < 0.8 x V_{IN}, V_{IN} < 13.2 V	12	15	18	
I_{CS_MAX}	Current Limit Max Clamp Voltage, Low VIN (Note 9)	0.8 x V_{IN} < V_{OUT}, Vt < V_{GS}, V_{IN} < 13.2 V	24	30	36	A
t_{CL_REG}	CL Duration before SD (Note 9)		200	250	300	μs
VIN > 13.2 V						
I_{CS_LO}	Current Limit Clamp Voltage, High VIN (Note 9)	V_{OUT} < 0.4 x V_{IN}, V_{IN} > 13.2 V	4	5	6	A
I_{CS_HI}	Current Limit Clamp Voltage, High VIN (Note 9)	0.4 x V_{IN} < V_{OUT} < 0.8 x V_{IN}, V_{IN} > 13.2 V	8	10	12	
I_{CS_MAX}	Current Limit Max Clamp Voltage, High VIN (Note 9)	0.8 x V_{IN} < V_{OUT}, Vt < V_{GS}, V_{IN} > 13.2 V	16	20	24	A
t_{CL_REG}	CL Duration before SD (Note 9)		200	250	300	μs
OCP PROTECTION						
OCP Threshold						
I_{OCP}	Over Current Detection Range	VIN = 12 V, OCP1 = 10 A (Note 9)	10	–	80	A
I_{OCP_HYS}	Over Current Hysteresis – Percentage of Threshold		–	80	–	%
$OCP_{Accuracy}$	Over Current Detection Accuracy	VIN = 12 V, OCPx = 10 A	−10	–	+12	%
		VIN = 12 V, OCPx = 15 to 80 A	−10	–	+10	

ELECTRICAL CHARACTERISTICS (Typical values are at T_J = 25°C, VIN = VINF = 12.0 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 100 nF. Min/Max values are valid for 6 V ≤ VIN ≤ 18 V, −40°C ≤ T_J ≤ +125°C, unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OCP PROTECTION						
Timeout Delay						
OCP_{Timer}	Over Current Debounce Timer Range		0.25	–	50	ms
$OCP_{Accuracy}$	Over Current Debounce Timer Accuracy		−10	–	+10	%
$OCP_{Reset-Timer}$	Over Current Debounce Timer Reset		90	100	110	μs
SHORT CIRCUIT PROTECTION						
I_{SC}	Short Circuit Current Threshold (Note 9)		135	150	165	A
t_{SC}	Response Time (Note 9)	From $I_{OUT} > I_{LIMSC}$ until gate pulldown	–	–	2000	ns
THERMAL PROTECTION						
T_{OT_F}	Programmable Threshold Range		120.5	–	150	°C
	Resolution		–	0.5	–	
	Default Over−Temperature Value		–	140	–	
OUTPUT SWITCH (FET)						
R_{DS_ON}	Rdson Resistance	V_{IN} = 6 V to 18 V, I_{LOAD} = 8 A	–	0.65	1.3	mΩ
I_{ds_OFF}	Off−state leakage current	V_{IN} = 18 V, Device Disabled, T_J = 25°C	–	–	1	μA
FAULT DETECTION						
VG_TH	V_G Low Threshold	Latch/Restart if $V_{GS} < V_{G\_TH}$ after t_{SS_FLT}, V_{IN} = 12 V	5.2	5.5	5.8	V
VDG_TH	V_{GD} Short Threshold	Startup postpones if $V_G > V_{DG\_TH}$ when device is enabled, V_{IN} = 12 V	2.5	3.0	3.6	V
VDG_OK	V_{GD} Short OK Threshold	Startup resumes if $V_G < V_{DG\_OK}$, V_{IN} = 12 V	2.1	2.6	3.2	V
t_{SS_FLT}	Startup Timer Failsafe (Note 9)	V_{IN} = 12 V	180	200	220	ms
VTEMP						
$V_{VTEMP25}$	VTEMP Pin Voltage at 25°C	T_J = 25°C	410	420	430	mV
A_{VTEMP}	VTEMP Pin Gain per °C	25°C ≤ T_J ≤ 150°C	7.0	7.8	8.6	mV/°C
FAULT#_C, FAULT#_D PINS						
V_{FLT_IL}	FAULT#_X Active Low Input		–	–	0.4	V
V_{FLT_IH}	FAULT#_X Active High Input		3.2	–	–	V
R_{FLT_Rup}	Pull−up resistance on FAULT#_x		300	450	700	Ω
R_{FLT_Rdwn}	Pull−down resistance on FAULT#_x		5	10	15	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design or characterization data. Not tested in production.

TYPICAL CHARACTERISTICS

(V_{IN} = V_{INF} = 12 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 220 nF, C_{OUT} = 100 μF, T_A = 25°C, unless otherwise specified)

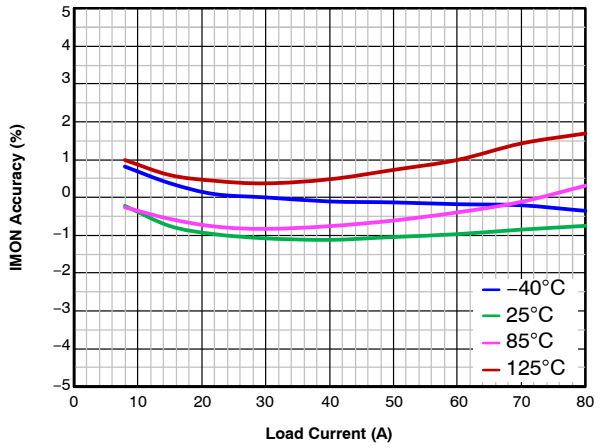


Figure 4. IMON Accuracy vs. Load Current and Temperature

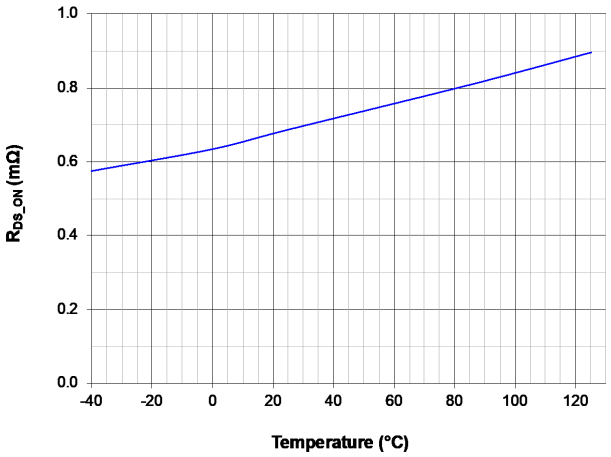


Figure 5. Switch RDS_ON @ 8 A vs. Temperature

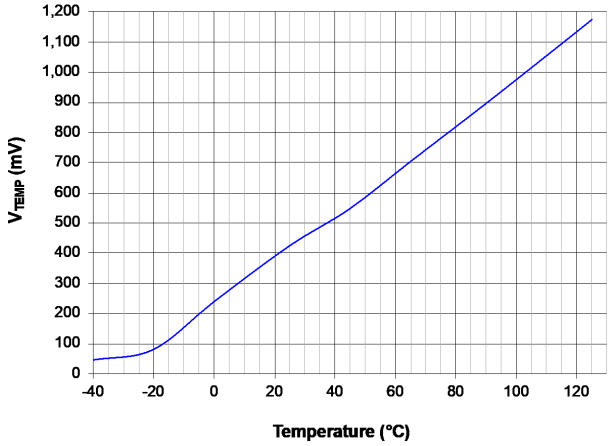


Figure 6. VTEMP vs. Temperature

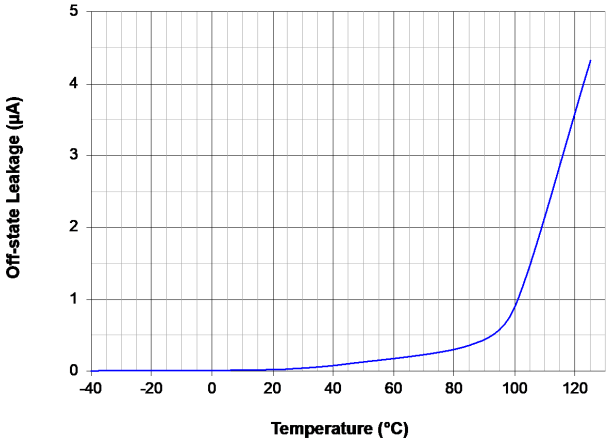


Figure 7. Switch Off−State Leakage vs. Temperature

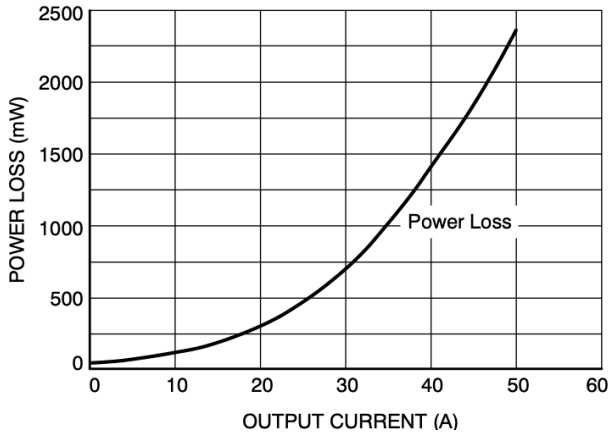


Figure 8. Power Loss vs. Current

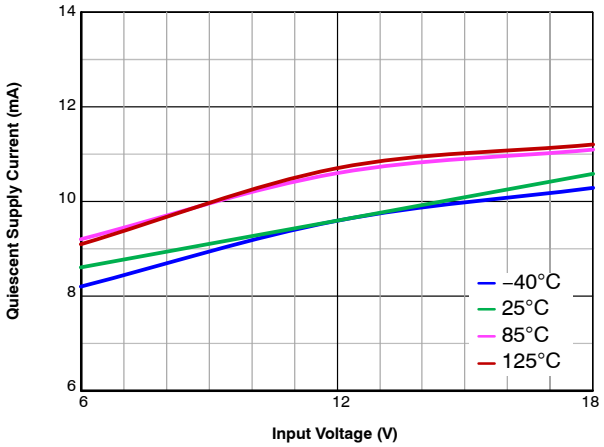


Figure 9. Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS

(V_{IN} = V_{INF} = 12 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 220 nF, C_{OUT} = 100 μF, T_A = 25°C, unless otherwise specified)

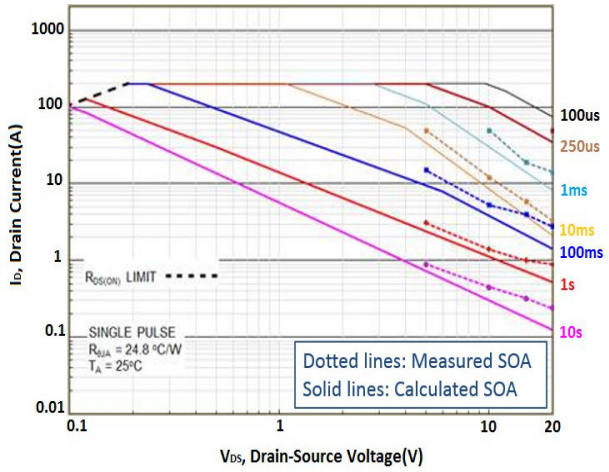


Figure 10. Power FETs Safe Operating Area

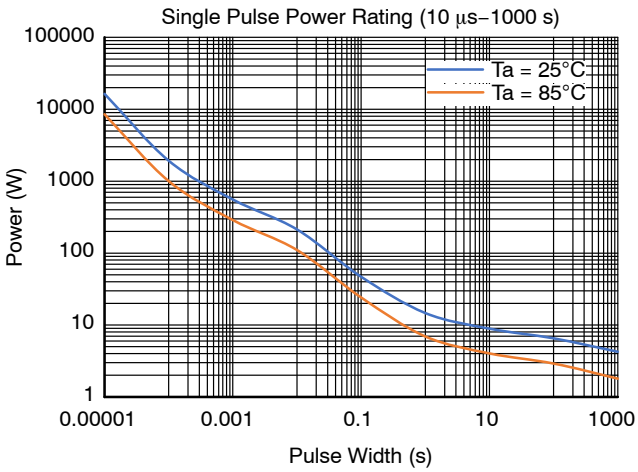


Figure 11. Single Pulse Power Rating (10 μs to 1000 s, Junction to Ambient, Note 6)

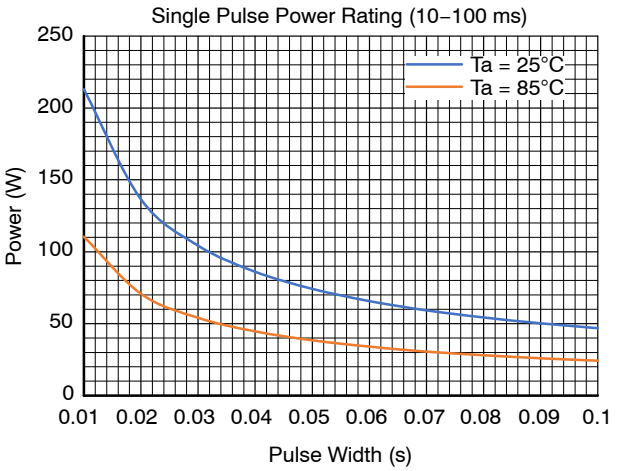


Figure 12. Single Pulse Power Rating (10 ms to 100 ms, Junction to Ambient, Note 6)

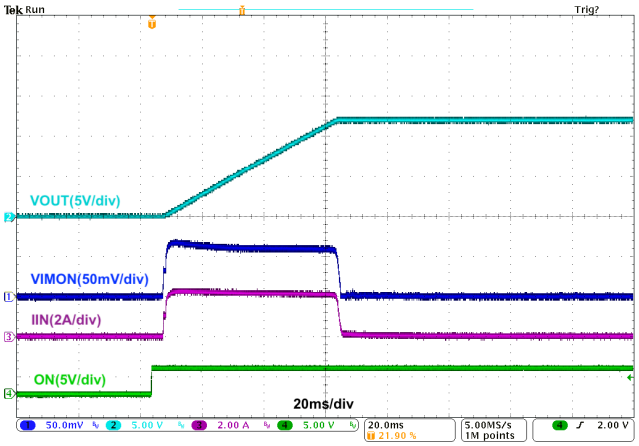


Figure 13. Start−up by ON, IOUT = 0 A, COUT = 10 mF

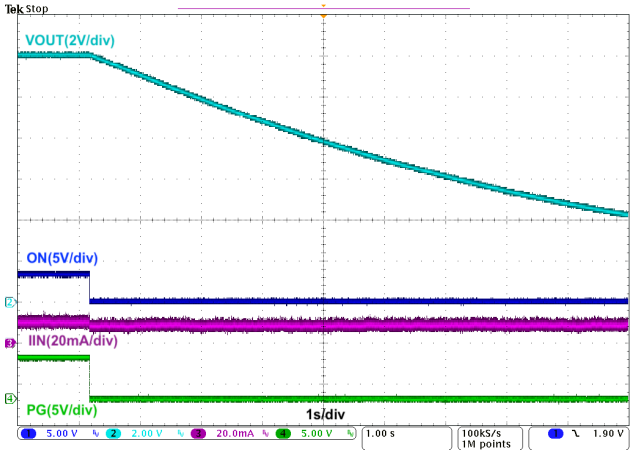


Figure 14. Shutdown by ON, IOUT = 0 A, COUT = 10 mF, Output Pulldown Enabled

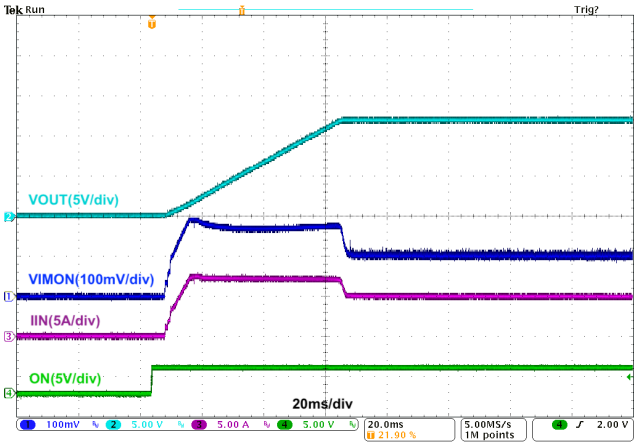


Figure 15. Start−up by ON, IOUT = 5 A, COUT = 10 mF

TYPICAL CHARACTERISTICS (CONTINUED)

(VIN = VINF = 12 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 220 nF, C_{OUT} = 100 μF, T_A = 25°C, UNLESS OTHERWISE SPECIFIED)

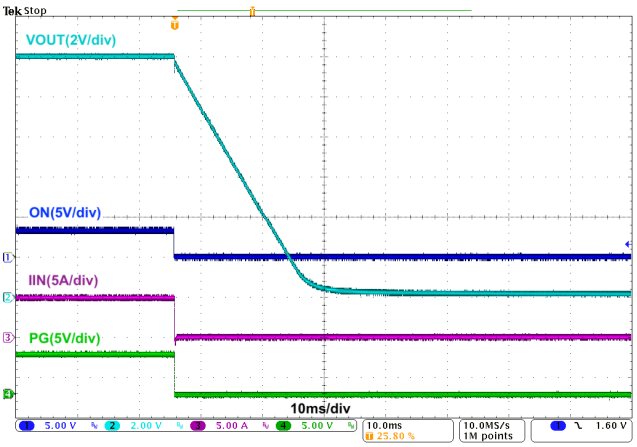


Figure 16. Shutdown by ON, IOUT = 5 A, COUT = 10 mF

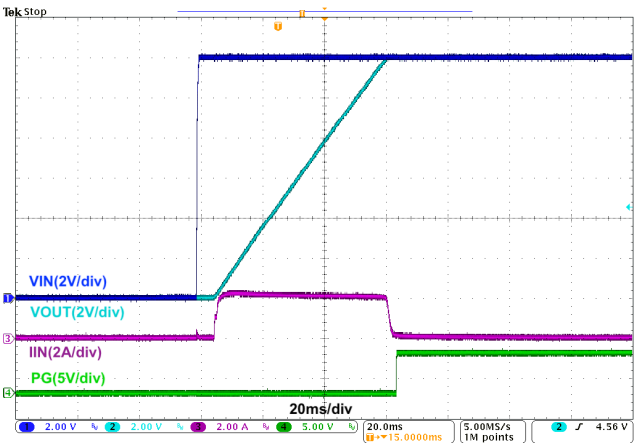


Figure 17. Start−up by VIN, IOUT = 0 A, COUT = 10 mF

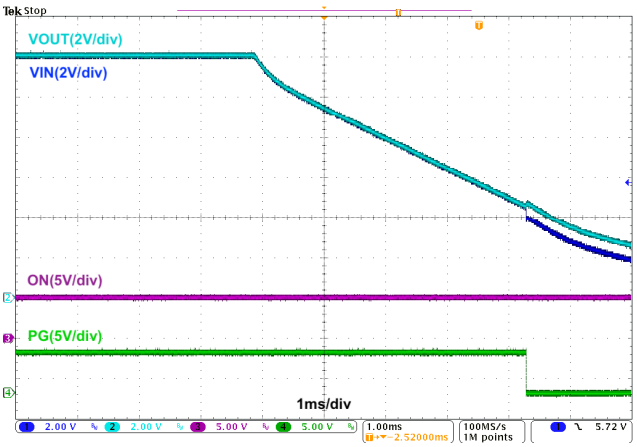


Figure 18. Shut−down by VIN, IOUT = 0 A, COUT = 10 mF

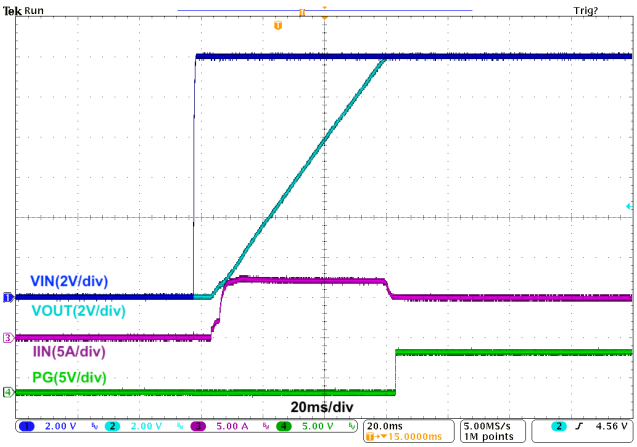


Figure 19. Start−up by VIN, IOUT = 5 A, COUT = 10 mF

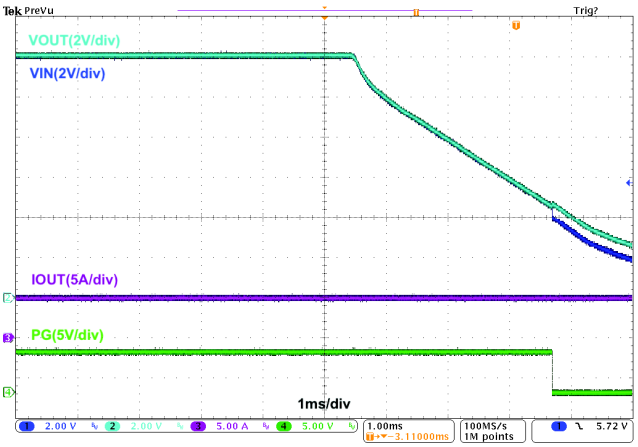


Figure 20. Shut−down by VIN, IOUT = 5 A, COUT = 10 mF

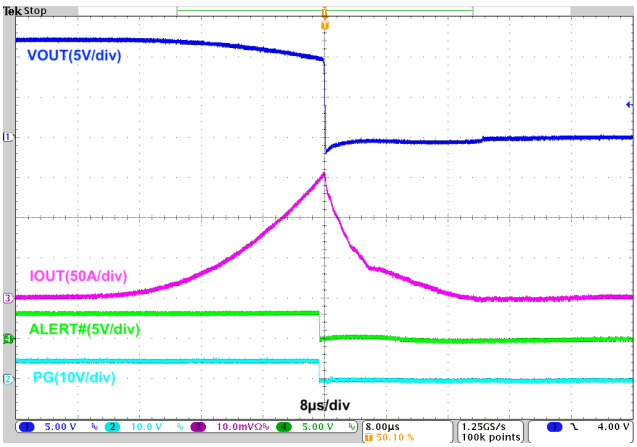


Figure 21. Short Circuit During Normal Operation, Initial IOUT = 0 A

TYPICAL CHARACTERISTICS (CONTINUED)

(VIN = VINF = 12 V, C_{VINF} = 0.1 μF, C_{VDD} = 4.7 μF, C_{SS} = 220 nF, C_{OUT} = 100 μF, T_A = 25°C, UNLESS OTHERWISE SPECIFIED)

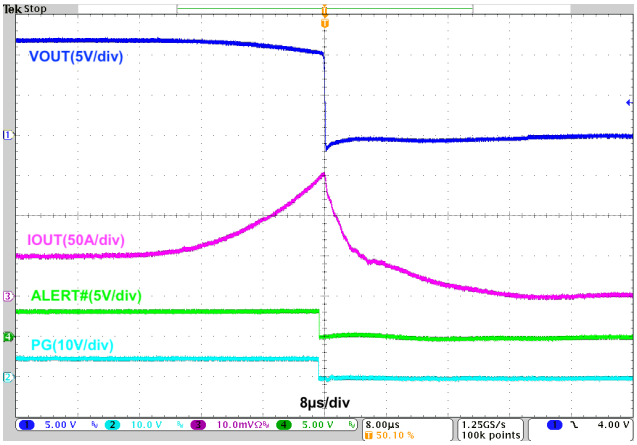


Figure 22. Short Circuit During Normal Operation, Initial IOUT = 50 A

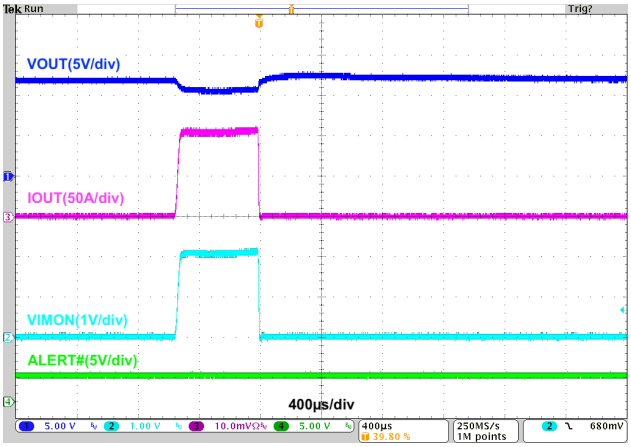


Figure 23. Over Current Protection During Normal Operation, OCP3 Level = 80 A, OCP3 Debounce Timer =1 ms, Load Pulse Width = 500 μs

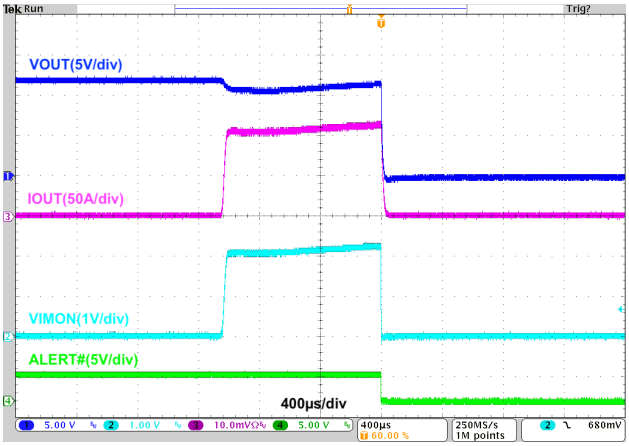


Figure 24. Over Current Protection During Normal Operation, OCP3 Level = 80 A, OCP3 Debounce Timer = 1 ms, Load Pulse Width = 1.5 ms

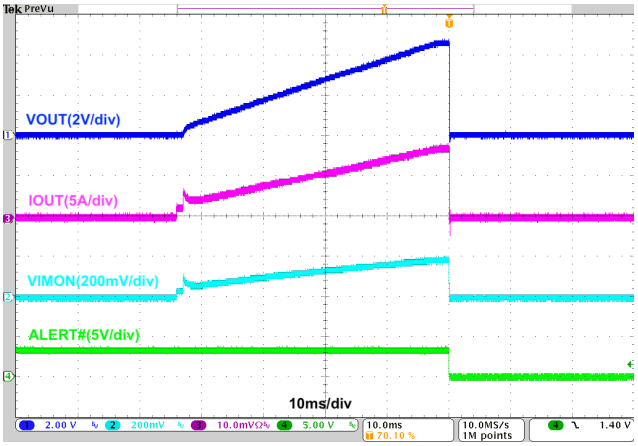


Figure 25. Over Current Protection During Softstart

TERMS AND DEFINITIONS

Definitions

The NCP81418 uses “Host”, “Master” and “Slave” terminology when referring to the operation of the NCP81418’s function in the application:

- A Host is the device which controls the PMBus®
- A Master is a device that is a Slave to the Host, controls the Slaves’ On/Off Operation and/or the Two Wire Interface (TWI) via FAULT#_C and FAULT#_D.
- A device referred to as a Slave is controlled by the Master for enablement, TWI communication and fault reporting.

Please refer to the Master/Slave Configuration and the TWI sections for further information.

General Information

The NCP81418 is a slave−only, electronically re−settable eFuse for use in server−based, high current 12 V hot−swap applications. The NCP81418 consists of a very low RDSon NMOS pass device for minimal power dissipation and in using a copper clip leadframe improves heat transfer away from the power FET.

The device has two pins dedicated (Fault#_C and Fault#_D) for controlled start−up and shutdown between the device and the Master.

Initialization

The diagram below is the State Machine for the operation.

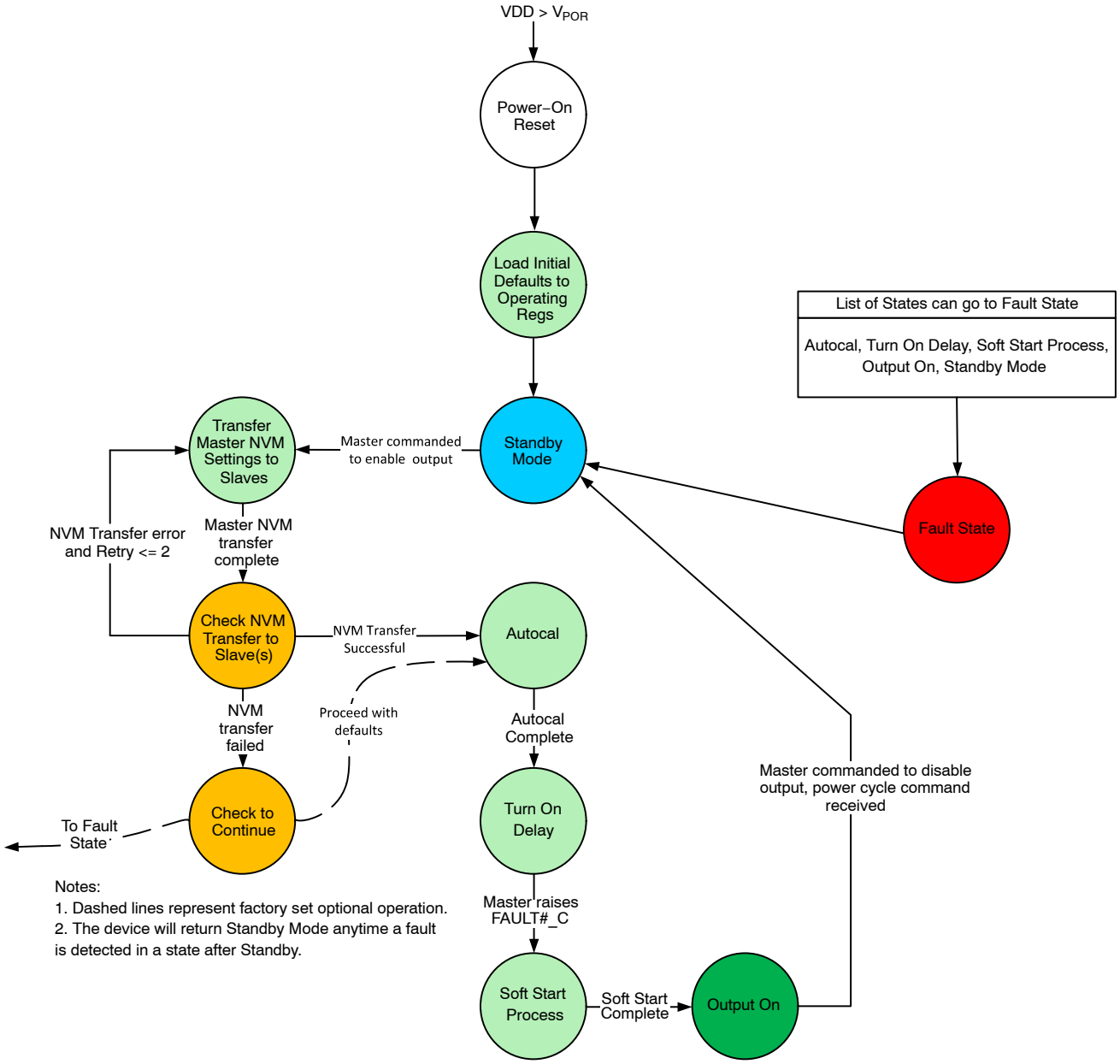


Figure 26. Master/Slave State Diagram

State Machine Simplified Breakdown

Upon applying power to the device as the LDO output crosses the VDD UVLO threshold, the default values are transferred to the operating registers. Once the default values are loaded into the operating registers, the device proceeds to standby mode.

In standby mode, when the Master is enabled, FAULT#_C and FAULT#_D become CLK and SDA outputs from the Master and inputs to NCP81418 only during data transfer. Once data is transferred, the NCP81418 Slave devices regain control over the FAULT#_D pin and notify the Master if there is data mismatch by asserting FAULT#_D low. In the event there is an error in the data transfer, the master will attempt to transfer the data 3 times. If after three failures to transfer, there is a factory setting to either proceed with the default values or shutdown. Once in auto_cal, a t_{ON} Delay is built into the process to ensure the devices are ready before the Master simultaneously enables soft−start in itself and NCP81418's by asserting FAULT#_C High. Note that there are three 8us consecutive FAULT#_ C pulses that occur during the initial soft−start stage for gate pre−charge and synchronization between Master and NCP81418's to ensure a current balanced soft−start.

With the exception of during data transfer, in all modes starting at standby, FAULT#_C is used for the Master to enable all devices in parallel or to signal that the Master has a fault. While FAULT#_D is used by NCP81418 to notify the Master that it has a fault.

Power−Up with VIN Release

Once the voltage at VDD rises above VDD UVLO threshold, NCP81418's LDO is always on irrespective of output enable status. In parallel configurations where data transfer is enabled, the Master will blank PMBus commands for approximately 2 ms after it is enabled. During this period, the Master will attempt to transfer stored settings in the Non−Volatile Memory to the NCP81418 slave devices. For this reason, it is recommended that any changes to the Master control registers be performed 2 ms or more after the VDD UVLO occurs and prior to enabling the device. Additionally, if the new settings are to be shared with the NCP81418 slave devices, that a Store_User_All command be sent following any writes to control registers and prior to enabling the device.

After the first 2 ms blanking, if there are no faults present, the NCP81418 slave devices release FAULT#_D to high, which indicates to the Master that the Slaves are ready for the data transfer. Then when the Master is enabled, FAULT#_C goes high, enabling itself and the slaves and data transfer begins. During data transfer FAULT#_D and FAULT#_C are configured as output signals (DATA, CLK) respectively from the Master device and input signals to the Slave. The Master sends a series of high frequency pulses on FAULT#_D to initiate the data transfer while FAULT#_C is held high until the transfer begins. Once data transmission is complete, FAULT#_C and FAULT#_D pins on the Master and Slaves revert back to being Master and Slave fault indicators respectively. Then the master drives FAULT#_C high signaling the slaves to begin soft−start simultaneously with the master.

The plot below showcases a simplified parallel eFuse application power−up event with data transfer enabled. The Master device detects a VIN Over−Voltage fault at the end of soft−start and asserts FAULT#_C to disable itself and the Slaves. If a slave fault would have occurred instead, FAULT#_D asserts low alerting the Master device which in turn asserts FAULT#_C low disabling all the NCP81418 slave devices simultaneously.

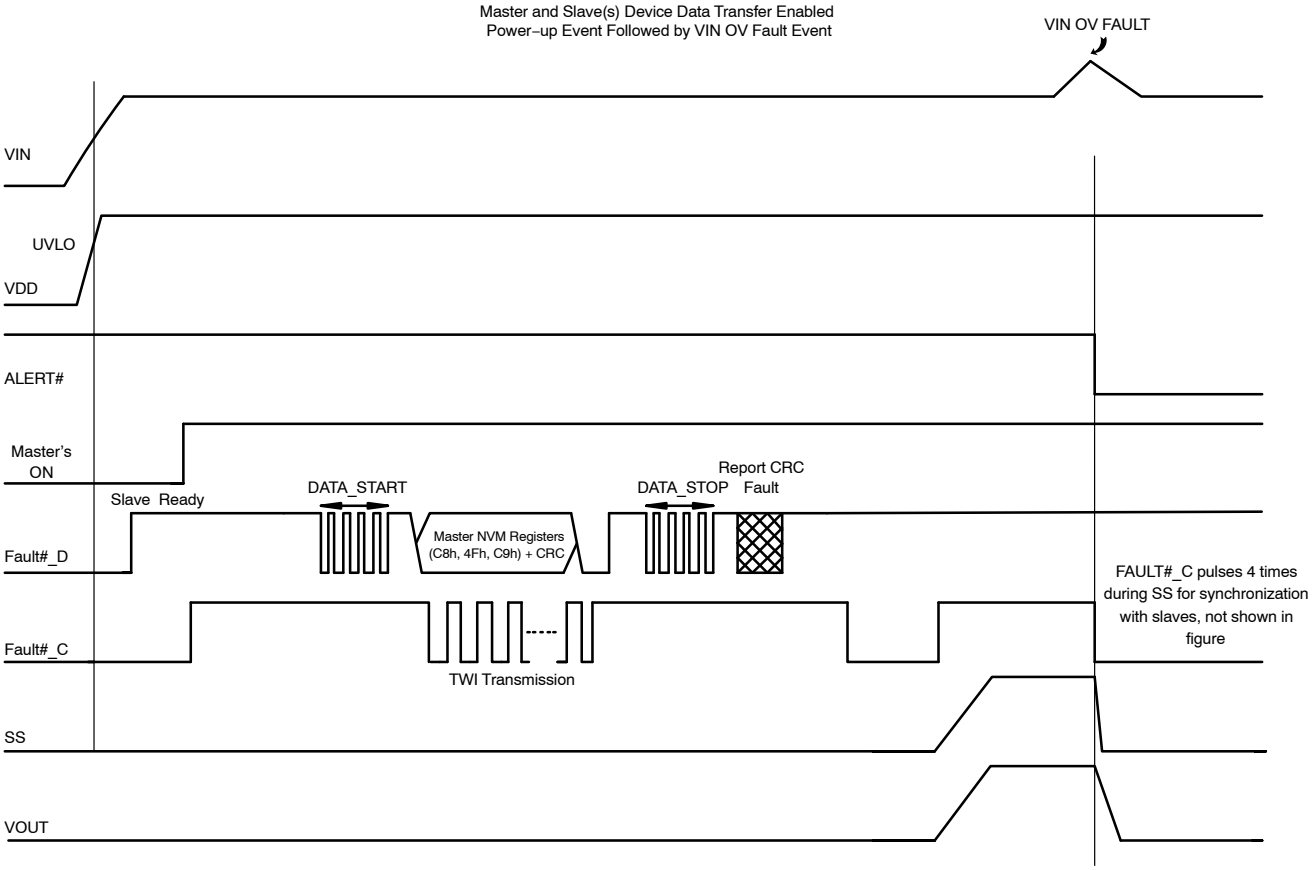


Figure 27. Data Transfer Sequence and VIN OV Fault

Simplified System Block Diagram

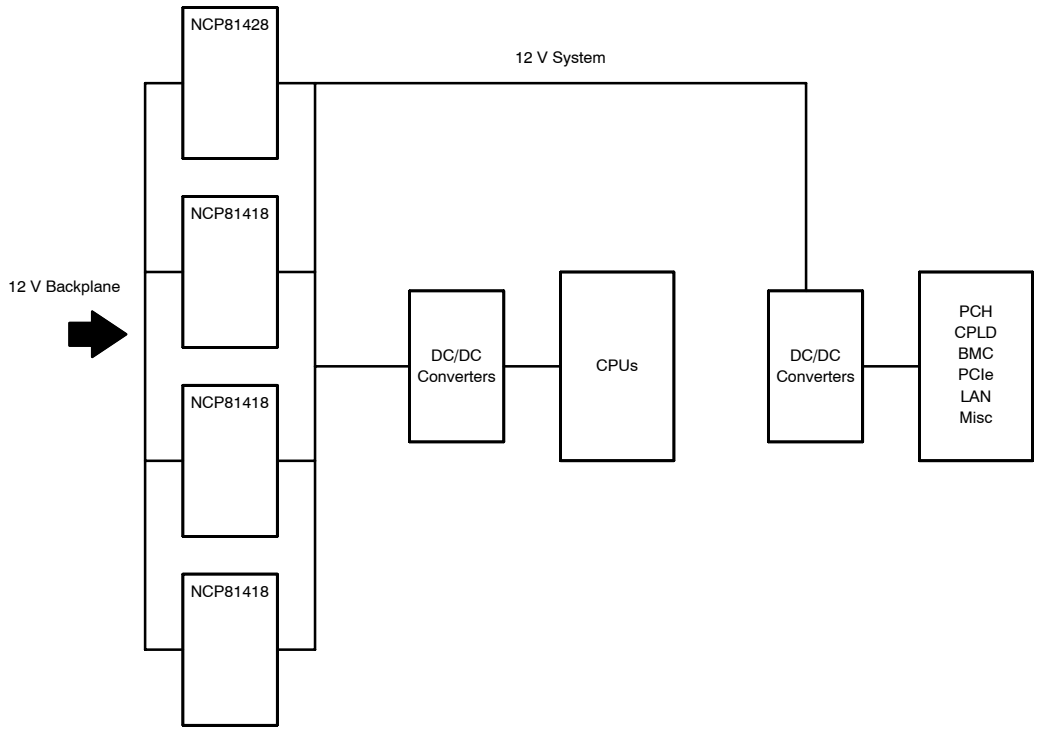


Figure 28. Simplified System Block Diagram

Configurations

Parallel eFuse Applications

A maximum of 6 NCP81418 devices can be paralleled as Slaves with NCP81428 as the Master. With the NCP81418 having its own TWI communication, the Master can provide over−current, over−temperature protection and base address settings to the Slaves from the Master's on−board, non−volatile memory (NVM). Additionally, if any Slave in the system identifies a fault, the Slave will alert the Master device by pulling FAULT#_D low. Upon capturing a FAULT#_D logic low, the Master forces FAULT#_C low to turn itself and all the slaves off. Utilizing the TWI bus features, communication and control can be entirely between the system's application processor and the Master eFuse. This reduces the complexity and host activity for parallel eFuse applications.

When power is applied to the NCP81418 slave device, no LDO faults are detected on either Master or Slave(s) and the LDO outputs have settled, POR is generated, manufacturer's default settings are populated. As the Master gets enabled, its NVM registers registers get transferred to all the Slaves simultaneously via the FAULT#_C and FAULT#_D pins. Note that copying the Master's NVM data to the slaves is repeated every time a fault is detected or power is removed and reapplied. The user must not alter the operating memory prior to enabling the device as that would cause a mismatch between what was written in the NVM and what gets transferred during the TWI process. Once the data transfer is complete, both the Master and the Slaves reconfigure their TWI bus pins to be a 2−wire fault notification system.

A fault event among a Slave will be relayed to the Master via FAULT#_D which asserts FAULT#_C low to disable all of the eFuses simultaneously.

Inputs/Outputs

VDD Output (Auxiliary Regulated Supply)

An internal linear regulator draws current from the VINF pin to produce and regulate the voltage at the VDD pin. This auxiliary output supply is current limited to I_{DD_CL}. A 4.7 μF ceramic capacitor must be placed between the VDD and GND pins and as close as possible to the NCP81418. The voltage difference between the VIN and VINF pin voltage should be within 0.4 V for adequate IMON performance. A small time constant R/C filter such as 1 Ω/0.1 μF on the VINF pin is recommended. The VDD pin is intended to power internal circuitry in the NCP81418. Do not connect any load to the VDD pin. Doing so, may result in erratic behavior.

Device Enable

Simplified Parallel Configuration Enabling and Soft−Start Synchronization Diagram

When the Master is in standby mode and no faults are present, FAULT#_D is driven high to indicate Slave readiness for data transfer. Then when the Master device is enabled, FAULT#_C goes high by the Master, which enables itself and all Slaves and data transfer begins. Once data transfer is complete, the Master drives FAULT#_C high signaling the Slaves to begin soft−start simultaneously with the Master. Note there are three 8us FAULT#_C logic high pulses that occur during the initial soft−start stage for gate pre−charge and synchronization between Master and Save to ensure a current balanced soft−start.

The diagram below showcases how the NCP81418 Slave releases FAULT#_D line to indicate readiness for the Master and upon receiving a logic high on the ON pin, the Master pulls up the FAULT#_C. Various state machine transitions were skipped as depicted by the dashed lines since this plot concentrates on enablement and soft−start sequencing.

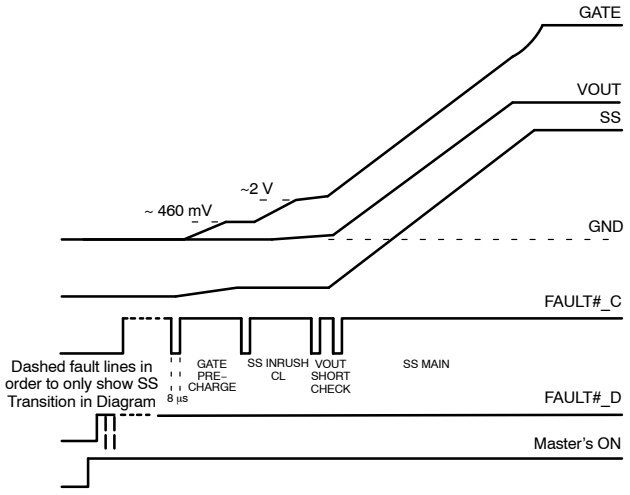


Figure 29. Soft Start Signals

SS Output (Soft−Start)

In parallel eFuse applications, the SS pins of all eFuses should be shorted together to one shared SS capacitor, note that only the Master device will source out the 5 μA current (ISS) to initiate soft−start. The internal soft−start load balancing circuitry will ensure the soft−start currents are evened out among the devices so that it doesn't put stress on one device over another or cause a soft start−current limiting event.

The soft−start capacitor value can be calculated by the following equation: $C_{SS} = (t_{SS} \times I_{SS} \times AV_{SS}) / VIN$ (where t_{SS} is the target soft−start time and the recommended range is 10−110 ms).

The typical C_{SS} values for different t_{SS} are approximated below for 12 V VIN.

Table 1. SOFT START PROGRAMMING CAPACITOR

T_{SS} (ms)	C_{SS} (nF)
12	47
20	82
29	120
43	180
52	220
64	270
78	330
110	470

The calculated soft−start times in Table 1 reflect the time when VOUT begins charging up from ground level to VIN. This does not include the gate pre−charge and synchronization delays before the main soft−start event which can be approximated to about 2 ms.

The maximum load capacitor value that NCP81418 can start up with depends on the device's soft−start time.

IMON Output (Current Monitor)

The IMON pin sources a current that is A_{IMON} (10 μA/A) times the VOUT output current. A 2 kΩ resistor connected from the IMON pin to ground must be used to monitor current information as a voltage up to V_{IM_CLMP}. A 100 nF capacitor can be used to low−pass filter the IMON signal without affecting the internal operation of the device. In parallel applications, the IMON pins of all eFuses should be tied together. Connect a 2 kΩ resistor from the IMON pin of each eFuse to the ground. The total equivalent IMON resistance would be 2 kΩ/#D, where #D is the number of eFuses in parallel. In order to simplify the BOM, one single RIMON resistor with the value of 2 kΩ/#D can be used across all IMON pins and the ground.

VTEMP Pin

The VTEMP pin is a voltage output proportional to the device's temperature, with an offset voltage (420 mV at 25°C). The VTEMP output can source much more current than it can sink, so that if multiple VTEMP pins are connected together, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest device in the application.

Data Transfer Sequencing

Figure 30 below represents the sequence of starting, transferring, checking, stopping and validation of the data transfer from the Master's NVM values to the slaves. During data transfer, the clock frequency will be a typical 400 kHz and the entire process will take approximately 120 μs.

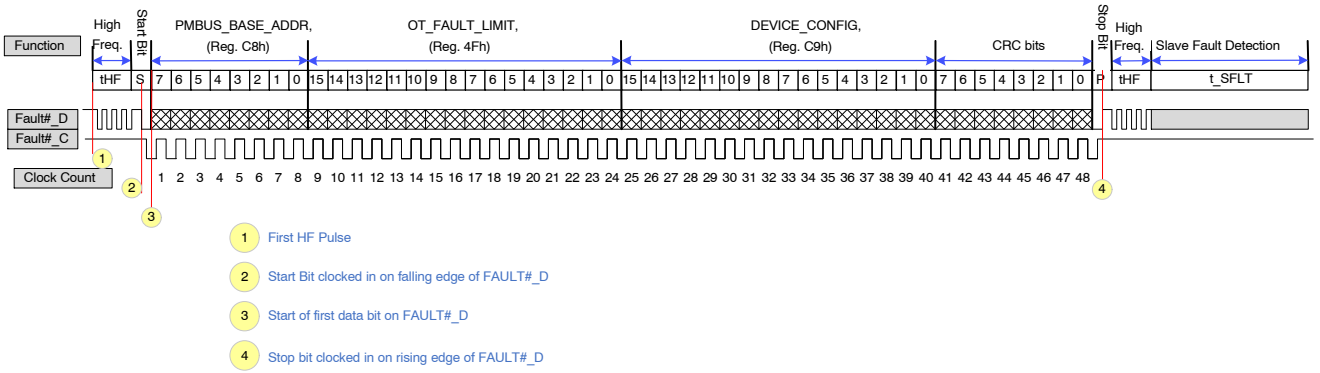


Figure 30. Master to Slave NVM Content Transfer Sequence

Warnings

Table 2. WARNINGS SUMMARY

Warning Type	FAULT#_C	FAULT#_D
Over_Temperature	H	H

NCP81418 only reports Over_Temperature warning.

FAULT#_C and FAULT#_D Operation

FAULT#_C and FAULT#_D are used for initiating soft−start and proper sequencing but also for fault communication between master and slave devices. Under normal operating conditions FAULT#_C and FAULT#_D are set in the high state. The tables below summarize the master / slaves actions upon a fault condition.

Table 3. FAULT#_C AND FAULT#_D FAULT BEHAVIOR

Slave Faults	FAULT#_C	FAULT#_D	Notes
SS Current Limit VDD UVLO FET Health OCP SCP OT**	*H to L	H to L	Slave FET health includes (VGS and VGD faults)

NOTE: In a Master/Slave system, only the Master monitors VIN and VOUT related faults.

*Represents a delayed signal on the master upon receiving a FAULT#_D low from the slave.

**Represents that a Slaves OT Fault range is from 120.5°C to 150°C. The Master is responsible for OT faults outside of this range.

10. A typical FAULT#_D to FAULT#_C delay is 500 ns.

Protection Features

Excessive Current Limiting at Start−up

During startup, the NCP81418 current limits are dependent on a number of factors such as VIN and VOUT levels relative to VIN.

Table 4. FOR V_{IN} < 13.2 V

VOUT/VIN	I_{CS}
0 < VOUT < 0.4 x VIN	7.5 A (Typ)
0.4 x VIN < VOUT < 0.8 x VIN	15 A (Typ)
0.8 x VIN < VOUT < VOUT~VIN	30 A (Typ)

Table 5. FOR V_{IN} > 13.2 V

VOUT/VIN	I_{CS}
0 < VOUT < 0.4 x VIN	5 A (Typ)
0.4 x VIN < VOUT < 0.8 x VIN	10 A (Typ)
0.8 x VIN < VOUT < VOUT~VIN	20 A (Typ)

As VOUT is approximately equal to VIN, the device stops current limiting and Over Current Protection becomes active.

If a current limiting condition exists anytime for a continuous duration > t_{CL_REG}, the device will restart or latch off based on the selection made by the Master.

Excessive Soft Start Duration

If VGS < VG_TH when t_{SS_FLT} expires, the NMOS FET latches−off or restarts based on the setting decided by the master.

Short Circuit Detection

The NCP81418 contains a high−bandwidth current sense SCP amplifier monitoring and rapidly responding to severe shorts which may cause irreparable damage. The fast current loop circuit allows the device to start pulling the gate low within the t_{SC} limit from the time it senses the fault. Once the Power FET latches−off, it either is restarted or remains latched off depending on the setting decided by the Master.

Over Current Protection

The NCP81418 provides three levels of over current protection (OCP), which are programmable via the Master. OCP1 provides the lowest current range while OCP3 allows up to 80 A before the device determines an overcurrent condition.

OCP1 and OCP2 settings can work in parallel to provide a case where a longer timer can be used for OCP1 and a shorter timer for OCP2 such that the energy during a fault remains similar and below the SOA of the device for the application. OCP3 is reserved for higher operating current applications.

Each OCP level can be programmed via the Master for a debounce time of 0.25 to 50 ms to determine if the fault is valid. A reset timer is also implemented such that if the current level exceeds the OCP setting, but returns to a value below the hysteresis of the OCP threshold for a minimum of 100 μs before the debounce timer expires, the debounce timer will reset. If an OCP debounce timer expires on a NCP81418 Slave device, it will pull FAULT#_D low to signal the Master of a fault.

Over Temperature Shutdown

The NCP81418 employs an internal thermal sensor for monitoring the die temperature. If the junction temperature exceeds the thermal shutdown fault threshold set by the master, the device will shut off. After thermal shutdown, the NCP81418 recovery mode depends on the Retry_Latchoff setting decided by the master. If retry mode is selected, when the die temperature falls below the OT_WARN_LIMIT, the device restarts. If latch−off mode is selected, the device has to be re−enabled for a restart and will only restart after the temperature falls below OT_WARN_LIMIT.

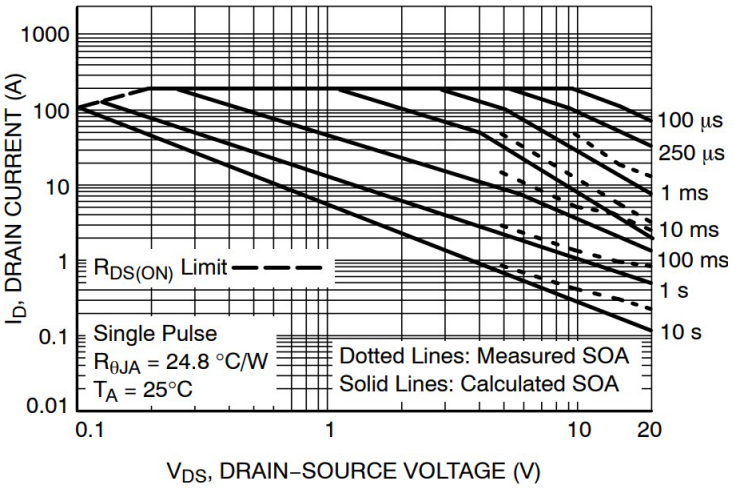
FET Fault Detection (FET Health)

NCP81418 contains various FET monitoring circuits:

- GATE to VIN short, latching/auto−retry condition: If the device is disabled and V_{GATE} > V_{DG_TH}, the device latches/auto−retries.
- GATE leakage: If (V_{GATE} −VINF) < V_{G_TH} after t_{SSF_FLT} expires, the device latches/auto−retries. The two faults mentioned above are monitored across both the Master and the NCP81418. FAULT#_C and FAULT#_D will pull low depending on the offending device. For instance, a NCP81418 device experiences a gate leakage when t_{SS_FLT} timer expires, then it will assert FAULT#_D low, alerting the Master, which in turn asserts FAULT#_C low to disable itself and the NCP81418 slave(s) simultaneously.

FET SOA Limits

The NCP81418 has built−in current limits and fault−monitoring circuits to ensure that the co−packaged powerFET is always kept within SOA limits. The startup current limiting conditions adjust based on the input voltage levels as described in the electrical specifications table to ensure constant power across the device throughout the soft−start transition. Refer to the internal current sensing section for more details. Note that the NCP81418 does not current limit during an OCP event because the powerFET will always be in the linear region.



Internal FET's Safe Operating Area (SOA)

Figure 31. Power FET Safe Operating Curves

Application Circuit

Application Circuit Diagram

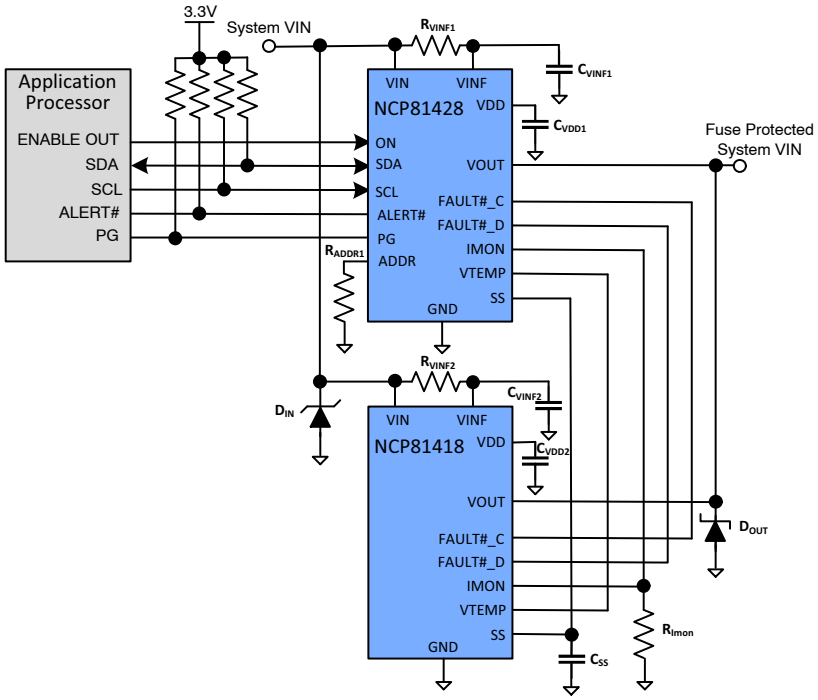


Figure 32. Application Circuit

Application Circuit Components

Table 6. PRIMARY COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
R_{VINF}	Vishay	CRCW06031R00FKEA	1 Ω	0603	75 V
C_{VINF}	Murata	0603YC104KAT2A	0.1 μF	0603	16 V
C_{VDD}	Murata	GRM188C81E475KE11D	4.7 μF	0603	25 V
R_{Imon}	YAGEO	RC0603FR−071KL	1 kΩ	0603	75 V
C_{SS}	Murata	0603YC104KAT2A	0.1 μF	0603	16 V
D_{IN}	LittleFuse	SMBJ13A	Clamping Voltage = 21.5 V, Peak Current = 28 A	DO− 214AA, 3.30 mm x 4.06 mm	13 V
D_{OUT}	**onsemi**	MBR2045MFST1G	20 A	8−SOFL, 5 mm x 6 mm	45 V

Application Component Guidelines

Transient Voltage Suppression

Hotswap eFuses are prone to sudden interruption in current flow, input cable inductance creates a positive voltage transient spike on the input of the device. These type of events if not suppressed by an external TVS diode they could easily exceed the AMR of the NCP81418. Similarly, output inductance creates a negative voltage spike on the output of the device that needs to be clamped by a diode with the cathode connected to ground and the anode to Vout.

Users can roughly estimate the magnitudes of these spike by referring to the Formula below:

$$V_{Spike} = V_{DC} + I_{OUT} \times \sqrt{L / C} \qquad \text{(eq. 1)}$$

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
MBR2045MFST1G	NCP81418	LQFN32 5x5, 0.5P	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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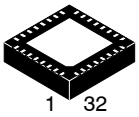
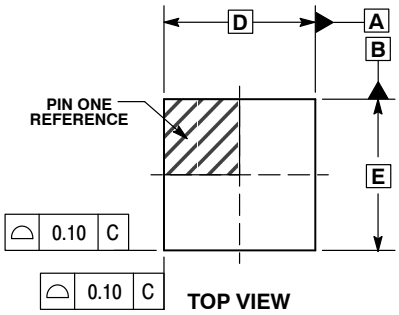
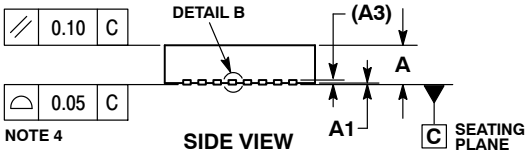
LQFN32 5x5, 0.5P
CASE 487AA
ISSUE A

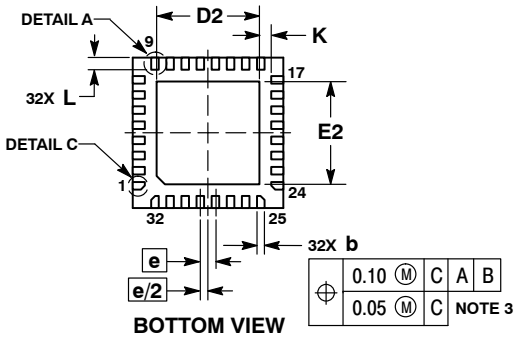
DATE 03 OCT 2017

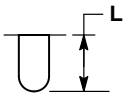


SCALE 2:1

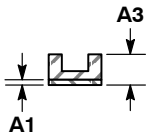




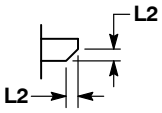




DETAIL A
ALTERNATE CONSTRUCTION



DETAIL B
ALTERNATE CONSTRUCTION

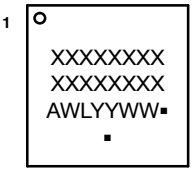


DETAIL C
4 PLACES

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	1.20	1.40
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.30	3.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L2	0.13 REF	

GENERIC MARKING DIAGRAM*

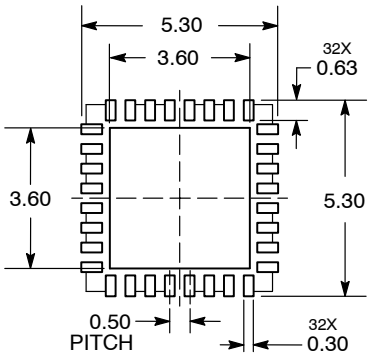


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**LQFN32, 5x5, 0.5P**	**PAGE 1 OF 1**

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