

# Synchronous Buck MOSFET Driver

## NCP81258

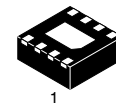
The NCP81258 is a high-performance dual MOSFET gate driver in a small 2 mm x 2 mm package, optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. A zero-current detection feature allows for a high-efficiency solution even at light load conditions. VCC UVLO ensures the MOSFETs are off when supply voltages are low. A bi-directional Enable pin provides a fault signal to the controller when a UVLO fault is detected.

### Features

- Space-efficient 2 mm x 2 mm DFN8 Thermally-enhanced Package
- VCC Range of 4.5 V to 13.2 V
- Internal Bootstrap Diode
- 5 V 3-stage PWM Input
- Zero Current Detect Function Provides Power Saving Operation during Light Load Conditions
- Bi-directional Enable Feature pulls Enable Pin Low during a UVLO Fault
- Pre-OVP Function Protects Load during HS FET Short
- Adaptive Anti-cross Conduction Circuit Protects against Cross-conduction during FET Turn-on and Turn-off
- Output Disable Control Turns Off Both MOSFETs via Enable Pin
- VCC Undervoltage Lockout
- These Devices are Pb-free, Halogen-free/BFR-free and are RoHS Compliant

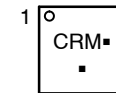
### Typical Applications

- Power Solutions for Notebook and Desktop Systems



1  
DFN8  
MN SUFFIX  
CASE 506AA

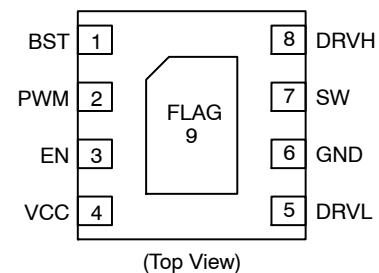
### MARKING DIAGRAM



CR = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

| Device        | Package           | Shipping <sup>†</sup> |
|---------------|-------------------|-----------------------|
| NCP81258MNTBG | DFN8<br>(Pb-Free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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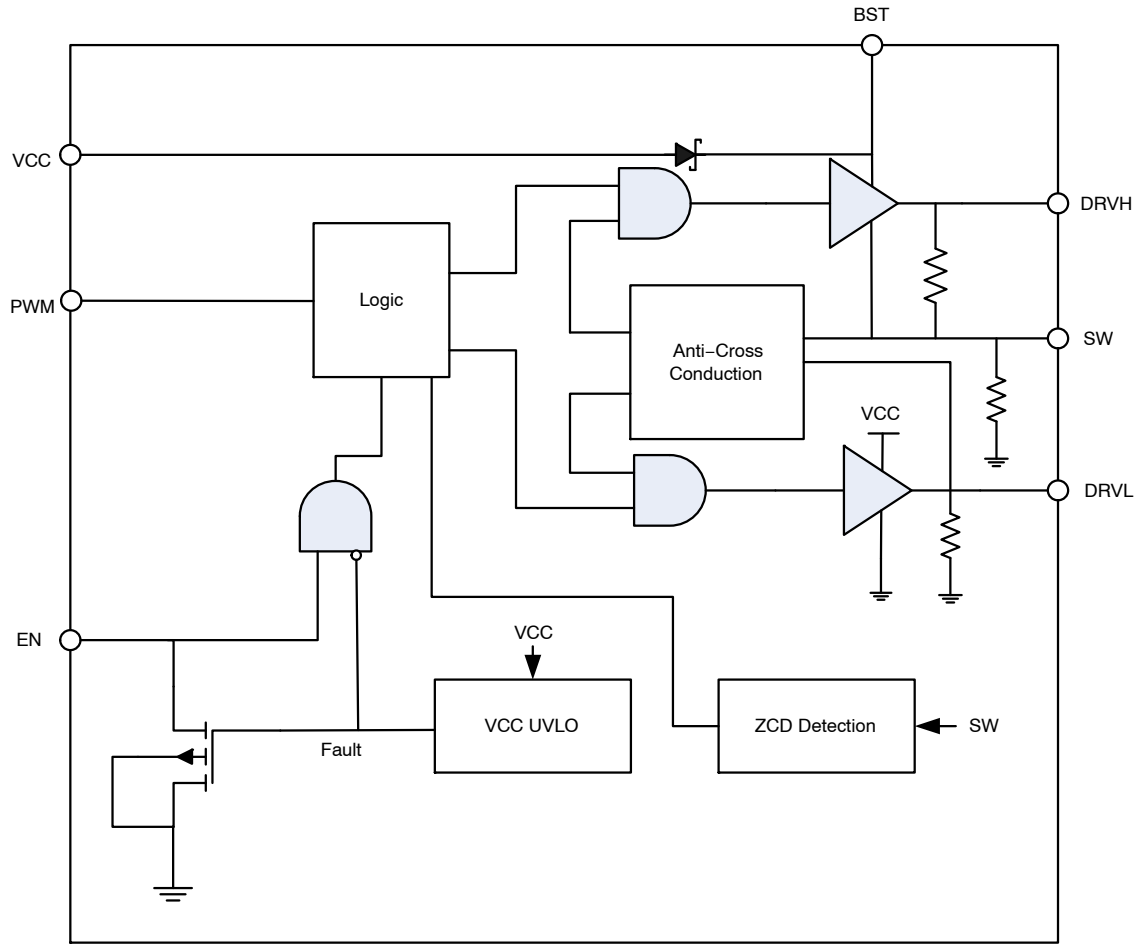


Figure 1. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description                                                                                                                                                           |
|---------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | BST      | Floating bootstrap supply pin for the high-side gate driver. Connect the external bootstrap capacitor between this pin and SW.                                        |
| 2       | PWM      | Control input:<br>PWM = High → DRVH is high, DRVL is low.<br>PWM = Mid → Zero current detect enabled. Diode emulation mode.<br>PWM = Low → DRVH is low, DRVL is high. |
| 3       | EN       | Control input:<br>EN = High → Driver is enabled.<br>EN = Low → Driver is disabled.                                                                                    |
| 4       | VCC      | Power supply input. Connect a bypass capacitor (1 $\mu$ F) from this pin to ground.                                                                                   |
| 5       | DRVL     | Low-side gate drive output. Connect to the gate of the low-side MOSFET.                                                                                               |
| 6       | GND      | Bias and reference ground. All signals are referenced to this node.                                                                                                   |
| 7       | SW       | Switch node. Connect this pin to the source of the high-side MOSFET and drain of the low-side MOSFET.                                                                 |
| 8       | DRVH     | High-side gate drive output. Connect to the gate of the high-side MOSFET.                                                                                             |
| 9       | FLAG     | Thermal flag. There is no electrical connection to the IC. Connect to the ground plane.                                                                               |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating                               | Symbol           | Min                                           | Max                                                         |
|--------------------------------------|------------------|-----------------------------------------------|-------------------------------------------------------------|
| Main Supply Voltage (Note 1)         | VCC              | -0.3 V                                        | 15 V<br>16 V (< 50 ns)                                      |
| Bootstrap Supply Voltage             | BST              | -0.3 V wrt/SW                                 | 35 V wrt/GND<br>40 V ( $\leq 50$ ns) wrt/GND<br>15 V wrt/SW |
| Switch Node Voltage                  | SW               | -5 V<br>-10 V ( $\leq 200$ ns)                | 35 V<br>40 V ( $\leq 50$ ns)                                |
| High-Side Driver Output              | DRVH             | -0.3 V wrt/SW<br>-2 V ( $\leq 200$ ns) wrt/SW | BST + 0.3 V<br>SW + 15 V (< 80 ns)                          |
| Low-Side Driver Output               | DRVL             | -0.3 V<br>-5 V ( $\leq 200$ ns)               | VCC + 0.3 V<br>15 V (< 80 ns)                               |
| DRVH/DRVL Control Input, Enable Pin  | PWM, EN          | -0.3 V                                        | 6.5 V                                                       |
| Ground                               | GND              | 0 V                                           | 0 V                                                         |
| Storage Temperature Range            | T <sub>STG</sub> | -55°C                                         | 150°C                                                       |
| Operating Junction Temperature Range | T <sub>J</sub>   | -40°C                                         | 150°C                                                       |
| Moisture Sensitivity Level           | MSL              | 1                                             |                                                             |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

**Table 3. THERMAL CHARACTERISTICS**

| Rating                                                                                | Symbol           | Value | Unit |
|---------------------------------------------------------------------------------------|------------------|-------|------|
| Thermal Characteristics, DFN8, 2x2 mm (Note 2)<br>Thermal Resistance, Junction-to-Air | R <sub>θJA</sub> | 74    | °C/W |

2. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

**Table 4. OPERATING RANGES** (Note 3)

| Rating              | Symbol         | Min | Max  | Unit |
|---------------------|----------------|-----|------|------|
| Input Voltage       | VCC            | 4.5 | 13.2 | V    |
| Ambient Temperature | T <sub>A</sub> | -10 | 125  | °C   |

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

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**Table 5. ELECTRICAL CHARACTERISTICS** VCC = 4.5 V to 13.2 V, BST-SW = 4.5 V to 13.2 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T<sub>A</sub> = 25°C, for min/max values T<sub>A</sub> = -10°C to 125°C; unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

## SUPPLY VOLTAGE

|                       |  |  |     |      |      |   |
|-----------------------|--|--|-----|------|------|---|
| VCC Operation Voltage |  |  | 4.5 |      | 13.2 | V |
| Pre-OVP VCC Threshold |  |  |     | 2.75 | 3.2  | V |

## UNDERVOLTAGE LOCKOUT

|                                              |                                         |                       |     |      |     |    |
|----------------------------------------------|-----------------------------------------|-----------------------|-----|------|-----|----|
| VCC Start Threshold                          | V <sub>CC</sub> rising                  | V <sub>UVLO</sub>     | 3.8 | 4.35 | 4.5 | V  |
| VCC UVLO Hysteresis                          |                                         | V <sub>UVLO_HYS</sub> | 150 | 200  | 250 | mV |
| Output Overvoltage Trip Threshold at Startup | V <sub>CC</sub> > Pre-OVP VCC Threshold |                       | 2.1 | 2.25 | 2.4 | V  |

## SUPPLY CURRENT

|                   |                                                                                                                |                       |  |      |     |    |
|-------------------|----------------------------------------------------------------------------------------------------------------|-----------------------|--|------|-----|----|
| Normal Mode       | I <sub>CC</sub> + I <sub>BST</sub> , EN = 5 V, PWM = 100 kHz, C <sub>LOAD</sub> = 3 nF for DRVH, 3 nF for DRVL | I <sub>normal</sub>   |  | 12.2 |     | mA |
| Shutdown Mode     | I <sub>CC</sub> + I <sub>BST</sub> , EN = GND                                                                  | I <sub>shutdown</sub> |  | 0.5  | 1.9 | mA |
| Standby Current 1 | I <sub>CC</sub> + I <sub>BST</sub> , EN = 5 V, PWM = 0 V, No loading on DRVH & DRVL                            | I <sub>standby1</sub> |  | 2.1  |     | mA |
| Standby Current 2 | I <sub>CC</sub> + I <sub>BST</sub> , EN = 5 V, PWM = 5 V, No loading on DRVH & DRVL                            | I <sub>standby2</sub> |  | 2.2  |     | mA |

## BOOTSTRAP DIODE

|                 |                                                     |  |     |     |     |   |
|-----------------|-----------------------------------------------------|--|-----|-----|-----|---|
| Forward Voltage | V <sub>CC</sub> = 12 V, Forward bias current = 2 mA |  | 0.1 | 0.4 | 0.6 | V |
|-----------------|-----------------------------------------------------|--|-----|-----|-----|---|

## PWM INPUT

|                    |  |                    |     |     |     |    |
|--------------------|--|--------------------|-----|-----|-----|----|
| PWM Input High     |  | PWM <sub>HI</sub>  | 3.4 |     |     | V  |
| PWM Mid-State      |  | PWM <sub>MID</sub> | 1.3 |     | 2.7 | V  |
| PWM Input Low      |  | PWM <sub>LO</sub>  |     |     | 0.7 | V  |
| ZCD Blanking Timer |  |                    |     | 250 |     | ns |

## HIGH-SIDE DRIVER (VCC = 12 V)

|                                    |                                                                                                    |                      |   |      |     |    |
|------------------------------------|----------------------------------------------------------------------------------------------------|----------------------|---|------|-----|----|
| Output Impedance, Sourcing Current | (V <sub>BST</sub> - V <sub>SW</sub> ) = 12 V                                                       |                      |   | 2.0  | 3.5 | Ω  |
| Output Impedance, Sinking Current  | (V <sub>BST</sub> - V <sub>SW</sub> ) = 12 V                                                       |                      |   | 1.0  | 2.0 | Ω  |
| DRVH Rise Time                     | V <sub>CC</sub> = 12 V, 3 nF load, (V <sub>BST</sub> - V <sub>SW</sub> ) = 12 V                    | tr <sub>DRVH</sub>   |   | 16   | 30  | ns |
| DRVH Fall Time                     | V <sub>CC</sub> = 12 V, 3 nF load, (V <sub>BST</sub> - V <sub>SW</sub> ) = 12 V                    | tf <sub>DRVH</sub>   |   | 11   | 25  | ns |
| DRVH Turn-Off Propagation Delay    | C <sub>load</sub> = 3 nF, [PWM = PWM <sub>LO</sub> ] to [V <sub>DRVH</sub> = 90%]                  | tpd <sub>lDRVH</sub> | 8 |      | 30  | ns |
| DRVH Turn-On Propagation Delay     | C <sub>load</sub> = 3 nF, [V <sub>DRVL</sub> = 1 V] to [V <sub>DRVH</sub> - V <sub>SW</sub> = 10%] | tpd <sub>hDRVH</sub> |   |      | 30  | ns |
| SW Pull-down Resistance            | SW to PGND                                                                                         |                      |   | 37.5 |     | kΩ |
| DRVH Pull-down Resistance          | DRVH to SW, (V <sub>BST</sub> - V <sub>SW</sub> ) = 0 V                                            |                      |   | 37.5 |     | kΩ |

## HIGH-SIDE DRIVER (VCC = 5 V)

|                                    |                                                                                                    |                      |  |      |  |    |
|------------------------------------|----------------------------------------------------------------------------------------------------|----------------------|--|------|--|----|
| Output Impedance, Sourcing Current | (V <sub>BST</sub> - V <sub>SW</sub> ) = 5 V                                                        |                      |  | 2.5  |  | Ω  |
| Output Impedance, Sinking Current  | (V <sub>BST</sub> - V <sub>SW</sub> ) = 5 V                                                        |                      |  | 1.6  |  | Ω  |
| DRVH Rise Time                     | V <sub>CC</sub> = 5 V, 3 nF load, (V <sub>BST</sub> - V <sub>SW</sub> ) = 5 V                      | tr <sub>DRVH</sub>   |  | 30   |  | ns |
| DRVH Fall Time                     | V <sub>CC</sub> = 5 V, 3 nF load, (V <sub>BST</sub> - V <sub>SW</sub> ) = 5 V                      | tf <sub>DRVH</sub>   |  | 27   |  | ns |
| DRVH Turn-Off Propagation Delay    | C <sub>LOAD</sub> = 3 nF, [PWM = PWM <sub>LO</sub> ] to [V <sub>DRVH</sub> = 90%]                  | tpd <sub>lDRVH</sub> |  | 20   |  | ns |
| DRVH Turn-On Propagation Delay     | C <sub>LOAD</sub> = 3 nF, [V <sub>DRVL</sub> = 1 V] to [V <sub>DRVH</sub> - V <sub>SW</sub> = 10%] | tpd <sub>hDRVH</sub> |  | 27   |  | ns |
| SW Pull-down Resistance            | SW to PGND                                                                                         |                      |  | 37.5 |  | kΩ |

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**Table 5. ELECTRICAL CHARACTERISTICS** VCC = 4.5 V to 13.2 V, BST-SW = 4.5 V to 13.2 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T<sub>A</sub> = 25°C, for min/max values T<sub>A</sub> = -10°C to 125°C; unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

## HIGH-SIDE DRIVER (VCC = 5 V)

|                           |                                                         |  |  |      |  |    |
|---------------------------|---------------------------------------------------------|--|--|------|--|----|
| DRVH Pull-down Resistance | DRVH to SW, (V <sub>BST</sub> - V <sub>SW</sub> ) = 0 V |  |  | 37.5 |  | kΩ |
|---------------------------|---------------------------------------------------------|--|--|------|--|----|

## LOW-SIDE DRIVER (VCC = 12 V)

|                                    |                                                                                                    |                      |   |      |     |    |
|------------------------------------|----------------------------------------------------------------------------------------------------|----------------------|---|------|-----|----|
| Output Impedance, Sourcing Current | V <sub>CC</sub> = 12 V                                                                             |                      |   | 2.0  | 3.5 | Ω  |
| Output Impedance, Sinking Current  | V <sub>CC</sub> = 12 V                                                                             |                      |   | 0.7  | 1.8 | Ω  |
| DRVL Rise Time                     | V <sub>CC</sub> = 12 V, C <sub>LOAD</sub> = 3 nF                                                   | tr <sub>DRVL</sub>   |   | 16   | 35  | ns |
| DRVL Fall Time                     | V <sub>CC</sub> = 12 V, C <sub>LOAD</sub> = 3 nF                                                   | tf <sub>DRVL</sub>   |   | 11   | 20  | ns |
| DRVL Turn-Off Propagation Delay    | C <sub>LOAD</sub> = 3 nF, [PWM = PWM <sub>HI</sub> ] to [V <sub>DRVL</sub> = 90%]                  | tpd <sub>DRVL</sub>  |   |      | 35  | ns |
| DRVL Turn-On Propagation Delay     | C <sub>LOAD</sub> = 3 nF, [V <sub>DRVH</sub> -V <sub>SW</sub> ] = 1 V to [V <sub>DRVL</sub> = 10%] | tpdh <sub>DRVL</sub> | 8 |      | 30  | ns |
| DRVL Pull-down Resistance          | DRVL to GND, VCC = GND                                                                             |                      |   | 37.5 |     | kΩ |

## LOW-SIDE DRIVER (VCC = 5 V)

|                                    |                                                                                                    |                      |  |      |  |    |
|------------------------------------|----------------------------------------------------------------------------------------------------|----------------------|--|------|--|----|
| Output Impedance, Sourcing Current | V <sub>CC</sub> = 5 V                                                                              |                      |  | 2.5  |  | Ω  |
| Output Impedance, Sinking Current  | V <sub>CC</sub> = 5 V                                                                              |                      |  | 1.0  |  | Ω  |
| DRVL Rise Time                     | V <sub>CC</sub> = 5 V, C <sub>LOAD</sub> = 3 nF                                                    | tr <sub>DRVL</sub>   |  | 30   |  | ns |
| DRVL Fall Time                     | V <sub>CC</sub> = 5 V, C <sub>LOAD</sub> = 3 nF                                                    | tf <sub>DRVL</sub>   |  | 22   |  | ns |
| DRVL Turn-Off Propagation Delay    | C <sub>LOAD</sub> = 3 nF, [PWM = PWM <sub>HI</sub> ] to [V <sub>DRVL</sub> = 90%]                  | tpd <sub>DRVL</sub>  |  | 27   |  | ns |
| DRVL Turn-On Propagation Delay     | C <sub>LOAD</sub> = 3 nF, [V <sub>DRVH</sub> -V <sub>SW</sub> ] = 1 V to [V <sub>DRVL</sub> = 10%] | tpdh <sub>DRVL</sub> |  | 12   |  | ns |
| DRVL Pull-down Resistance          | DRVL to GND, VCC = GND                                                                             |                      |  | 37.5 |  | kΩ |

## EN INPUT

|                                |                                                                        |                      |     |     |     |    |
|--------------------------------|------------------------------------------------------------------------|----------------------|-----|-----|-----|----|
| Enable Voltage High            |                                                                        | EN <sub>HI</sub>     | 2.0 |     |     | V  |
| Enable Voltage Low             |                                                                        | EN <sub>LO</sub>     |     |     | 1.0 | V  |
| Hysteresis                     |                                                                        |                      |     | 500 |     | mV |
| Normal Bias Current            |                                                                        |                      | -1  |     | 1   | μA |
| Enable Pin Sink Current        |                                                                        |                      | 4   |     | 30  | mA |
| EN High Propagation Delay Time | PWM = 0 V, EN going from 0 V to EN <sub>HI</sub> to DRVL rising to 10% | tpd <sub>EN_HI</sub> |     |     | 60  | μs |

## SWITCH NODE

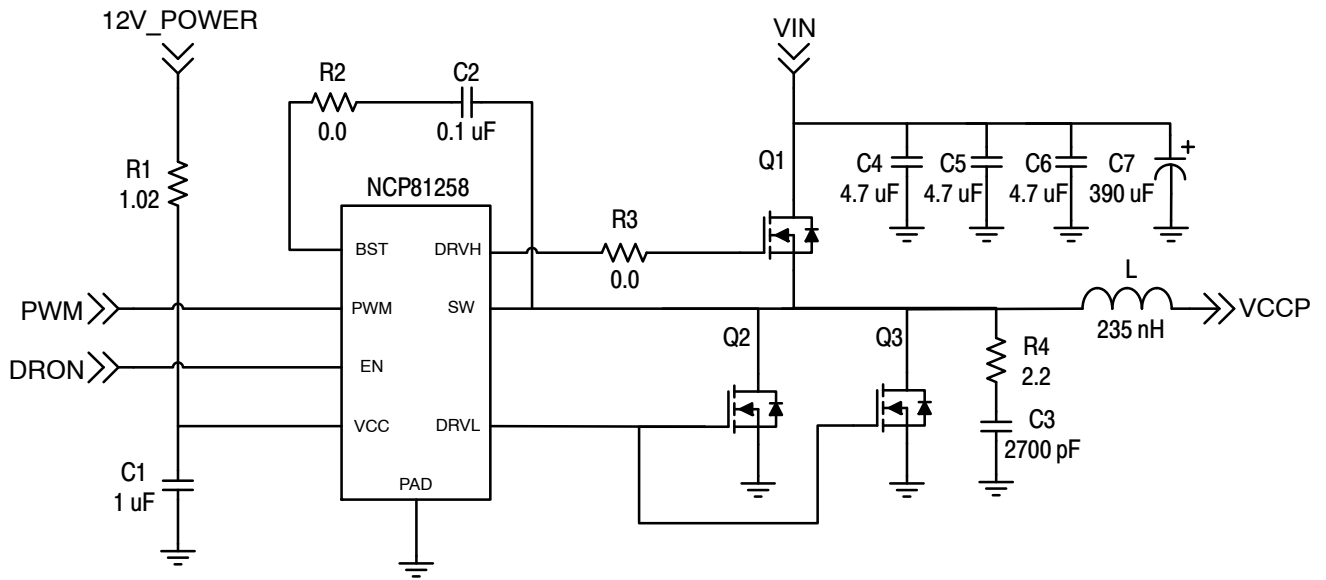
|                                        |                                                     |  |  |    |    |    |
|----------------------------------------|-----------------------------------------------------|--|--|----|----|----|
| SW Node Leakage Current                |                                                     |  |  |    | 20 | μA |
| Zero Cross Detection Threshold Voltage | Ramp slowly until DRVL goes off (start in DCM mode) |  |  | -3 |    | mV |

- Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T<sub>J</sub> = T<sub>A</sub> = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
- Values based on design and/or characterization.

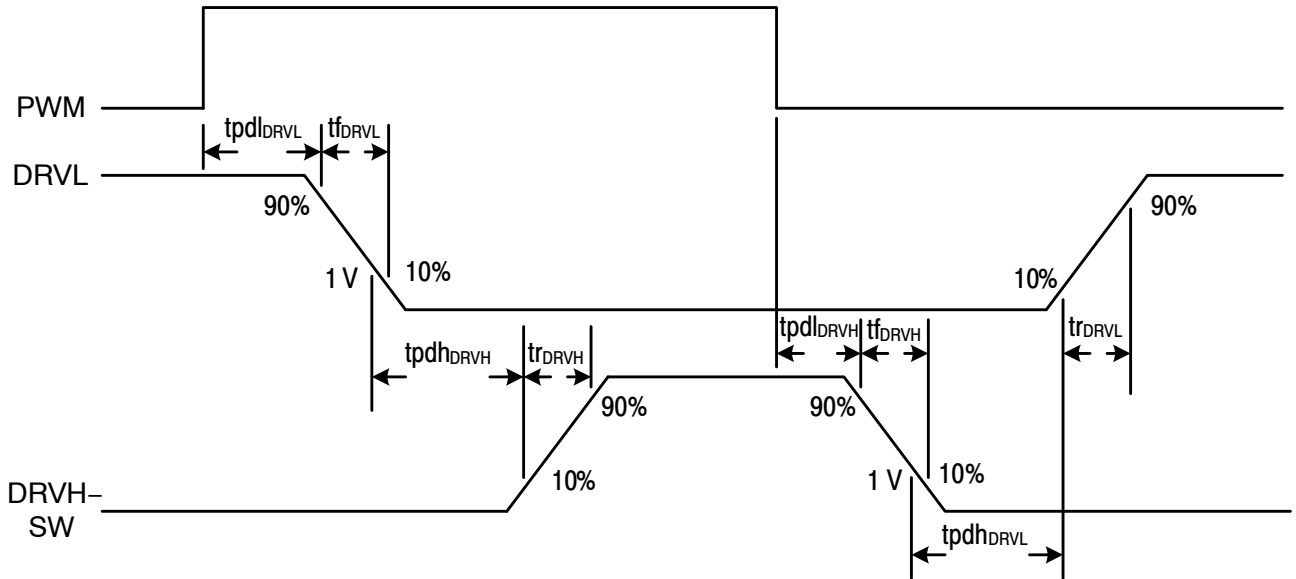
**Table 6. ZCD DECODER TRUTH TABLE**

| PWM Input                  | ZCD                                                          | DRVL | DRVH |
|----------------------------|--------------------------------------------------------------|------|------|
| PWM High                   | ZCD Reset                                                    | Low  | High |
| PWM Mid (positive current) | Positive current through the inductor                        | High | Low  |
| PWM Mid (negative current) | Zero current through the inductor (after ZCD blanking timer) | Low  | Low  |
| PWM Low                    | ZCD Reset                                                    | High | Low  |

**NCP81258**



### Figure 2. Application Circuit



### Figure 3. Gate Timing Diagram

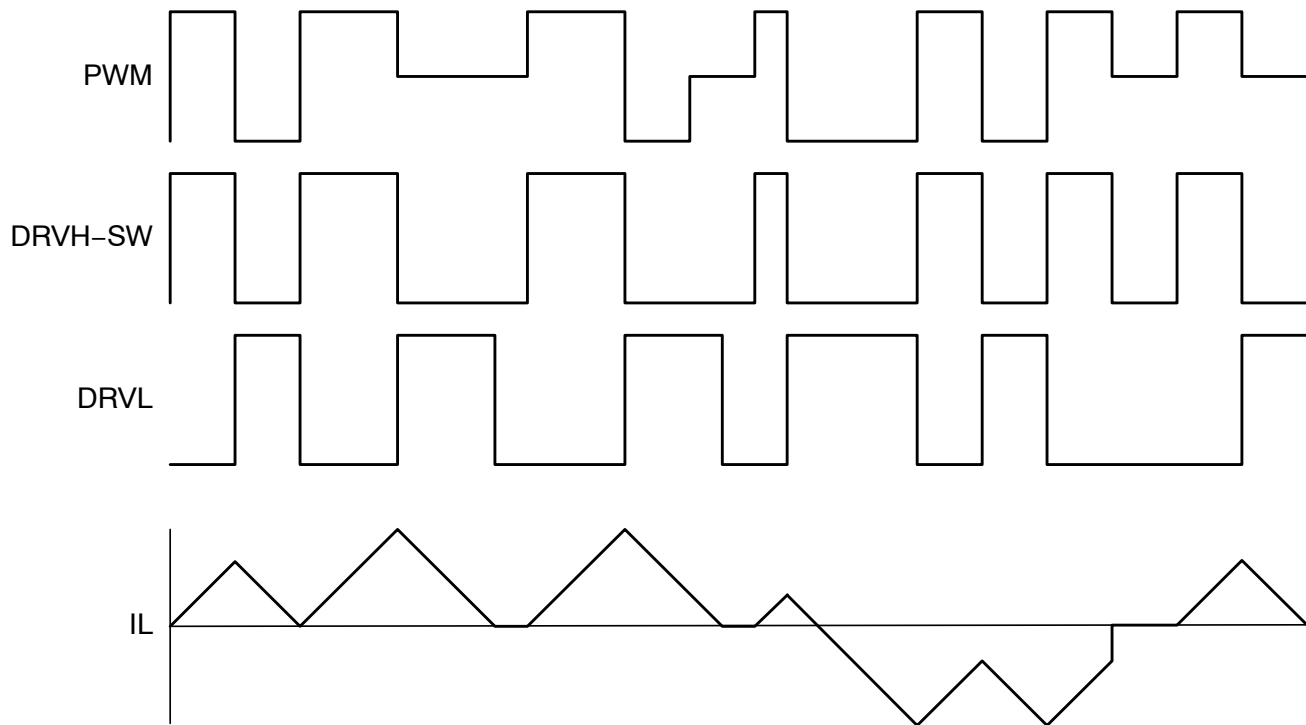


Figure 4. PWM/EN Logic Diagram

## APPLICATIONS INFORMATION

The NCP81258 gate driver is a single-phase MOSFET driver designed for driving N-channel MOSFETs in a synchronous buck converter topology.

### Low-Side Driver

The low-side driver is designed to drive a ground-referenced low- $R_{DS(on)}$  N-channel MOSFET. The voltage supply for the low-side driver is internally connected to the VCC and GND pins.

### High-Side Driver

The high-side driver is designed to drive a floating low- $R_{DS(on)}$  N-channel MOSFET. The gate voltage for the high-side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81258 is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high-side driver will turn on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the SW pin rises. When the high-side MOSFET is fully turned on, SW will settle to VIN, and BST will settle to VIN + VCC (excluding parasitic ringing).

### Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor ( $C_{BST}$ ) and an integrated diode to provide current to the high-side driver. A multi-layer ceramic capacitor

(MLCC) with a value greater than 100 nF should be used for  $C_{BST}$ .

### Power Supply Decoupling

The NCP81258 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low-ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1  $\mu$ F and 4.7  $\mu$ F is typically used.

### Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull-down resistors on DRVH, DRVL and SW to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

### Pre-Overvoltage Protection

The pre-Overvoltage Protection (pre-OVP) feature is used to protect the load if there is a short across the high-side FET. When VCC is greater than 2.75 V, the voltage on SW is monitored. During startup, if SW is determined to be greater than Output Overvoltage Trip Threshold, DRVL will be latched high to turn on the synchronous FET and provide a path from VIN to ground. This also pulls the EN pin low. To exit this behavior, power to the driver must be turned off (VCC less than  $V_{UVLO}$  minus  $V_{UVLO\_HYS}$ ) and then VCC powered back on. When VCC rises above  $V_{UVLO}$  and EN is

above  $EN_{HI}$ , the gate driver enters normal PWM operation if SW is no longer above the Output Overvoltage Trip Threshold.

### Bi-Directional EN Signal

The Enable pin (EN) is used to disable the DRVH and DRVH outputs to prevent power transfer. When EN is above the  $EN_{HI}$  threshold, DRVH and DRVH change their states according to the PWM input. A UVLO fault turns on the internal MOSFET that pulls the EN pin towards ground. By connecting EN to the DRON pin of a controller, the controller is alerted when the driver encounters a fault condition.

Every time EN is brought from a low to a high state, the NCP81258 conducts an auto-calibration cycle on the ZCD SW threshold. During the auto-calibration cycle, the driver outputs are prevented from responding to the PWM input, and both outputs are in the low state. This auto-calibration cycle is guaranteed to complete by 60  $\mu$ s.

### Three-State PWM Input

Switching PWM between logic-high and logic-low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet. Refer to Figure 21 for the gate timing diagrams and Table 1 for the EN/PWM logic table.

When PWM is set above  $PWM_{HI}$ , DRVH will first turn off after a propagation delay of  $tpd_{DRVH}$ . To ensure non-overlap between DRVH and DRVH, there is a delay of  $tpdh_{DRVH}$  from the time DRVH falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below  $PWM_{LO}$ , DRVH will first turn off after a propagation delay of  $tpd_{DRVH}$ . To ensure non-overlap between DRVH and DRVH, there is a delay of

$tpdh_{DRVH}$  from the time DRVH – SW falls to 1 V, before DRVH is allowed to turn on.

When PWM enters the mid-state voltage range,  $PWM_{MID}$ , DRVH goes high after the non-overlap delay, and stays high for the duration of the ZCD blanking timer and an 80 ns de-bounce timer. Once these timers expire, SW is monitored for zero current detection and pulls DRVH low once zero current is detected.

### Thermal Considerations

As power in the NCP81258 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81258 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81258 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 1})$$

Since  $T_J$  is not recommended to exceed 150°C, the NCP81258, soldered on to a 645 mm<sup>2</sup> copper area, using 1 oz. copper and FR4, can dissipate up to 2.3 W when the ambient temperature ( $T_A$ ) is 25°C. The power dissipated by the NCP81258 can be calculated from the following equation:

$$P_D \approx VCC \times \left[ (n_{HS} \times Q_{gHS} + n_{LS} \times Q_{gLS}) \times f + I_{standby} \right] \quad (\text{eq. 2})$$

Where  $n_{HS}$  and  $n_{LS}$  are the number of high-side and low-side FETs, respectively,  $Q_{gHS}$  and  $Q_{gLS}$  are the gate charges of the high-side and low-side FETs, respectively and  $f$  is the switching frequency of the converter.

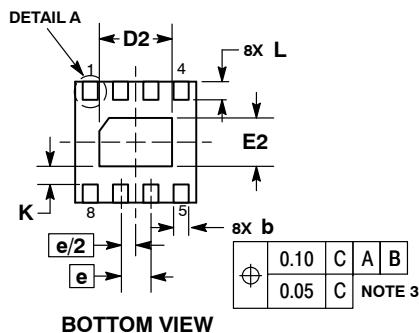
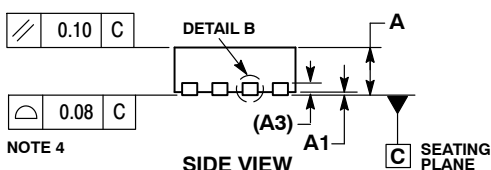
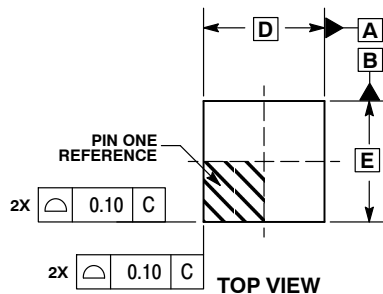




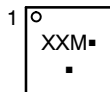
SCALE 4:1

DFN8 2x2, 0.5P  
CASE 506AA  
ISSUE F

DATE 04 MAY 2016

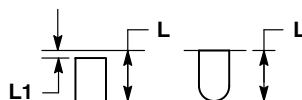


GENERIC  
MARKING DIAGRAM\*

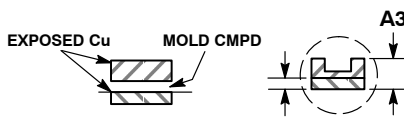


XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



DETAIL A  
OPTIONAL  
CONSTRUCTIONS



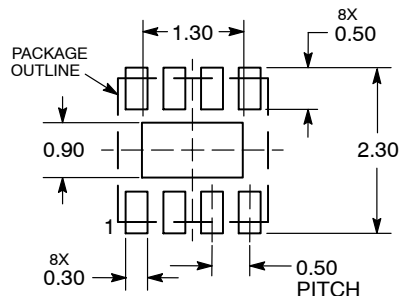
DETAIL B  
ALTERNATE  
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 2.00 | BSC  |
| D2          | 1.10 | 1.30 |
| E           | 2.00 | BSC  |
| E2          | 0.70 | 0.90 |
| e           | 0.50 | BSC  |
| K           | 0.30 | REF  |
| L           | 0.25 | 0.35 |
| L1          |      | 0.10 |

RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                            |                                                                                                                                                                                  |
|------------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | DFN8, 2.0X2.0, 0.5MM PITCH | PAGE 1 OF 1                                                                                                                                                                      |

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