Dual-Channel/Two-Phase Controller for DrMOS

NCP81234

The NCP81234, a dual−channel/two−phase synchronous buck controller, provides flexible power management solutions for applications supported by DrMOS. Operating in high switching frequency up to 1.2 MHz allows employing small size inductor and capacitors.

Features

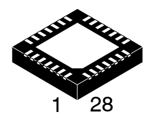
- Single Vin = 4.5 ~ 20 V with Input Feedforward
- Integrated 5.35 V LDO
- Vout = 0.6 V ~ 5.3 V
- Fsw = 200 k ~ 1.2 MHz
- PWM Output Compatible to 3.3 V and 5 V DrMOS
- Dual−Channel or Two−Phase Operation
- DDR Power Mode Option
- Interleaved Operation
- Differential Current Sense Compatible for both Inductor DCR Sense and DrMOS Iout
- 2 Independent Enables with Programmable Input UVLO
- Programmable DrMOS Power Ready Detection (DRVON)
- 2 Power Good Indicators
- Comprehensive Fault Indicator
- Externally Programmable Soft Start and Delay Time
- Programmable Hiccup Over Current Protection
- Hiccup Under Voltage Protection
- Recoverable Over Voltage Protection
- Hiccup Over Temperature Protection
- Thermal Shutdown Protection
- QFN−28, 5x5 mm, 0.5 mm Pitch Package
- This is a Pb−Free Device

Typical Applications

- Telecom Applications
- Server and Storage System
- Multiple Rail Systems
- DDR Applications

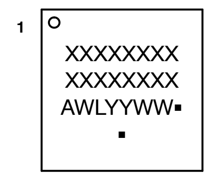
ON Semiconductor®

www.onsemi.com



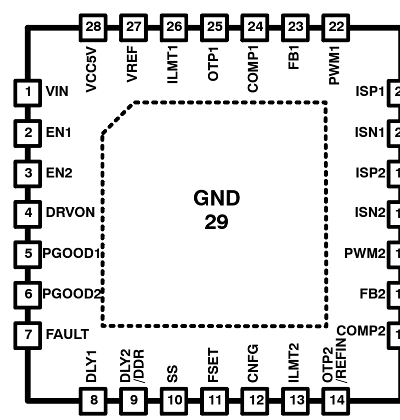
QFN28
MN SUFFIX
CASE 485BQ

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81234MNTXG	QFN28 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	VIN	Power Input	Power Supply Input. Power supply input pin of the device, which is connected to the integrated 5 V LDO. 4.7 μF or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin.
2	EN1	Analog Input	Enable 1. Logic high enables channel 1 and logic low disables channel 1. Input supply UVLO can be programmed at this pin for channel 1.
3	EN2	Analog Input	Enable 2. Logic high enables channel 2 and logic low disables channel 2. Input supply UVLO can be programmed at this pin for channel 2.
4	DRVON	Logic Input	Driver On. Logic high input means drivers' power is ready.
5	PGOOD1	Logic Output	Power GOOD 1. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window of channel 1.
6	PGOOD2	Logic Output	Power GOOD 2. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window of channel 2.
7	FAULT	Logic Output	Fault. Digital output to indicate fault mode.
8	DLY1	Analog Input	Delay 1. A resistor from this pin to GND programs delay time of soft start for channel 1.
9	DLY2/DDR	Analog Input	Delay 2 / DDR. A resistor from this pin to GND programs delay time of soft start for channel 2. Short to GND to have DDR operation mode.
10	SS	Analog Input	Soft Start Time. A resistor from this pin to ground programs soft start time for both channels.
11	FSET	Analog Input	Frequency Selection. A resistor from this pin to ground programs switching frequency.
12	CNFG	Analog Input	Configuration. A resistor from this pin to ground programs configuration of power stages.
13	ILIMT2	Analog Input	Limit of Current 2. Voltage at this pin sets over−current threshold for channel 2.
14	OTP2/REFIN	Analog Input	Over Temperature Protection 2. Voltage at this pin sets over−temperature threshold for channel 2.
15	COMP2	Analog Output	Compensation 2. Output pin of error amplifier of channel 2.
16	FB2	Analog Input	Feedback 2. An inverting input of internal error amplifier for channel 2.
17	PWM2	Analog Output	PWM 2. PWM output of phase 2.
18	ISN2	Analog Input	Current Sense Negative Input 2. Inverting input of differential current sense amplifier of phase 2.
19	ISP2	Analog Input	Current Sense Positive Input 2. Non−inverting input of differential current sense amplifier of phase 2.
20	ISN1	Analog Input	Current Sense Negative Input 1. Inverting input of differential current sense amplifier of phase 1.
21	ISP1	Analog Input	Current Sense Positive Input 1. Non−inverting input of differential current sense amplifier of phase 1.
22	PWM1	Analog Output	PWM 1. PWM output of phase 1.
23	FB1	Analog Input	Feedback 1. An inverting input of internal error amplifier for channel 1.
24	COMP1	Analog Output	Compensation 1. Output pin of error amplifier of channel 1.
25	OTP1	Analog Input	Over Temperature Protection 1. Voltage at this pin sets over−temperature threshold for channel 1.
26	ILIMT1	Analog Input	Limit of Current 1. Voltage at this pin sets over−current threshold for channel 1.
27	VREF	Analog Output	Output of Reference. Output of 0.6 V reference. A 10 nF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
28	VCC5V	Analog Power	Voltage Supply of Controller. Output of integrated 5.35 V LDO and power supply input pin of control circuits. A 4.7 μF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
29	THERM/GND	Analog Ground	Thermal Pad and Analog Ground. Ground of internal control circuits. Must be connected to the system ground.

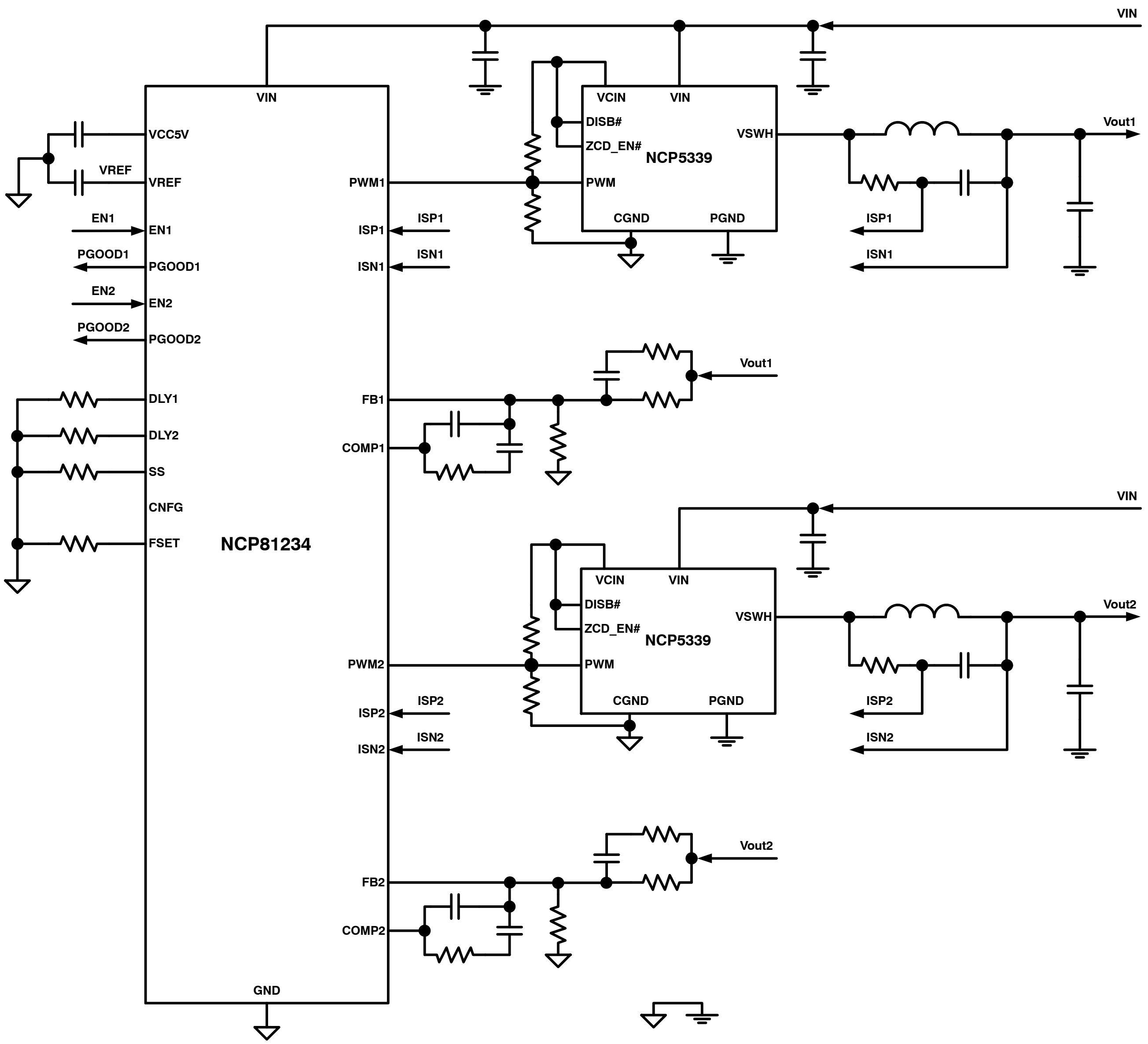


Figure 1. Typical Application Circuit for Dual−Channel Applications

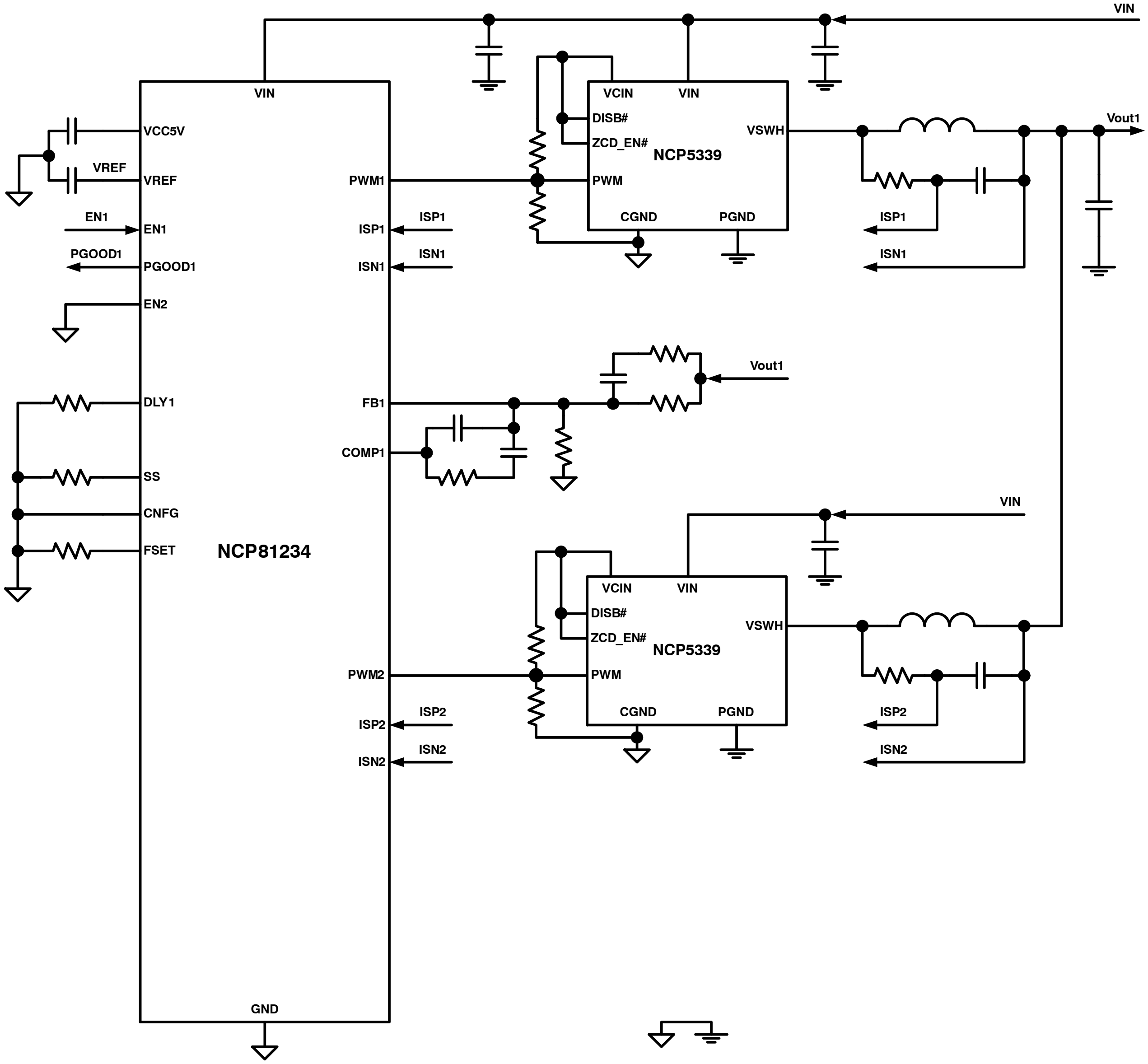


Figure 2. Typical Application Circuit for Two−Phase Applications

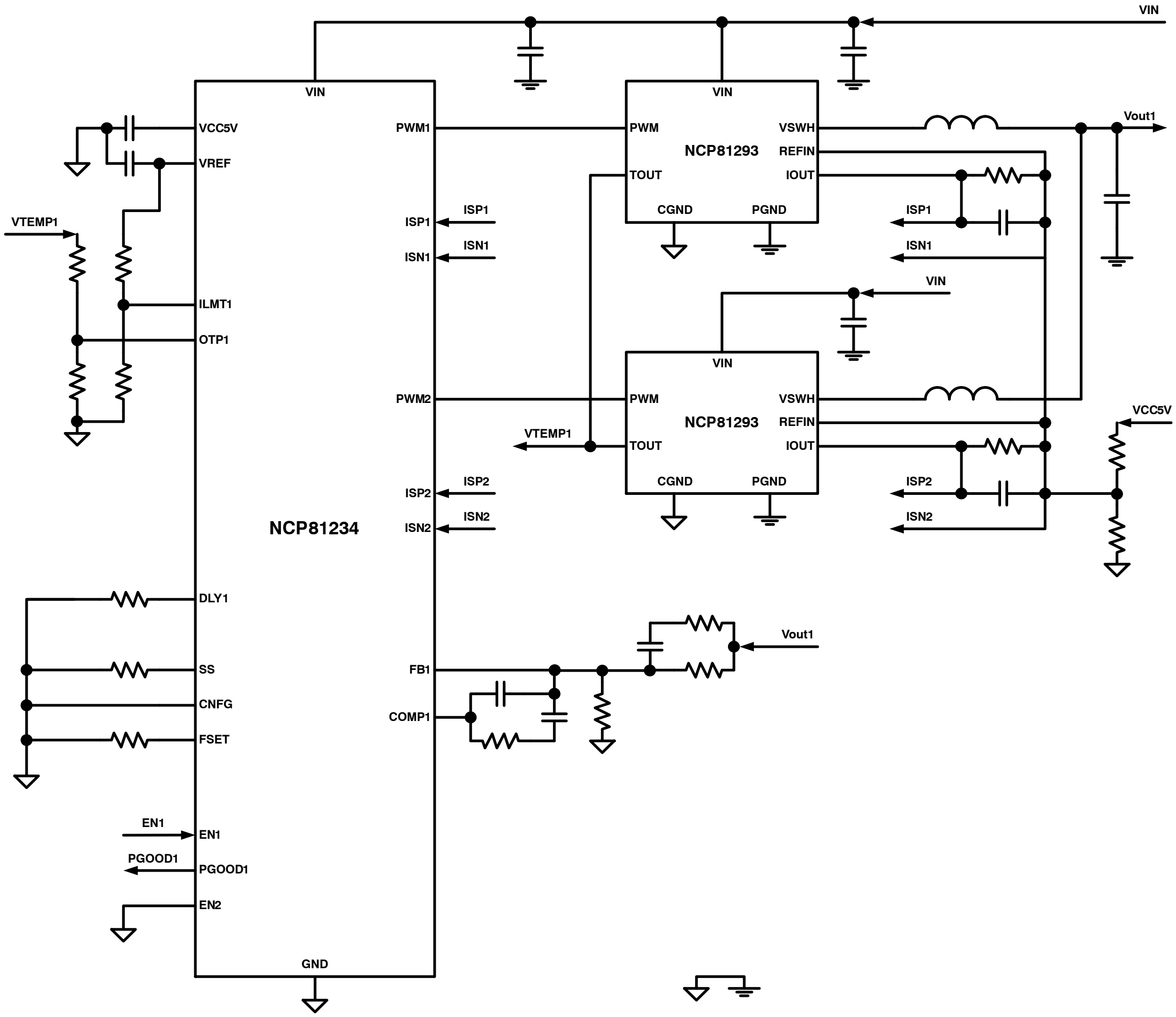


Figure 3. Typical Two–Phase Application Circuit for DrMOS with Integrated Current Sense and Temperature Sense

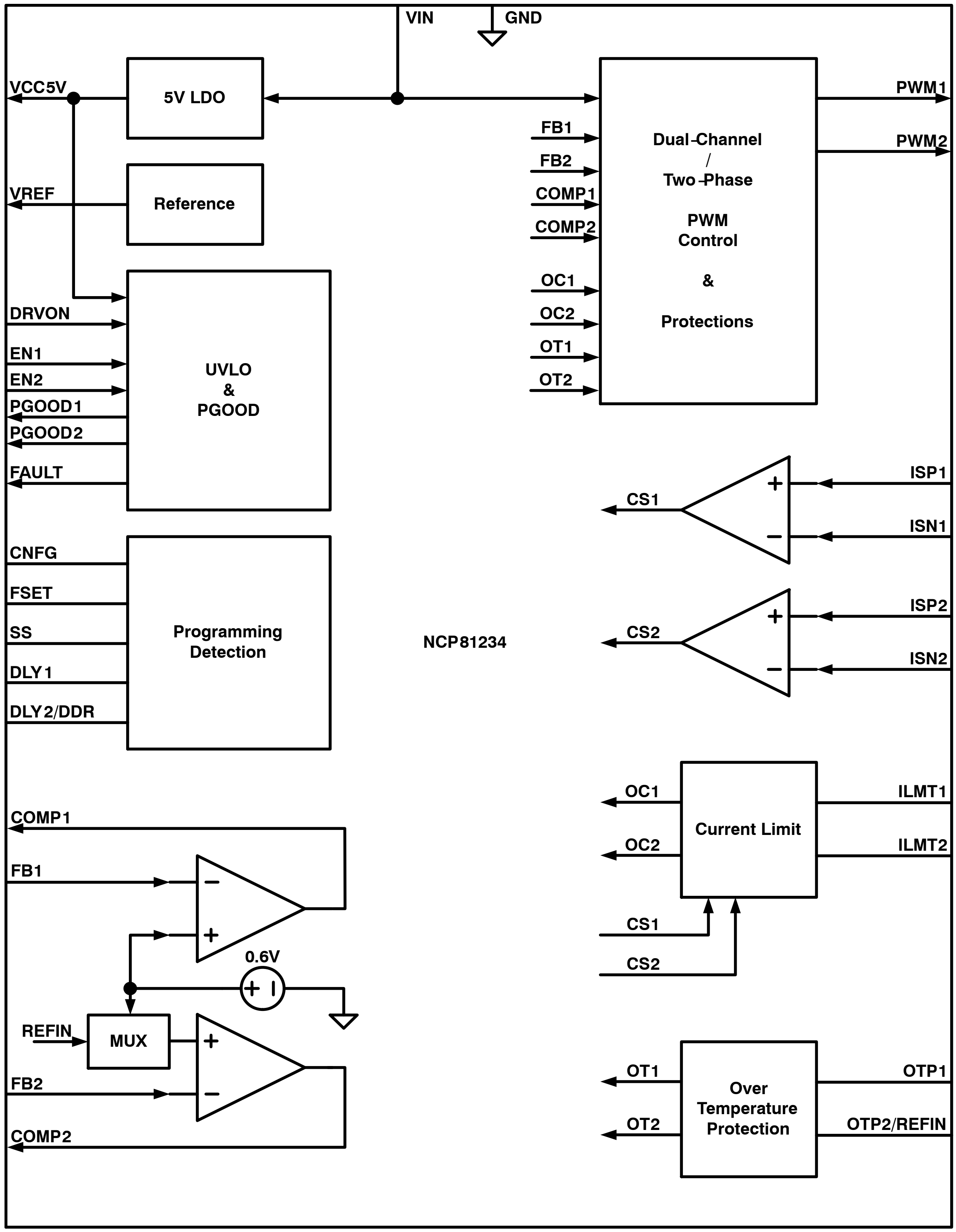


Figure 4. Functional Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage to PGND	V_{VIN}		30	V
Supply Voltage VCC5V to GND	V_{VCC5V}	−0.3	6.5	V
Other Pins to GND		−0.3	VCC5V + 0.3	V
Human Body Model (HBM) ESD Rating (Note 1)	ESD HBM		2000	V
Machine Model (MM) ESD Rating (Note 1)	ESD MM		200	V
Latch up Current: (Note 2) All pins, except digital pins Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range (Note 3)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	125	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction to Top Case (Note 4)	$R_{\Psi JC}$	5.0		°C/W
Thermal Resistance Junction to Board (Note 4)	$R_{\Psi JB}$	3.8		°C/W
Thermal Resistance Junction to Ambient (Note 4)	$R_{\theta JA}$	38		°C/W
Power Dissipation (Note 5)	P_D	2.63		W
Moisture Sensitivity Level (Note 6)	MSL	1		–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. JEDEC standard JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM. It is for checking junction temperature using external measurement.
5. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected. $T_A = 25°C$, $T_{J\_max} = 125°C$, $P_D = (T_{J\_max−T\_amb})$/Theta JA
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to T_A = 25°C, Min and Max values are referenced to T_A from −40°C to 125°C. unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
VIN Supply Voltage Range	(Note 7)	V_{IN}	4.5	12	20	V
VCC5V Under−Voltage (UVLO) Threshold	VCC5V falling	V_{CCUV-}	3.7			V
VCC5V OK Threshold	VCC5V rising	V_{CCOK}			4.3	V
VCC5V UVLO Hysteresis		V_{CCHYS}		260		mV
VCC5V REGULATOR						
Output Voltage	6 V < VIN < 20 V, I_{VCC5V} = 15 mA (External), EN1 = EN2 = Low	V_{CC}	5.2	5.35	5.5	V
Load Regulation	I_{VCC5V} = 5 mA to 25 mA (External), EN1 = EN2 = Low		−2.0	0.2	2.0	%
Dropout Voltage	VIN = 5 V, I_{VCC5V} = 25 mA (External), EN1 = EN2 = Low	V_{DO_VCC}			200	mV
SUPPLY CURRENT						
VIN Quiescent Current	EN1 high, 1 channel and 1 phase only EN1 and EN2 high, 2 channel and 2 phase	I_{QVIN}	– –	15 18	20 25	mA
VIN Shutdown Current	EN1 and EN2 low	I_{sdVIN}	–	8	10	mA
REGULATION REFERENCE						
Regulated Feedback Voltage	Include offset of error amplifier, 0°C to 85°C	V_{FB}	596	600	604	mV
	Include offset of error amplifier, −40°C to 125°C		594	600	606	
REFERENCE OUTPUT						
VREF Output Voltage	I_{VREF} = 500 μA	V_{VREF}	594	600	606	mV
Load Regulation	I_{VREF} = 0 mA to 2 mA		−1.0		1.0	%
VOLTAGE ERROR AMPLIFIER						
Open−Loop DC Gain	(Note 7)	$GAIN_{EA}$		80		dB
Unity Gain Bandwidth	(Note 7)	GBW_{EA}		20		MHz
Slew Rate	(Note 7)	SR_{COMP}		20		V/μs
COMP Voltage Swing	$I_{COMP(source)}$ = 2 mA	$V_{maxCOMP}$	3.2	3.4	–	V
	$I_{COMP(sink)}$ = 2 mA	$V_{minCOMP}$	–	1.05	1.15	
FB, REFIN Bias Current	V_{FB} = V_{REFIN} = 1.0 V	I_{FB}	−400		400	nA
DIFFERENTIAL CURRENT−SENSE AMPLIFIER						
DC Gain		$GAIN_{CA}$		6		V/V
−3 dB Gain Bandwidth	(Note 7)	BW_{CA}		10		MHz
Input Common Mode Voltage Range	(Note 7)		−0.2		V_{CC}+0.1	V
Differential Input Voltage Range	(Note 7)		−60	–	60	mV
Input Bias Current	ISP,ISN = 2.5 V	I_{CS}	−100		100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to T_A = 25°C, Min and Max values are referenced to T_A from −40°C to 125°C. unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SWITCHING FREQUENCY						
Switching Frequency	Rfs = 2.7k Rfs = 5.1k Float Rfs = 8.2k Short to GND Rfs = 13k Rfs = 20k Rfs = 33k	F_{SW}	180 270 360 450 540 720 900 1080	200 300 400 500 600 800 1000 1200	220 330 440 550 660 880 1100 1320	kHz
Source Current		I_{FS}	45	50	55	µA
SYSTEM RESET TIME						
System Reset Time	Measured from EN to start of soft start with T_{DL} = 0 ms	T_{RST}	1.8	2.0	2.2	ms
DELAY TIME						
Delay Time	Float Rdl = 33k Rdl = 20k Rdl = 13k Rdl = 8.2k Rdl = 5.1k Rdl = 2.7k Short to GND (DLY1 Only) Short to GND (DDR Mode, DLY2 Only) (Note 7)	T_{DL}	– 0.9 1.8 2.7 3.6 7.2 10.8 18 –	0 1.0 2.0 3.0 4.0 8.0 12 20 T_{DL1}	– 1.1 2.2 3.3 4.4 8.8 13.2 22 –	ms
Source Current		I_{DL}	45	50	55	µA
SOFT START TIME						
Soft Start Time	OTP Configuration 1 (Note 7): Rss = 13k Float Rss = 20k Rss = 33k	T_{SS}	0.9 2.7 3.6 5.4	1.0 3.0 4.0 6.0	1.1 3.3 4.4 6.6	ms
	OTP Configuration 2 (Note 7): Rss = 2.7k Short to GND Rss = 5.1k Rss = 8.2k		0.9 2.7 3.6 5.4	1.0 3.0 4.0 6.0	1.1 3.3 4.4 6.6	
Source Current		I_{SS}	45	50	55	µA
CONFIGURATION						
PWM Configuration	(Note 7)	**Channel 1**			**Channel 2**	
	CNFG pin is Float	PWM1			PWM2	
	CNFG shorted to GND	PWM1, PWM2				
Source Current		I_{CNFG}	45	50	55	µA
PGOOD						
PGOOD Startup Delay	Measured from end of Soft Start to PGOOD assertion	T_{d_PGOOD}		100		µs
PGOOD Shutdown Delay	Measured from EN to PGOOD de−assertion			240		ns
PGOOD Low Voltage	I_{PGOOD} = 4 mA (sink)	V_{lPGOOD}	–	–	0.3	V
PGOOD Leakage Current	PGOOD = 5 V	$I_{lkgPGOOD}$	–	–	1.0	µA
FAULT						
FAULT Output High Voltage	I_{source} = 0.5 mA	V_{FAULT_H}	V_{CC}−0.5			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to T_A = 25°C, Min and Max values are referenced to T_A from −40°C to 125°C. unless other noted.)

Characteristics	Test Conditions		Symbol	Min	Typ	Max	Unit
FAULT							
FAULT Output Low Voltage	I_{sink} = 0.5 mA		V_{FAULT_L}			0.5	V
PROTECTIONS							
Positive Current Limit Threshold	Measured from ILIMT to GND	ISP−ISN = 50 mV	V_{OCTH+}	285	300	315	mV
		ISP−ISN = 20 mV		110	120	130	
Negative Current Limit Threshold	Measured from ILIMT to GND (only active in non−latched OVP)	ISP−ISN = −50 mV	V_{OCTH-}	285	300	315	mV
		ISP−ISN = −20 mV		110	120	130	
Positive Over Current Protection (OCP) Debounce Time	(Note 7)				8 Cycles		μs
Under Voltage Protection (UVP) Threshold	Voltage from FB to GND		V_{UVTH}	500	510	520	mV
Under Voltage Protection (UVP) Hysteresis	Voltage from FB to GND		V_{UVHYS}		20		mV
Under Voltage Protection (UVP) Debounce Time	(Note 7)				1.5		μs
Shutdown Time in Hiccup Mode	UVP (Note 7) OCP (Note 7) OTP (Note 7)				12*T_{SS} 16*T_{SS} 8*T_{SS}		ms
First−Level Over Voltage Protection (OVP_L) Threshold	Voltage from FB to GND		V_{OVTH_L}	650	660	670	mV
First−Level Over Voltage Protection (OVP_L) Hysteresis	Voltage from FB to GND		V_{LOVHYS}		−20		mV
First−Level Over Voltage Protection (OVP_L) Debounce Time	(Note 7)				1.0		μs
Second−Level Over Voltage Protection (OVP_H) Threshold	Voltage from FB to GND		V_{OVTH_H}	710	720	730	mV
Second−Level Over Voltage Protection (OVP_H) Hysteresis	Voltage from FB to GND		V_{HOVHYS}		−20		mV
Second−Level Over Voltage Protection (OVP_H) Debounce Time	(Note 7)				1.0		μs
Offset Voltage of OTP Comparator	V_{ILMT} = 200 mV		V_{OS_OTP}	−2		2	mV
OTP Source Current			I_{OTP}	9	10	11	μA
OTP Debounce Time	(Note 7)				160		ns
Thermal Shutdown (TSD) Threshold	(Note 7)		T_{sd}	140	165		°C
Recovery Temperature Threshold	(Note 7)		T_{rec}		125		°C
Thermal Shutdown (TSD) Debounce Time	(Note 7)				120		ns
ENABLE							
EN ON Threshold			V_{EN_TH}	0.75	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK		I_{EN_HYS}	25	30	35	μA
DRVON							
DRVON ON Threshold			V_{DRVON_TH}	0.75	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK		I_{DRVON_HYS}	25	30	35	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to T_A = 25°C, Min and Max values are referenced to T_A from −40°C to 125°C. unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
PWM MODULATION						
Minimum On Time	(Note 7)	T_{on_min}			50	ns
Minimum Off Time	(Note 7)	T_{off_min}	160			ns
0% Duty Cycle	COMP voltage when the PWM outputs remain Lo (Note 7)			1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI, V_{in} = 12.0 V (Note 7)			2.5		V
Ramp Feed−forward Voltage Range	(Note 7)		4.5		20	V
PWM OUTPUT						
PWM Output High Voltage	I_{source} = 0.5 mA	V_{PWM_H}	V_{CC}−0.2			V
PWM Output Low Voltage	I_{sink} = 0.5 mA	V_{PWM_L}			0.2	V
Rise and Fall Times	C_L (PCB) = 50 pF, measured between 10% & 90% of V_{CC} (Note 7)			10		ns
Leakage Current in Hi−Z Stage		I_{LK_PWM}	−1.0		1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

Table 4. RESISTOR OPTIONS FOR FUNCTION PROGRAMMING

Resistance Range (kΩ)			Resistor Options (kΩ)				
Min	**Typ**	**Max**	**±5%**	**±1%**			
2.565	2.7	2.835	2.7	2.61	2.67	2.74	2.80
4.845	5.1	5.355	5.1	4.87	4.99	5.11	5.23
7.79	8.2	8.61	8.2	7.87	8.06	8.25	8.45
12.35	13	13.65	13	12.4	12.7	13	13.3
19	20	21	20	19.1	19.6	20	20.5
31.35	33	34.65	33	31.6	32.4	33.2	34

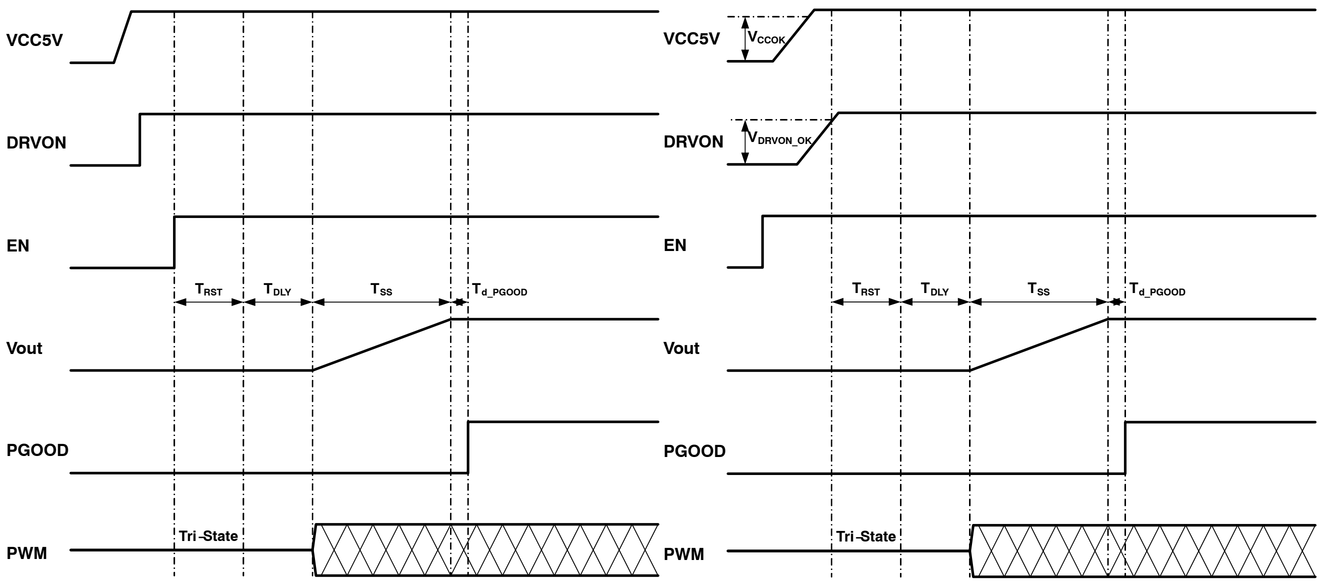
DETAILED DESCRIPTION

General

The NCP81234, a dual−channel/two−phase synchronous buck controller, provides flexible power management solutions for applications supported by DrMOS. Operating in high switching frequency up to 1.2 MHz allows employing small size inductor and capacitors.

Soft Start

The NCP81234 has a soft start function and the soft start time is externally programmed at SS pins. The output starts to ramp up following a system reset period T_{RST} and a programmable delay time T_{DLY} after the device is enabled and both VCC5V and DRVON are ready. The device is able to start up smoothly under an output pre−biased condition without discharging the output before ramping up.



(1) VCC5V and DRVON Ready before EN

(2) VCC5V and DRVON Ready after EN

Figure 5. Timing Diagrams of Power Up Sequence

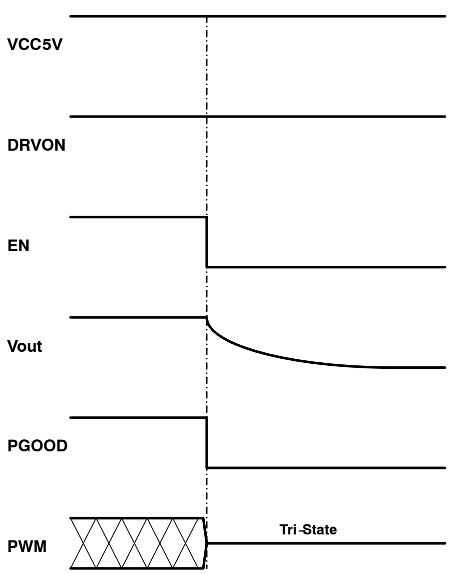


Figure 6. Timing Diagram of Power Down Sequence

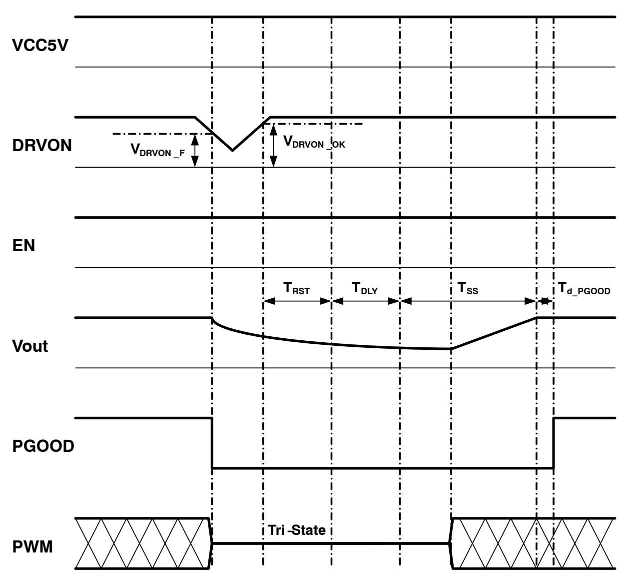


Figure 7. Timing Diagram of DRVON UVLO

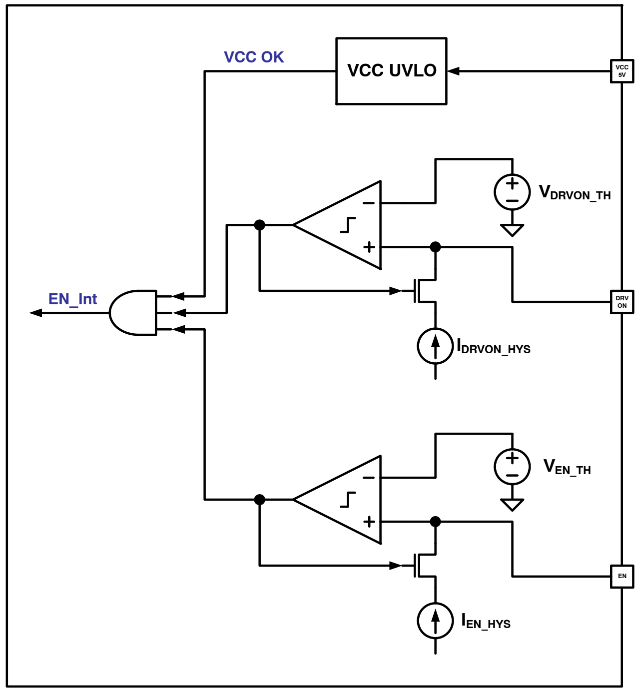


Figure 8. Enable, DRVON, and VCC UVLO

Enable and Input UVLO

The NCP81234 is enabled when the voltage at EN pin is higher than an internal threshold V_{EN_TH} = 0.8 V. A hysteresis can be programmed by an external resistor R_{EN} connected to EN pin as shown in Figure 9. The high threshold in ENABLE signal is

$$V_{EN\_H} = V_{EN\_TH} \quad \text{(eq. 1)}$$

The low threshold in ENABLE signal is

$$V_{EN\_L} = V_{EN\_TH} - V_{EN\_HYS} \quad \text{(eq. 2)}$$

The programmable hysteresis in ENABLE signal is

$$V_{EN\_HYS} = I_{EN\_HYS} \cdot R_{EN} \quad \text{(eq. 3)}$$

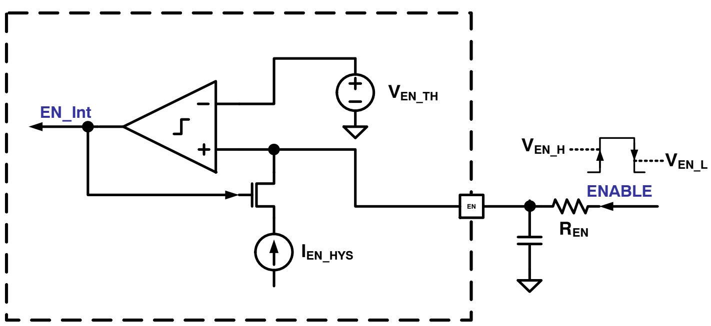


Figure 9. Enable and Hysteresis Programming

A UVLO function for input power supply can be implemented at EN pins. As shown in Figure 10, the UVLO threshold can be programmed by two external resistors.

$$V_{IN\_H} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \cdot V_{EN\_TH} \quad \text{(eq. 4)}$$

$$V_{IN\_L} = V_{IN\_H} - V_{IN\_HYS} \quad \text{(eq. 5)}$$

$$V_{IN\_HYS} = I_{EN\_HYS} \cdot R_{EN1} \quad \text{(eq. 6)}$$

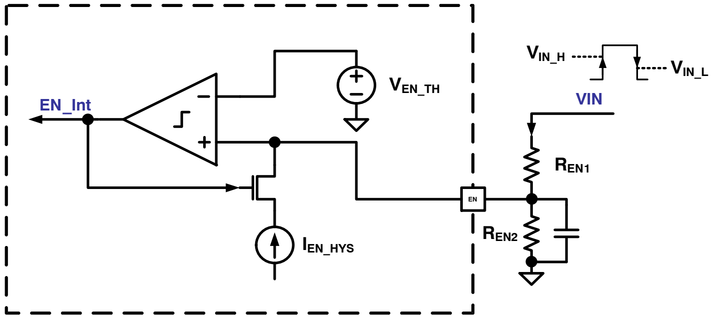


Figure 10. Enable and Input Supply UVLO Circuit

To avoid undefined operation, EN pins cannot be left float in applications.

DDR Mode Operation

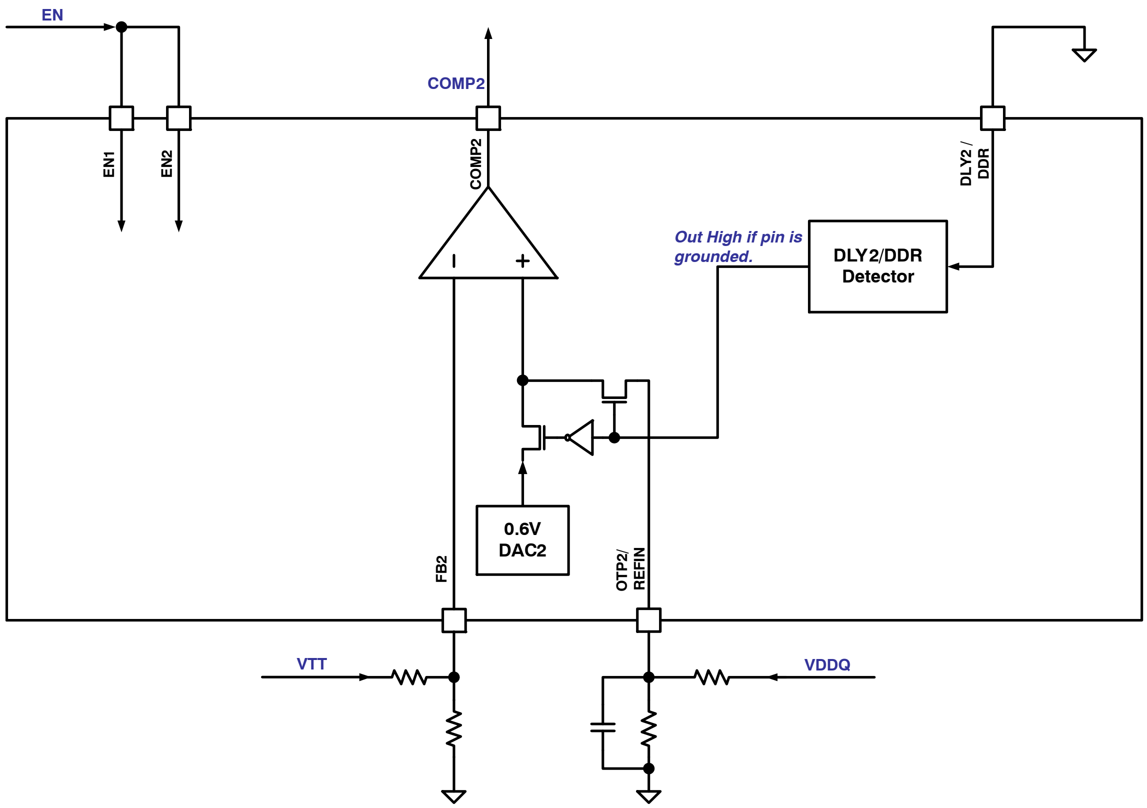


Figure 11. Block Diagram of DDR Mode Operation

As shown in Figure 11, if DLY2/DDR pin is shorted to GND before the device starts up, the NCP81234 is internally configured to operate in DDR mode. The two enable pins need to be connected together. The channel 1 provides power for VDDQ rail and the channel 2 provides power for VTT rail. The both channels have the same delay time programmed at DLY1 pin, and VTT rail always tracks with VDDQ/2. An external resistor divider, which is connected from VDDQ to GND, is employed to get 0.6 V at REFIN pin in steady−state operation. Another external resistor divider, which is connected from VTT to GND, is applied to obtain an expected VTT voltage considering FB2 voltage is 0.6 V as REFIN.

In DDR mode, two channels have independent fault detections and protections but have hiccup together if anyone of them needs to start a hiccup.

Over Voltage Protection (OVP)

A two−level recoverable over voltage protection is employed in the NCP81234, which is based on voltage detection at FB pin. If FB voltage is over V_{OVTH_L} (660 mV typical) for more than 1 μs, the first over voltage protection OVPL is triggered and PGOOD is pulled low. In the meanwhile, all the high−side MOSFETs are turned off and all the low−side MOSFETs are turned on. A negative current protection in low−side MOSFETs is active in this protection level, and it turns off low−side MOSFET for at least 50 ns if negative current is over the limit. However, in a worse case that FB voltage rises to be over V_{OVTH_H} (720 mV typical) for more than 1 μs, the second level over voltage protection OVPH takes in charge. As same as the first level OVP, all the high−side MOSFETs are turned off and all the low−side MOSFETs are turned on, but the negative current protection is disabled. The over voltage protection can be cleared once FB voltage drops 20 mV lower than V_{OVTH_L}, and then the system comes back to normal operation.

OVPH detection starts from the beginning of soft−start time T_{SS} and ends in shutdown and idle time of hiccup mode caused by other protections, while OVPL detection starts after PGOOD delay (T_{d_PGOOD}) is expired and ends at the same time as OVPH.

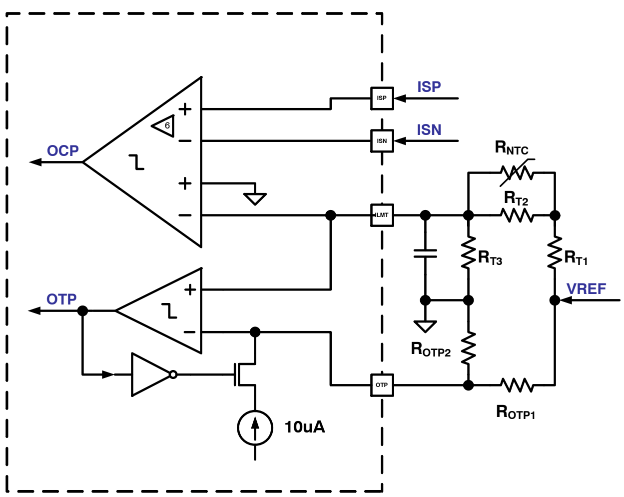
Under Voltage Protection (UVP)

The NCP81234 pulls PGOOD low and turns off both high−side and low−side MOSFETs once FB voltage drops below V_{UVTH} (540 mV typical) for more than 1.5 μs. Under voltage protection operates in a hiccup mode. A normal power up sequence happens after a hiccup interval.

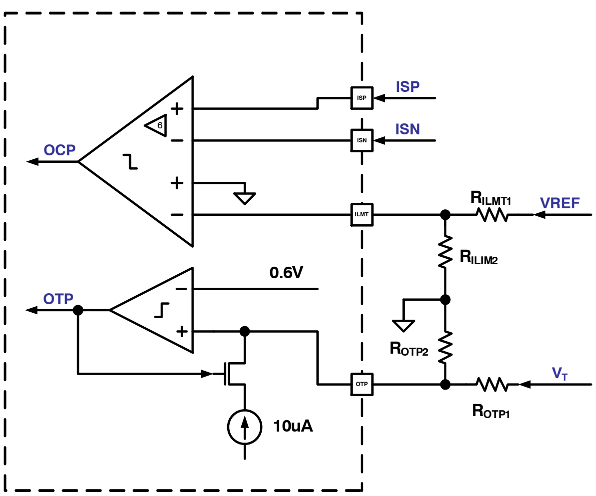
UVP detection starts when PGOOD delay (T_{d_PGOOD}) is expired right after a soft start, and ends in shutdown and idle time of hiccup mode.

Over Current Protection (OCP)

The NCP81234 senses phase currents by differential current sense amplifiers and provides a cycle−by−cycle over current protection for each phase. If OCP happens in all the phases of the same channel and lasts for more than 8 times of switching cycle, the channel shuts down and enters into a hiccup mode. The channel may enter into hiccup mode sooner due to the under voltage protection in a case if the output voltage drops down very fast.



(1) OTP Configuration 1



(2) OTP Configuration 2

Figure 12. Over−Current Protection and Over−Temperature Protection

The over−current threshold can be externally programmed at the ILIM pin for each channel. As shown in Figure 12 (1), a NTC resistor R_{NTC} can be employed for temperature compensated over current protection. The peak current limit per phase can be calculated by

$$V_{ISP} - V_{ISN} = \frac{1}{6} \cdot \frac{R_{T3}}{R_{T1} + \frac{R_{T2} \cdot R_{NTC}}{R_{T2} + R_{NTC}} + R_{T3}} \cdot V_{REF} \qquad \text{(eq. 7)}$$

If no temperature compensation is needed, as shown in Figure 12 (2), the peak current limit per phase can be simply set by

$$V_{ISP} - V_{ISN} = \frac{1}{6} \cdot \frac{R_{ILIM2}}{R_{ILIM1} + R_{ILIM2}} \cdot V_{REF} \qquad \text{(eq. 8)}$$

OCP detection starts from the beginning of soft−start time T_{SS}, and ends in shutdown and idle time of hiccup mode.

Over Temperature Protection (OTP)

The NCP81234 provides over temperature protection for each channel. To serve different types of DrMOS, one of two internal configurations of OTP detection can be selected at SS pin combined with a soft start time programming.

With OTP Configuration 1, as shown in Figure 12 (1), the NTC resistor R_{NTC} senses the hot−spot temperature and changes the voltage at ILMT pin. Both over−temperature threshold and hysteresis are externally programmed at OTP pin by a resistor divider. Once the voltage at ILMT pin is higher than the voltage at OTP pin, OTP trips and the channel is shut down. The channel will have a normal start up after a hiccup interval in condition that the temperature drops below the OTP reset threshold. The OTP assertion threshold V_{OTP} and reset threshold V_{OTP_RST} can be calculated by

$$V_{OTP} = \frac{V_{REF} + I_{OTP\_HYS} \cdot R_{OTP1}}{1 + \frac{R_{OTP1}}{R_{OTP2}}} \quad \text{(eq. 9)}$$

$$V_{OTP\_RST} = \frac{V_{REF} \cdot R_{OTP2}}{R_{OTP1} + R_{OTP2}} \quad \text{(eq. 10)}$$

The corresponding OTP temperature T_{OTP} and reset temperature T_{OTP_RST} can be calculated by

$$T_{OTP} = \frac{1}{\frac{\ln\left(R_{NTC\_OTP}/R_{NTC}\right)}{B} + \frac{1}{25+273.15}} - 273.15 \quad \text{(eq. 11)}$$

$$T_{OTP\_RST} = \frac{1}{\frac{\ln\left(R_{NTC\_OTPRST}/R_{NTC}\right)}{B} + \frac{1}{25+273.15}} - 273.15 \quad \text{(eq. 12)}$$

where

$$R_{NTC\_OTP} = \frac{1}{\frac{1}{R_{T\_OTP} - R_{T1}} - \frac{1}{R_{T2}}} \quad \text{(eq. 13)}$$

$$R_{NTC\_OTPRST} = \frac{1}{\frac{1}{R_{T\_OTPRST} - R_{T1}} - \frac{1}{R_{T2}}} \quad \text{(eq. 14)}$$

$$R_{T\_OTP} = \left(\frac{V_{REF}}{V_{OTP}} - 1\right) \cdot R_{T3} \quad \text{(eq. 15)}$$

$$R_{T\_OTPRST} = \left(\frac{V_{REF}}{V_{OTP\_RST}} - 1\right) \cdot R_{T3} \quad \text{(eq. 16)}$$

With OTP Configuration 2, as shown in Figure 12 (2), the NCP81234 receives an external signal V_T linearly representing temperature and compares to an internal 0.6 V reference voltage. If the voltage is over the threshold OTP happens. The OTP assertion threshold V_{OTP} and reset threshold V_{OTP_RST} in this configuration can be obtained by

$$V_{T\_OTP} = \left(1 + \frac{R_{OTP1}}{R_{OTP2}}\right) \cdot 0.6 \quad \text{(eq. 17)}$$

$$V_{T\_OTP\_RST} = \left(\frac{0.6}{R_{OTP2}} - I_{OTP\_HYS}\right) \cdot R_{OTP1} + 0.6 \quad \text{(eq. 18)}$$

OTP detection starts from the beginning of soft−start time T_{SS}, and ends in shutdown and idle time of hiccup mode.

Thermal Shutdown (TSD)

The NCP81234 has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds 165°C. TSD detection is activated when VCC5V and at least one of ENs are valid. Once the thermal protection is triggered, the whole chip shuts down and all PWM signals are in high impedance. If the temperature drops below 125°C, the system automatically recovers and a normal power sequence follows.

FAULT Indicator

The NCP81234 has a comprehensive fault indicator by means of a cycle−by−cycle fault signal output from FAULT pin. Figure 13 shows a typical timing diagram of FAULT signal. FAULT signal is composed of ALEART and two portions of fault flags for the two channels, having a total cycle period of 36 μs. A corresponding fault flag is asserted to high once the fault happens. The periodic fault signal starts from the point where any fault has been confirmed and ends after PGOOD is asserted again. Note the last FAULT cycle has to be complete after PGOOD assertion.

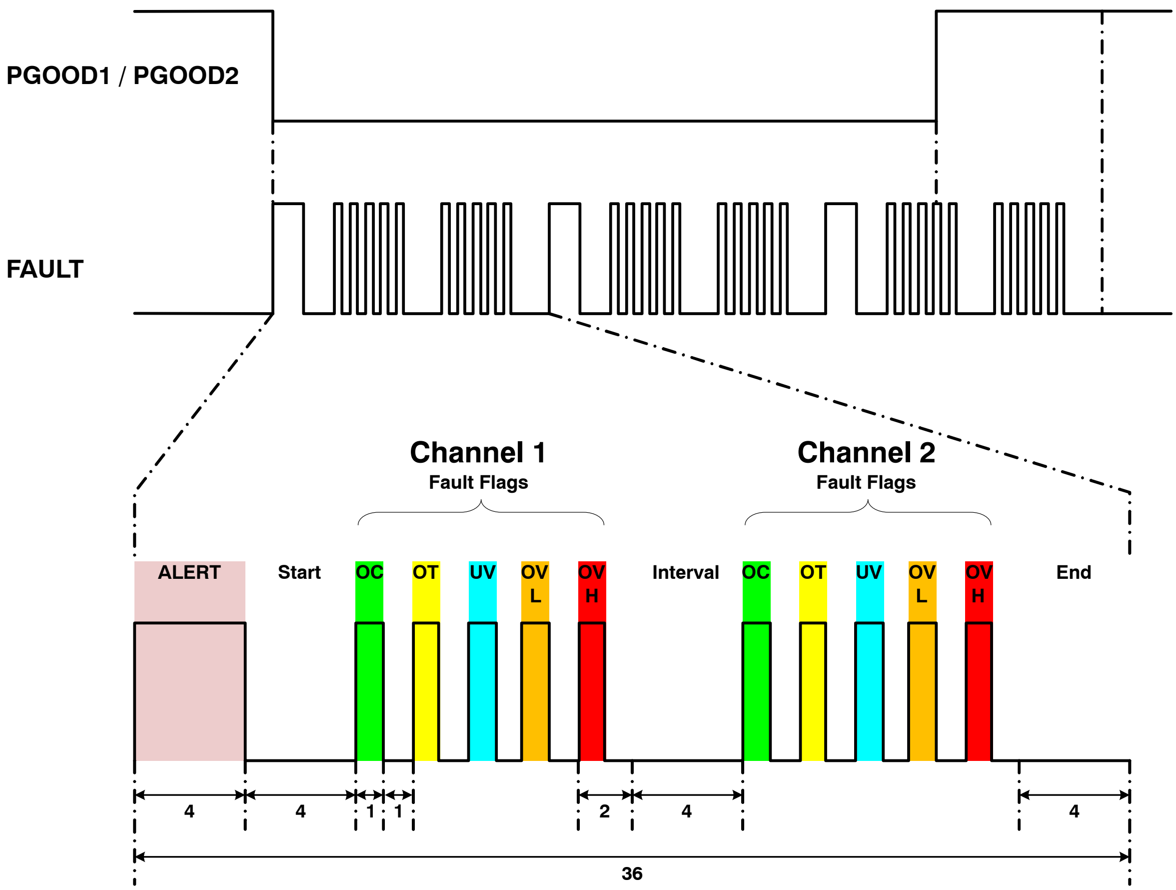


Figure 13. Timing Diagram of FAULT Signal

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- **Power Paths:** Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) in power stages to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling:** The devices should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to VIN and PGND pins.
- **VCC Decoupling:** Place decoupling caps as close as possible to VCC5V pin of the NCP81234 and VCCP pins of DrMOS.
- **Switching Node:** Each SW node in power stages should be a copper pour, but compact because it is also a noise source.
- **Bootstrap:** The bootstrap cap and an option resistor per phase need to be very close and directly connected between bootstrap pin and SW pin of DrMOS.
- **Ground:** It would be good to have separated ground planes for power ground PGND and analog ground GND and connect the two planes at one point.
- **Voltage Sense:** Connect the FB pin through the RC compensation network to V_{OUT}. It is best to place the RC components close to the controller, then establish a single, quiet connection to the V_{OUT} regulation point, avoiding noisy PWM and switching signals.
- **Current Sense:** Use Kelvin sense pair and arrange a "quiet" path for the differential current sense per phase. Careful layout for current sensing is critical for jitter minimization, accurate current limiting, and good current balance. The current−sense filter capacitors and resistors should be close to the controller. The temperature compensating thermistor should be placed as close as possible to the inductor. The wiring path should be kept as short as possible but well away from the switch nodes.
- **Compensation Network:** The small feedback capacitor from COMP to FB should be as close to the controller as possible. Keep the FB traces short to minimize their capacitance to ground.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around DrMOS and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the DrMOS, thus the heat sources are decentralized.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊