ON Semiconductor

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Three-Rail Controller with SVID Interface for IMVP8 CPU Applications

NCP81218P

The NCP81218P contains a two−phase, and two single−phase buck regulator controllers optimized for Intel IMVP8 compatible CPUs.

The two−phase controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for IMVP8 CPU Core or GT rails.

The two single−phase controllers can be used for Core, GT, SA or GTUS rails. Both make use of ON Semiconductor's patented high performance RPM operation. RPM control maximizes transient response while allowing smooth transitions between discontinuous frequency scaling operation and continuous mode full power operation. The single−phase rails have a low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

Features Common to All Rails

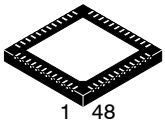
- Vin Range 4.5 V to 25 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot (except SA rail)
- High Impedance Differential Output Voltage Amplifiers
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 200 kHz –1.2 MHz
- Digitally Stabilized Switching Frequency
- UltraSonic Operation

Two−phase Rail Features

- Supports SVID Addresses 00 and 01
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Accurate Total Summing Current Amplifier
- Phase−to−Phase Dynamic Current Balancing
- Power Saving Phase Shedding

ON Semiconductor®

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QFN48
CASE 485BA

MARKING DIAGRAM



F = Wafer Fab Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NCP81218PMNTXG	QFN48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Single−phase Rail Features

- Supports SVID Addresses 00, 01, 02 and 03
- High performance RPM control system
- Low Offset IOUT monitor
- Zero Droop Capable

Other Features

- PSYS Input Monitor (SVID address 0D)
- Thermal Monitors for addresses 00, 01, and 03
- This is a Pb−Free Device

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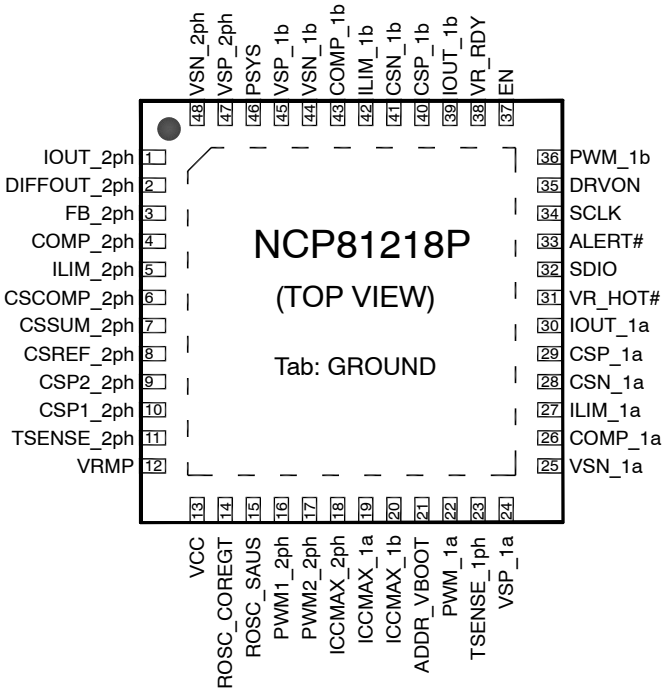


Figure 1.

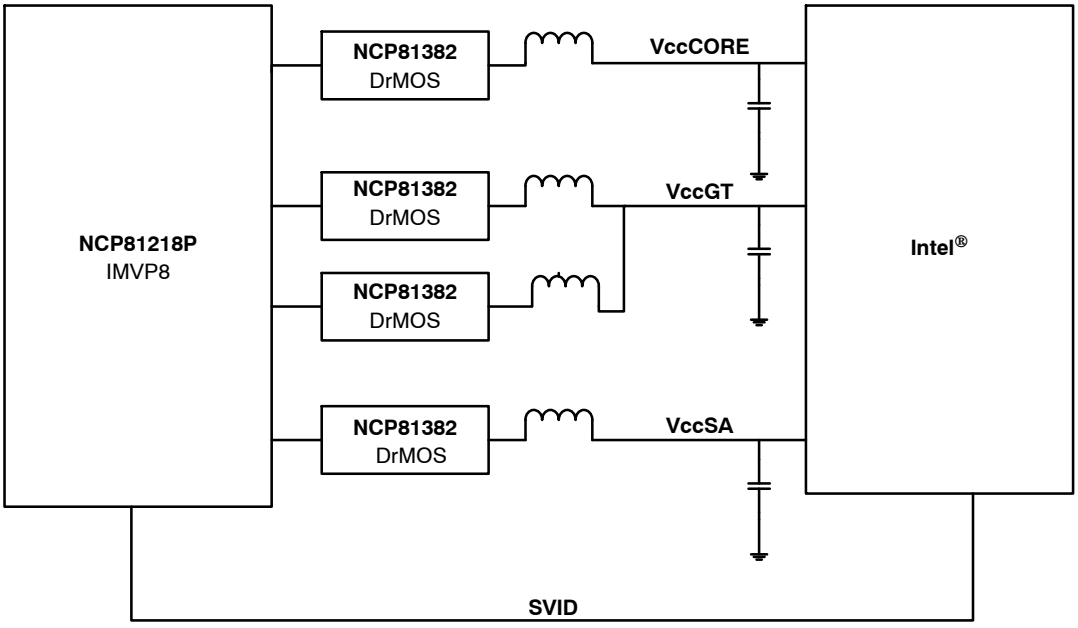


Figure 2. Typical DrMOS Application Diagram

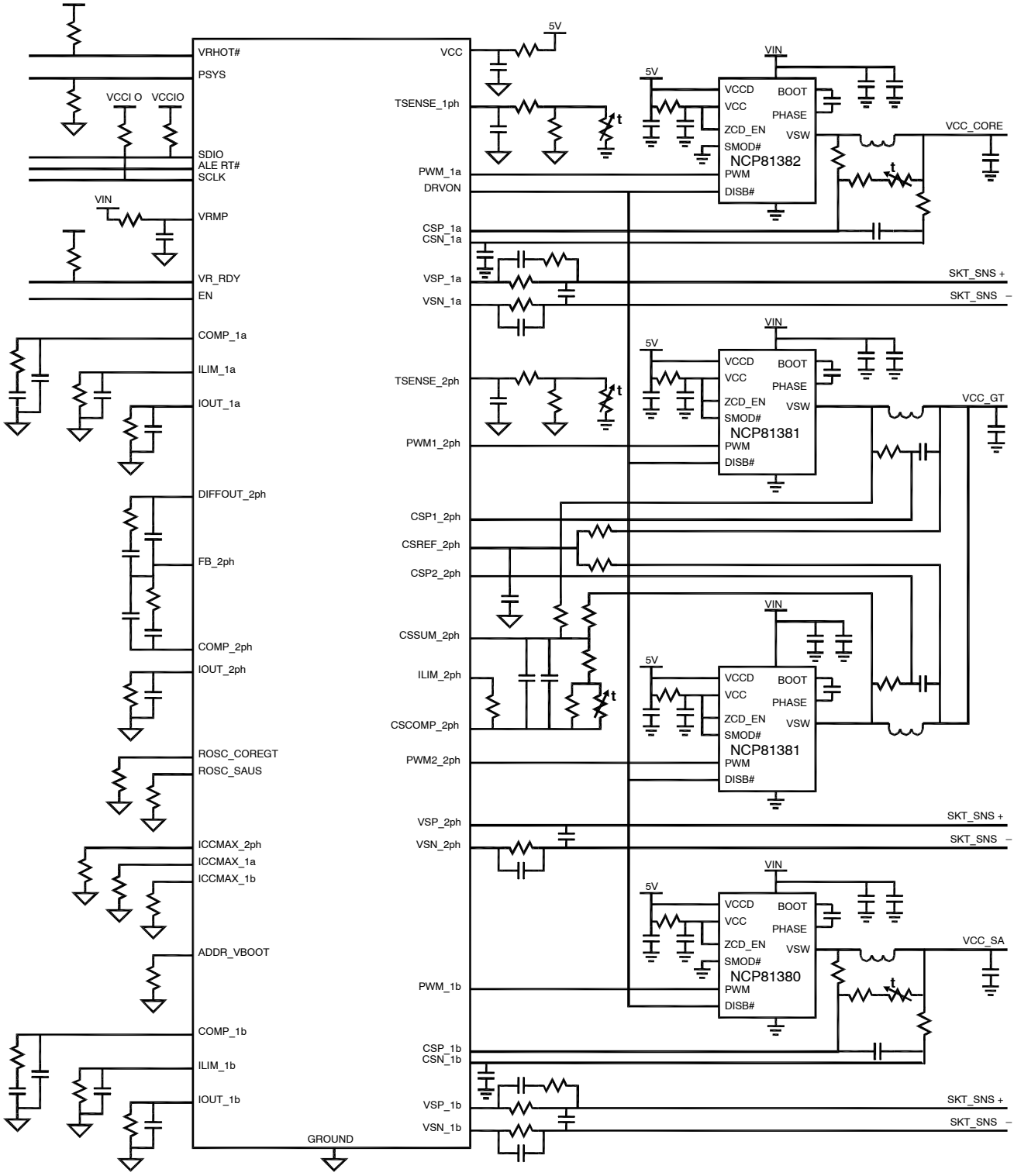


Figure 3. Application Schematic

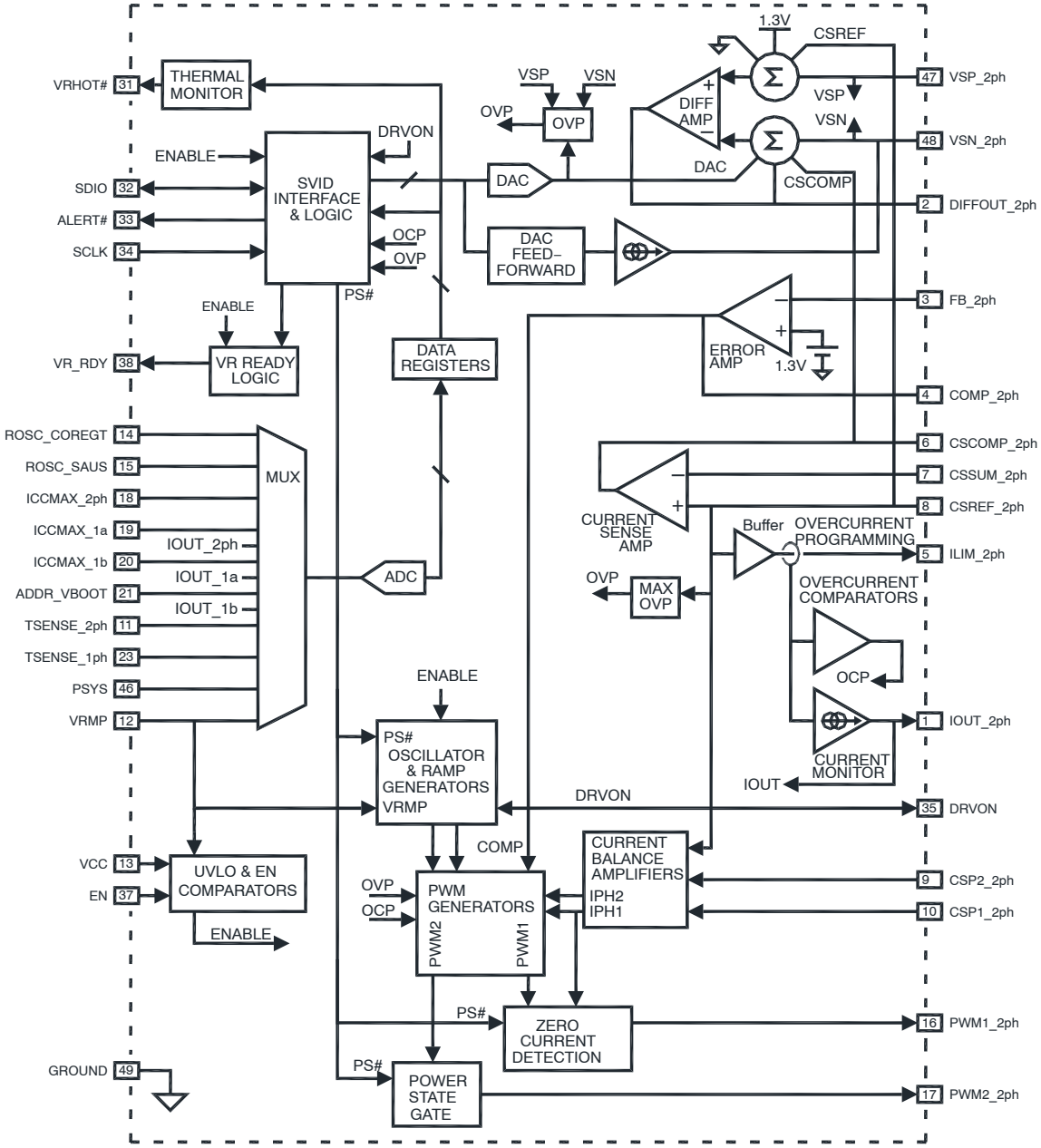


Figure 4. 2−Phase Rail Block Diagram

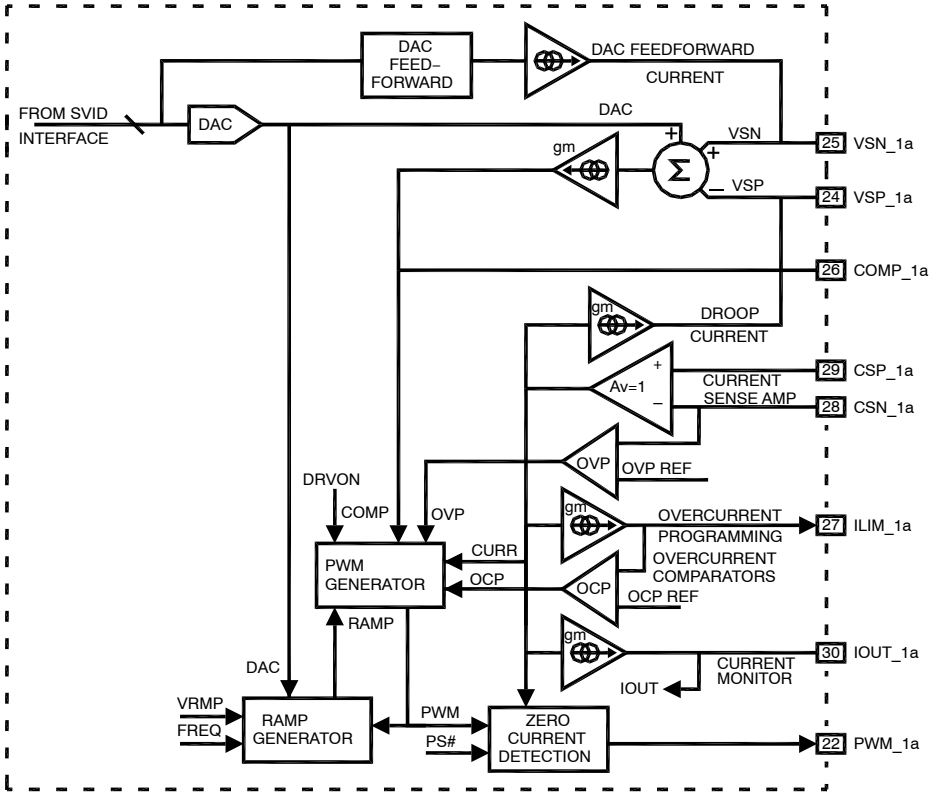


Figure 5. Single Phase “a” Block Diagram

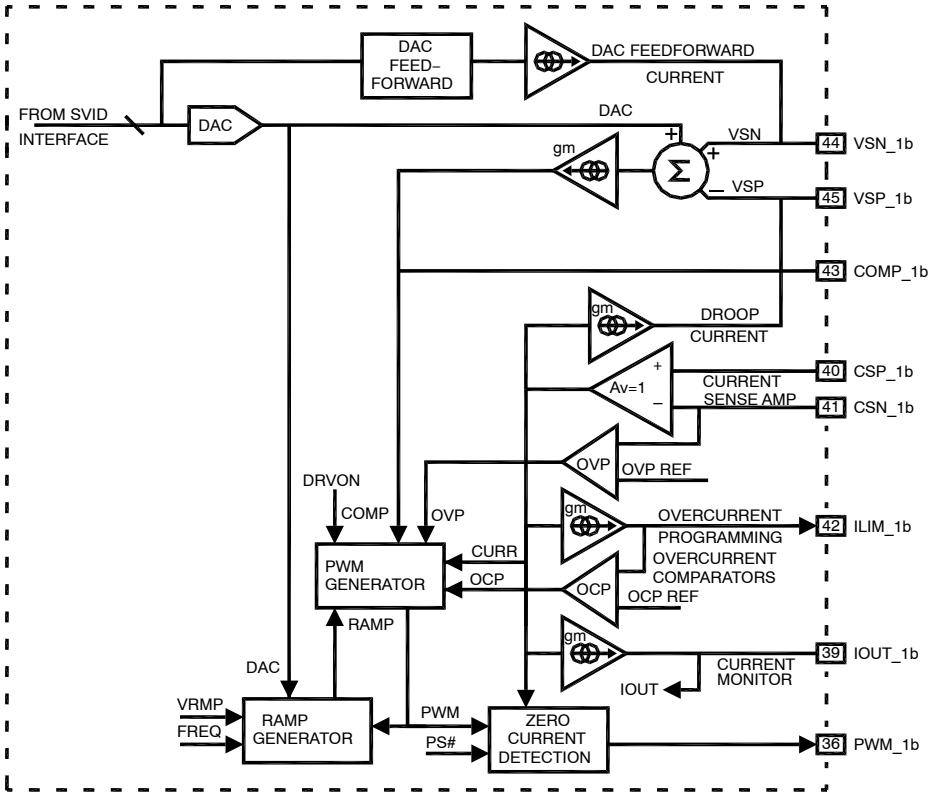


Figure 6. Single Phase “b” Block Diagram

NCP81218P PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	IOUT_2ph	IOUT gain programming pin for the 2−phase regulator
2	DIFFOUT_2ph	Output of the 2−phase regulator's output differential remote sense amplifier
3	FB_2ph	Error amplifier voltage feedback input for the 2−phase regulator
4	COMP_2ph	Output of the error amplifier and the inverting inputs of PWM comparators for the two−phase regulator
5	ILIM_2ph	Over−current monitor input for the 2−phase regulator −− programmed with a resistor to CSCOMP_2ph
6	CSCOMP_2ph	Output of total−current−sense amplifier for the 2−phase regulator
7	CSSUM_2ph	Inverting input of total−current−sense amplifier for the 2−phase regulator
8	CSREF_2ph	Total−current−sense amplifier reference voltage input for the 2−phase regulator
9	CSP2_2ph	Non−inverting input to 2−phase regulator Phase 2 current−balance amplifier
10	CSP1_2ph	Non−inverting input to 2−phase regulator Phase 1 current−balance amplifier
11	TSENSE_2ph	Temperature sense input for the 2−phase regulator (see Rail Configuration Table)
12	VRMP	VIN Feed−forward input for compensating modulator ramp−slopes. The current fed into this pin is used to control the ramp of the PWM slopes. Also, the input monitoring VIN for undervoltage (UVLO)
13	VCC	Power for the internal control circuits. A decoupling capacitor must be connected from this pin to ground
14	ROSC_COREGT	Switching frequency program input for rails configured as Core and GT
15	ROSC_SAUS	Switching frequency program input for the 1−phase rail configured as SA
16	PWM1_2ph	2−phase regulator Phase 1 PWM output
17	PWM2_2ph	2−phase regulator Phase 2 PWM output
18	ICCMAX_2ph	During startup, the IccMax of the 2−phase regulator is programmed by a pull−down resistor on this pin
19	ICCMAX_1a	During startup, the ICCMAX of 1−phase Regulator 1a is programmed by a pulldown resistor on this pin
20	ICCMAX_1b	During startup, the ICCMAX of 1−phase Regulator 1b is programmed by a pulldown resistor on this pin
21	ADDR_VBOOT	During startup, a resistor to GND programs SVID addresses and VBOOT options for all three rails
22	PWM_1a	1−phase regulator 1a PWM output
23	TSENSE_1ph	Temperature sense input for 1−phase regulator. (see Rail Configuration Table)
24	VSP_1a	Positive input of 1−phase regulator 1a differential output voltage sense amplifier
25	VSN_1a	Negative input of 1−phase regulator 1a differential output voltage sense amplifier
26	COMP_1a	Compensation for 1−phase regulator 1a
27	ILIM_1a	Current−limit for 1−phase regulator 1a is programmed by a pull−down resistor on this pin
28	CSN_1a	Negative input of 1−phase regulator 1a differential current sense amplifier
29	CSP_1a	Positive input of 1−phase regulator 1a differential current sense amplifier Pull this pin to VCC to disable 1−phase regulator 1a
30	IOUT_1a	IOUT gain programming pin for 1−phase regulator 1a
31	VR_HOT#	Open drain output for an over−temperature condition detected on any TSENSE input
32	SDIO	Serial VID data interface
33	ALERT#	Serial VID ALERT#
34	SCLK	Serial VID clock
35	DRVON	Enable output for external discrete FET drivers and/or ON Semiconductor DrMOS.
36	PWM1b	1−phase regulator 1b PWM output

NCP81218P PIN DESCRIPTIONS

Pin No.	Symbol	Description
37	EN	Enable. High activates all configured rails
38	VR_RDY	Open drain output. High indicates all three rails are ready to accept SVID commands
39	IOUT_1b	IOUT gain programming pin for 1−phase regulator 1b
40	CSP_1b	Positive input of 1−phase regulator 1b differential current sense amplifier Pull this pin to VCC to disable 1−phase regulator 1b
41	CSN_1b	Negative input of 1−phase regulator 1b differential current sense amplifier
42	ILIM_1b	Current−limit for 1−phase regulator 1b is programmed by a pull−down resistor on this pin
43	COMP_1b	Compensation for 1−phase regulator 1b
44	VSN_1b	Negative input of 1−phase regulator 1b differential output voltage sense amplifier
45	VSP_1b	Positive input of 1−phase regulator 1b differential output voltage sense amplifier
46	PSYS	System power signal input. Resistor to ground needed for scaling. When the NCP81218P is configured with a GTUS rail, this input is a temperature monitor. (see Rail Configuration Table)
47	VSP_2ph	Positive input of 2−phase regulator differential output voltage sense amplifier
48	VSN−2ph	Negative input of 2−phase regulator differential output voltage sense amplifier

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Pin Voltage Range (Note 1)	VSN_x	−0.3	+0.3	V
Pin Voltage Range (Note 1)	VCC	−0.3	6.5	V
Pin Voltage Range (Note 1)	IOUT_x	−0.3	2.5	V
Pin Voltage Range (Note 1)	VRMP	−0.3	+25	V
Pin Voltage Range (Note 1)	All Other Pins	−0.3	VCC + 0.3	V
Junction Temperature	$T_{J(max)}$		125	°C
Operating Ambient Temperature Range	$T_{A(OP)}$	−10	100	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Moisture Sensitivity Level QFN Package	MSL	1		−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
4. Pin ratings referenced to VCC apply with VCC at any voltage within the VCC Pin Voltage Range.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristic QFN Package (Note 5)	$R_{\theta JA}$	68	°C/W
Thermal Characteristic QFN Package (Note 5)	$R_{\theta JC}$	8	°C/W

5. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM

ELECTRICAL CHARACTERISTICS – ELEMENTS COMMON TO SINGLE & 2−PHASE RAILS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC INPUT SUPPLY						
Supply Voltage Range			4.75		5.25	V
Quiescent Current		EN = high, PS0,1,2 Mode, T_A = 100°C		28	32	mA
		EN=high, all rails PS3 Mode, T_A = 25°C		22	28	mA
		EN = high, all rails PS4, T_A = 25°C		155	175	μA
		EN = low, T_A = 25°C		30	50	μA
UVLO Threshold		VCC rising			4.5	V
		VCC falling	4			V
UVLO Hysteresis (Note 6)			180	290		mV
VRMP						
UVLO Threshold		VRMP Rising		3.95	4.25	V
		VRMP Falling	3	3.24		V
UVLO Hysteresis (Note 6)			500	710		mV
Ramp Feed−forward Control Range		Range in which the ramp slope is affected by VRMP voltage	5		20	V
ENABLE INPUT						
Enable High Input Leakage Current		External 1k pull−up to 3.3 V	−		1.0	μA
Activation Level		V_{UPPER}	0.8			V
Deactivation Level		V_{LOWER}			0.3	V
Total Hysteresis (Note 6)		$V_{RISING} - V_{FALLING}$		295		mV
Enable Delay Time − Rising		Time from Enable transitioning HIGH to DRVON going HIGH	1.0	2.1	2.5	ms
Enable Delay Time − Falling (Note 6)		Time from Enable transitioning LOW to DRVON below 0.8 V		190		ns
PHASE DETECTION						
CSP Pin Pulldown Current (Note 6)		Pulldown applied only prior to softstart		20		μA
CSP Pin Threshold voltage			4.5			V
Phase Detect Timer (Note 6)				1.8		ms
IMVP8 DAC						
System Voltage Accuracy		0.75 V ≤ DAC ≤ 1.52 V 0.5 V≤ DAC ≤ 0.745 V 0.25 V ≤ DAC ≤ 0.495 V	−0.5 −8 −10		0.5 8 +10	% mV mV

ELECTRICAL CHARACTERISTICS – ELEMENTS COMMON TO SINGLE & 2−PHASE RAILS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DAC SLEW RATE						
Soft Start Slew Rate				15		mV/μs
Slew Rate Slow				15		mV/μs
Slew Rate Fast				30		mV/μs
DRVON						
Output High Voltage		Sourcing 500 μA	3.0			V
Output Low Voltage		Sinking 500 μA			0.1	V
Rise Time		CL (PCB) = 20 pF, ΔVo = 10% to 90%	−	150		ns
Fall Time				2.5		
Internal Pull Up Resistance				2.5		kΩ
Internal Pull Down Resistance		EN = Low		50		kΩ
PWM OUTPUTS						
Output High Voltage		Sourcing 500 μA	VCC− 0.2V	−	−	V
Output Mid Voltage		PS2, No Load	1.7	1.8	1.9	V
Output Low Voltage		Sinking 500 μA	−	−	0.7	V
Rise and Fall Time (Note 6)		CL (PCB) = 50 pF, ΔVo = 10% to 90%	−	8		ns
VR_RDY OUTPUT						
Output Low Saturation Voltage		I_{VR_RDY} = 4 mA	−	−	0.3	V
Rise Time		External pull−up of 1 kΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 10% to 90%	−	120	150	ns
Fall Time		External pull−up of 1 kΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 90% to 10%	−	25	150	ns
Output Leakage Current When High		VR_RDY= 5.0 V	−1.0	−	1.0	μA
VR_RDY Delay (rising)		En rising to VR_RDY rising (TA)	−	−	2.5	ms
VR_RDY Delay (falling)		En falling to VR_RDY falling (TD+TE)	−	−	1.5	μs
VR_HOT#						
Output Low Voltage		I_{VRHOT} = 4 mA			0.3	V
Output Leakage Current		High Impedance State	−1.0	−	1.0	μA
ADC						
Linear Input Voltage Range			0		2.00	V
Differential Nonlinearity (DNL)		Highest 8−bits			1	LSB
Conversion Time				7.4		μs
Conversion Rate				136		kHz
Total Unadjusted Error (TUE)			−1.25		+1.25	%
Power Supply Sensitivity				±1		%
Round Robin Time				59		μs
SCLK, SDIO						
Input Low Voltage	V_{IL}				0.45	V

ELECTRICAL CHARACTERISTICS – ELEMENTS COMMON TO SINGLE & 2−PHASE RAILS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK, SDIO						
Input High Voltage	V_{IH}		0.65			V
Output High Voltage (SDIO only)	V_{OH}	Pullup resistor supply voltage		1.05		V
Pulldown Resistance (SDIO only)	R_{ON}		2.5		13	Ω
Leakage Current			−100		100	μA
Pad + Pin Capacitance (Note 6)					9.0	pF
VR clock to data delay (Note 6)	T_{CO}		4		8.3	ns
Setup time (Note 6)	T_{SU}		7			ns
Hold time (Note 6)	T_{HLD}		14			ns
ALERT PIN						
Output High Voltage	V_{OH}	Pullup resistor supply voltage		1.05		V
Pulldown Resistance	R_{ON}		2.5		13	Ω
Leakage Current			−100		100	μA
Pad + Pin Capacitance (Note 6)					9.0	pF
ICCMAX PINS (all)						
Full Scale Input Voltage (Note 6)				2.00		V
PSYS PIN						
Domain Detection Pulldown Current (Note 6)		Applied only after enabling, and prior to soft−start.		10		μA
Full Scale Input Voltage (Note 6)				2.00		V
ADC Resolution (Note 6)				7.8		mV
Register Update Time (Note 6)					500	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design or characterization data. Not tested in production.

ELECTRICAL CHARACTERISTICS – TWO PHASE REGULATOR (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC}=0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DIFFERENTIAL SUMMING AMPLIFIER						
Input Bias Current – VSP		VSP = 1.3 V	−1	–	1	μA
Input Bias Current – VSN		VSN = 0 V	−25	–	25	nA
VSP Input Voltage Range			−0.3	–	3.0	V
VSN Input Voltage Range			−0.3	–	0.3	V
−3 dB Bandwidth (Note 7)		CL = 20 pF to GND, RL = 10 kΩ to GND		18		MHz
Closed Loop DC gain		V_{VSP} − V_{VSN} = 0.5 to 1.3 V		1.0		V/V
ERROR AMPLIFIER						
Input Bias Current		V_{FB} = 1.3 V	−400		400	nA
Open Loop DC Gain (Note 7)		CL = 20 pF to GND, RL = 10 kΩ to GND		80		dB
Open Loop Unity Gain Bandwidth (Note 7)		CL = 20 pF to GND, RL = 10 kΩ to GND		20		MHz
Slew Rate (Note 7)		ΔVin = 100 mV, G = −10V/V, ΔVout = 1.5 V − 2.5V, CL = 20 pF to GND, DC Load = 10k to GND		30		V/μs
Maximum Output Voltage		I_{SOURCE} = 2.0 mA	3.5	–	–	V
Minimum Output Voltage		I_{SINK} = 2.0 mA	–	–	1	V
CURRENT SUMMING AMPLIFIER						
Offset Voltage (Note 7)	V_{OS}		−300		300	μV
Input Bias Current		V_{CSSUM} = V_{CSREF} = 1 V	−7.5		7.5	nA
Open Loop Gain (Note 7)				80		dB
Unity Gain Bandwidth (Note 7)		C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
Maximum CSCOMP Output Voltage		Isource = 2 mA	3.5			V
Minimum CSCOMP Output Voltage		Isink = 500 μA			100	mV
		Isink = 25 μA		7	30	mV
CURRENT BALANCE AMPLIFIERS						
Input Bias Current		V_{CSP1} = V_{CSP2} = V_{CSREF} = 1.2 V	−50	–	50	nA
Common Mode Input Voltage Range		V_{CSP1} = V_{CSP2} = V_{CSREF}	0	–	2.3	V
Differential Input Voltage Range		V_{CSREF} = 1.2 V	−100	–	100	mV
Input Offset Voltage Matching		V_{CSP1} = V_{CSP2} = V_{CSREF} = 1.2 V Deviation from average offset	−1.5	–	1.5	mV
Current Sense Amplifier Gain		0 V < V_{CSPX} − V_{CSREF} < 0.1 V	5.7	6.0	6.3	V/V
Current Sense Gain Matching		10 mV < V_{CSPX} − V_{CSREF} < 30 mV	−3		3	%
−3 dB Bandwidth (Note 7)				8		MHz
IOUT OUTPUT						
Input Referred Offset Voltage		ILIM to CSREF	−1.5		1.5	mV
Output Source Current		ILIM sink current = 20 μA	190			μA

ELECTRICAL CHARACTERISTICS – TWO PHASE REGULATOR (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC}=0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IOUT OUTPUT						
Current Gain		I_{IOUT} / I_{ILIM}; R_{ILIM} = 20k, R_{IOUT} = 5.0k , DAC = 0.8 V, 1.25 V, 1.52V	9.5	10	10.5	μA/μA
OVERCURRENT PROTECTION						
ILIM Threshold Current (delayed OCP shutdown)	I_{CL0}	PS0	9.0	10	11	μA
	I_{CL1}	PS1, PS2, and PS3		6.7		μA
ILIM Threshold Current (immediate OCP shutdown)	I_{CLM0}	PS0	13.5	15	16.5	μA
	I_{CLM1}	PS1, PS2, and PS3		10		μA
Shutdown Delay (immediate)				300		ns
Shutdown Delay (delayed)	t_{OCPDLY}			50		μs
ILIM Offset Voltage		V_{ILIM} − V_{CSREF}; ILIM sourcing 15 μA	−2		2	mV
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)						
Absolute Over Voltage Threshold	V_{OVABS2}	CSREF voltage during softstart		2		V
Over Voltage Threshold Above DAC	V_{OVP2}	V_{VSP} − V_{VSN} − VID rising	370		430	mV
Over Voltage Delay (Note 7)		V_{VSP} − V_{VSN} rising to PWM low		25		ns
Under Voltage	V_{UVM}	V_{VSP} − V_{VSN} − VID falling	−370	−295	−225	mV
Under−voltage Delay (Note 7)		V_{VSP} − V_{VSN} falling to VR_RDY falling		5		μs
OSCILLATOR						
Switching Frequency Range			200	–	1200	kHz
MODULATORS (PWM Comparators)						
0% Duty Cycle		COMP voltage when the PWM outputs remain LO		1.3	–	V
100% Duty Cycle		COMP voltage when the PWM outputs remain HI VRMP = 12.0 V	–	2.5	–	V
PWM Phase Angle Error				±15		deg
TSENSE_2ph						
Alert# Assert Threshold		25°C to 100°C		488		mV
Alert# De−assert Threshold		25°C to 100°C		510		mV
VRHOT Assert Threshold		25°C to 100°C		469		mV
VRHOT Rising Threshold		25°C to 100°C		489		mV
Bias Current		25°C to 100°C	116	120	124	μA
ICCMAX PIN						
Bias Current	$I_{MXBIAS2}$	Applied only after enabling, and prior to softstart.	9.63	9.98	10.32	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design or characterization data. Not tested in production.

ELECTRICAL CHARACTERISTICS – SINGLE PHASE REGULATORS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Input Bias Current		VSP – see DROOP OUTPUT	–	–	–	
		VSN	−25	–	25	nA
VSP Input Voltage Range			−0.3	–	3.0	V
VSN Input Voltage Range			−0.3	–	0.3	V
Gain	gm_{EA}		1.34	1.6	1.86	mS
Input Offset			−500		500	μV
Open loop Gain (Note 8)		Load = 1 nF in series with 1 kΩ in parallel with 10 pF to ground		73		dB
Source Current		Input Differential −200 mV		200		μA
Sink Current		Input Differential 200 mV		200		μA
−3dB Bandwidth (Note 8)		Load = 1 nF in series with 1 kΩ in parallel with 10 pF to ground		15		MHz
CURRENT SENSE AMPLIFIER						
Input Bias Current		V_{CSP} = V_{CSN} = 1.2 V	−50	–	50	nA
Common Mode Input Range (Note 8)		V_{CSP} = V_{CSN}	0	–	2.0	V
Common Mode Rejection		V_{CSP} = V_{CSN} = 0.5 V to 1.2 V	60	80	–	dB
Differential Input Voltage Range (Note 8)		V_{CSN} = 1.2 V	−70	–	70	mV
−3dB Bandwidth (Note 8)				6		MHz
IOUT						
Gain	gm_{IOUT}	0 mV ≤ V_{CSP} − V_{CSN} ≤ 25 mV; 25°C	0.965	1.0	1.035	mS
Output Offset Current		0 ≤ V_{IOUT} ≤ 2 V	−250		250	nA
Maximum Output Current (Note 8)		0 ≤ V_{IOUT} ≤ 2 V	70			μA
Maximum Output Voltage (Note 8)		I_{IOUT} = −100 μA	2.1			V
DROOP OUTPUT (VSP PIN)						
Gain	gm_{VSP}	0 V ≤ V_{CSP} − V_{CSN} ≤ 0.1 V	0.96	1.0	1.04	mS
Output Offset Current		0.5 ≤ V_{VSP} ≤ 1.2 V	−900		900	nA
Maximum Output Current (Note 8)		0 ≤ V_{VSP} ≤ 1.8 V	70			μA
Output Voltage Range (Note 8)		I_{VSP} = −100 μA	1.8			V
OVERCURRENT PROTECTION (ILIM PIN)						
Gain	gm_{ILIM}	18 mV ≤ V_{CSP} − V_{CSN} ≤ 50 mV	0.90	1.0	1.08	mS
Output Offset Current		V_{ILIM} = 1.3 V	−1.0		1.0	μA
Maximum Output Current (Note 8)		0 ≤ V_{ILIM} ≤ 1.3 V	70			μA
Maximum Output Voltage (Note 8)		I_{ILIM} = −100 μA	1.4			V
Activation Threshold Voltage	V_{CL}		1.275	1.3	1.325	V
Activation Delay (Note 8)				250		ns
OSCILLATOR						
Switching Frequency Range			200	–	1200	kHz
ZCD COMPARATOR						
Offset Accuracy (Note 8)		Referred to V_{CSP} − V_{CSN}		±1.5		mV

ELECTRICAL CHARACTERISTICS – SINGLE PHASE REGULATORS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)						
Over Voltage Threshold	V_{OVP1}	V_{VSP} – V_{VSN} – VID rising	370		430	mV
Absolute Over Voltage Threshold	V_{OVABS1}	CSN voltage during soft−start		2		V
Over Voltage Delay (Note 8)		V_{VSP} rising to PWM low		25		ns
Over Voltage VR_RDY Delay (Note 8)		V_{VSP} rising to VR_RDY low		350		ns
Under Voltage Threshold	V_{UVM1}	V_{VSP} – V_{VSN} – VID falling	−370	−295	−225	mV
Under−voltage Hysteresis (Note 8)				25		mV
Under−voltage Blanking Delay (Note 8)		V_{VSP} – V_{VSN} falling to VR_RDY falling		5		μs
TSENSE_1ph						
Alert# Assert Threshold		25°C to 100°C		490		mV
Alert# De−assert Threshold		25°C to 100°C		502		mV
VRHOT Assert Threshold		25°C to 100°C		476		mV
VRHOT Rising Threshold		25°C to 100°C		480		mV
Bias Current		25°C to 100°C	116	120	124	μA
ICCMAX PINS						
Bias Current (Note 8)	$I_{MXBIAS1A}$	Applied only after enabling, and prior to soft−start.	9.63	9.98	10.33	μA
	$I_{MXBIAS1B}$		9.53	9.94	10.33	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design or characterization data. Not tested in production.

IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	0	00	0	0	1	1	0	0	0	0	0.485	30
0	0	0	0	0	0	0	1	0.25	01	0	0	1	1	0	0	0	1	0.49	31
0	0	0	0	0	0	1	0	0.255	02	0	0	1	1	0	0	1	0	0.495	32
0	0	0	0	0	0	1	1	0.26	03	0	0	1	1	0	0	1	1	0.5	33
0	0	0	0	0	1	0	0	0.265	04	0	0	1	1	0	1	0	0	0.505	34
0	0	0	0	0	1	0	1	0.27	05	0	0	1	1	0	1	0	1	0.51	35
0	0	0	0	0	1	1	0	0.275	06	0	0	1	1	0	1	1	0	0.515	36
0	0	0	0	0	1	1	1	0.28	07	0	0	1	1	0	1	1	1	0.52	37
0	0	0	0	1	0	0	0	0.285	08	0	0	1	1	1	0	0	0	0.525	38
0	0	0	0	1	0	0	1	0.29	09	0	0	1	1	1	0	0	1	0.53	39
0	0	0	0	1	0	1	0	0.295	0A	0	0	1	1	1	0	1	0	0.535	3A
0	0	0	0	1	0	1	1	0.3	0B	0	0	1	1	1	0	1	1	0.54	3B
0	0	0	0	1	1	0	0	0.305	0C	0	0	1	1	1	1	0	0	0.545	3C
0	0	0	0	1	1	0	1	0.31	0D	0	0	1	1	1	1	0	1	0.55	3D
0	0	0	0	1	1	1	0	0.315	0E	0	0	1	1	1	1	1	0	0.555	3E
0	0	0	0	1	1	1	1	0.32	0F	0	0	1	1	1	1	1	1	0.56	3F
0	0	0	1	0	0	0	0	0.325	10	0	1	0	0	0	0	0	0	0.565	40
0	0	0	1	0	0	0	1	0.33	11	0	1	0	0	0	0	0	1	0.57	41
0	0	0	1	0	0	1	0	0.335	12	0	1	0	0	0	0	1	0	0.575	42
0	0	0	1	0	0	1	1	0.34	13	0	1	0	0	0	0	1	1	0.58	43
0	0	0	1	0	1	0	0	0.345	14	0	1	0	0	0	1	0	0	0.585	44
0	0	0	1	0	1	0	1	0.35	15	0	1	0	0	0	1	0	1	0.59	45
0	0	0	1	0	1	1	0	0.355	16	0	1	0	0	0	1	1	0	0.595	46
0	0	0	1	0	1	1	1	0.36	17	0	1	0	0	0	1	1	1	0.6	47
0	0	0	1	1	0	0	0	0.365	18	0	1	0	0	1	0	0	0	0.605	48
0	0	0	1	1	0	0	1	0.37	19	0	1	0	0	1	0	0	1	0.61	49
0	0	0	1	1	0	1	0	0.375	1A	0	1	0	0	1	0	1	0	0.615	4A
0	0	0	1	1	0	1	1	0.38	1B	0	1	0	0	1	0	1	1	0.62	4B
0	0	0	1	1	1	0	0	0.385	1C	0	1	0	0	1	1	0	0	0.625	4C
0	0	0	1	1	1	0	1	0.39	1D	0	1	0	0	1	1	0	1	0.63	4D
0	0	0	1	1	1	1	0	0.395	1E	0	1	0	0	1	1	1	0	0.635	4E
0	0	0	1	1	1	1	1	0.4	1F	0	1	0	0	1	1	1	1	0.64	4F
0	0	1	0	0	0	0	0	0.405	20	0	1	0	1	0	0	0	0	0.645	50
0	0	1	0	0	0	0	1	0.41	21	0	1	0	1	0	0	0	1	0.65	51
0	0	1	0	0	0	1	0	0.415	22	0	1	0	1	0	0	1	0	0.655	52
0	0	1	0	0	0	1	1	0.42	23	0	1	0	1	0	0	1	1	0.66	53
0	0	1	0	0	1	0	0	0.425	24	0	1	0	1	0	1	0	0	0.665	54
0	0	1	0	0	1	0	1	0.43	25	0	1	0	1	0	1	0	1	0.67	55
0	0	1	0	0	1	1	0	0.435	26	0	1	0	1	0	1	1	0	0.675	56
0	0	1	0	0	1	1	1	0.44	27	0	1	0	1	0	1	1	1	0.68	57
0	0	1	0	1	0	0	0	0.445	28	0	1	0	1	1	0	0	0	0.685	58
0	0	1	0	1	0	0	1	0.45	29	0	1	0	1	1	0	0	1	0.69	59
0	0	1	0	1	0	1	0	0.455	2A	0	1	0	1	1	0	1	0	0.695	5A
0	0	1	0	1	0	1	1	0.46	2B	0	1	0	1	1	0	1	1	0.7	5B
0	0	1	0	1	1	0	0	0.465	2C	0	1	0	1	1	1	0	0	0.705	5C
0	0	1	0	1	1	0	1	0.47	2D	0	1	0	1	1	1	0	1	0.71	5D
0	0	1	0	1	1	1	0	0.475	2E	0	1	0	1	1	1	1	0	0.715	5E
0	0	1	0	1	1	1	1	0.48	2F	0	1	0	1	1	1	1	1	0.72	5F

IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	0	0	0	0	0	0.725	60	1	0	0	1	0	0	0	0	0.965	90
0	1	1	0	0	0	0	1	0.73	61	1	0	0	1	0	0	0	1	0.97	91
0	1	1	0	0	0	1	0	0.735	62	1	0	0	1	0	0	1	0	0.975	92
0	1	1	0	0	0	1	1	0.74	63	1	0	0	1	0	0	1	1	0.98	93
0	1	1	0	0	1	0	0	0.745	64	1	0	0	1	0	1	0	0	0.985	94
0	1	1	0	0	1	0	1	0.75	65	1	0	0	1	0	1	0	1	0.99	95
0	1	1	0	0	1	1	0	0.755	66	1	0	0	1	0	1	1	0	0.995	96
0	1	1	0	0	1	1	1	0.76	67	1	0	0	1	0	1	1	1	1	97
0	1	1	0	1	0	0	0	0.765	68	1	0	0	1	1	0	0	0	1.005	98
0	1	1	0	1	0	0	1	0.77	69	1	0	0	1	1	0	0	1	1.01	99
0	1	1	0	1	0	1	0	0.775	6A	1	0	0	1	1	0	1	0	1.015	9A
0	1	1	0	1	0	1	1	0.78	6B	1	0	0	1	1	0	1	1	1.02	9B
0	1	1	0	1	1	0	0	0.785	6C	1	0	0	1	1	1	0	0	1.025	9C
0	1	1	0	1	1	0	1	0.79	6D	1	0	0	1	1	1	0	1	1.03	9D
0	1	1	0	1	1	1	0	0.795	6E	1	0	0	1	1	1	1	0	1.035	9E
0	1	1	0	1	1	1	1	0.8	6F	1	0	0	1	1	1	1	1	1.04	9F
0	1	1	1	0	0	0	0	0.805	70	1	0	1	0	0	0	0	0	1.045	A0
0	1	1	1	0	0	0	1	0.81	71	1	0	1	0	0	0	0	1	1.05	A1
0	1	1	1	0	0	1	0	0.815	72	1	0	1	0	0	0	1	0	1.055	A2
0	1	1	1	0	0	1	1	0.82	73	1	0	1	0	0	0	1	1	1.06	A3
0	1	1	1	0	1	0	0	0.825	74	1	0	1	0	0	1	0	0	1.065	A4
0	1	1	1	0	1	0	1	0.83	75	1	0	1	0	0	1	0	1	1.07	A5
0	1	1	1	0	1	1	0	0.835	76	1	0	1	0	0	1	1	0	1.075	A6
0	1	1	1	0	1	1	1	0.84	77	1	0	1	0	0	1	1	1	1.08	A7
0	1	1	1	1	0	0	0	0.845	78	1	0	1	0	1	0	0	0	1.085	A8
0	1	1	1	1	0	0	1	0.85	79	1	0	1	0	1	0	0	1	1.09	A9
0	1	1	1	1	0	1	0	0.855	7A	1	0	1	0	1	0	1	0	1.095	AA
0	1	1	1	1	0	1	1	0.86	7B	1	0	1	0	1	0	1	1	1.1	AB
0	1	1	1	1	1	0	0	0.865	7C	1	0	1	0	1	1	0	0	1.105	AC
0	1	1	1	1	1	0	1	0.87	7D	1	0	1	0	1	1	0	1	1.11	AD
0	1	1	1	1	1	1	0	0.875	7E	1	0	1	0	1	1	1	0	1.115	AE
0	1	1	1	1	1	1	1	0.88	7F	1	0	1	0	1	1	1	1	1.12	AF
1	0	0	0	0	0	0	0	0.885	80	1	0	1	1	0	0	0	0	1.125	B0
1	0	0	0	0	0	0	1	0.89	81	1	0	1	1	0	0	0	1	1.13	B1
1	0	0	0	0	0	1	0	0.895	82	1	0	1	1	0	0	1	0	1.135	B2
1	0	0	0	0	0	1	1	0.9	83	1	0	1	1	0	0	1	1	1.14	B3
1	0	0	0	0	1	0	0	0.905	84	1	0	1	1	0	1	0	0	1.145	B4
1	0	0	0	0	1	0	1	0.91	85	1	0	1	1	0	1	0	1	1.15	B5
1	0	0	0	0	1	1	0	0.915	86	1	0	1	1	0	1	1	0	1.155	B6
1	0	0	0	0	1	1	1	0.92	87	1	0	1	1	0	1	1	1	1.16	B7
1	0	0	0	1	0	0	0	0.925	88	1	0	1	1	1	0	0	0	1.165	B8
1	0	0	0	1	0	0	1	0.93	89	1	0	1	1	1	0	0	1	1.17	B9
1	0	0	0	1	0	1	0	0.935	8A	1	0	1	1	1	0	1	0	1.175	BA
1	0	0	0	1	0	1	1	0.94	8B	1	0	1	1	1	0	1	1	1.18	BB
1	0	0	0	1	1	0	0	0.945	8C	1	0	1	1	1	1	0	0	1.185	BC
1	0	0	0	1	1	0	1	0.95	8D	1	0	1	1	1	1	0	1	1.19	BD
1	0	0	0	1	1	1	0	0.955	8E	1	0	1	1	1	1	1	0	1.195	BE
1	0	0	0	1	1	1	1	0.96	8F	1	0	1	1	1	1	1	1	1.2	BF

IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	0	0	0	0	0	1.205	C0	1	1	1	0	0	0	0	0	1.365	E0
1	1	0	0	0	0	0	1	1.21	C1	1	1	1	0	0	0	0	1	1.37	E1
1	1	0	0	0	0	1	0	1.215	C2	1	1	1	0	0	0	1	0	1.375	E2
1	1	0	0	0	0	1	1	1.22	C3	1	1	1	0	0	0	1	1	1.38	E3
1	1	0	0	0	1	0	0	1.225	C4	1	1	1	0	0	1	0	0	1.385	E4
1	1	0	0	0	1	0	1	1.23	C5	1	1	1	0	0	1	0	1	1.39	E5
1	1	0	0	0	1	1	0	1.235	C6	1	1	1	0	0	1	1	0	1.395	E6
1	1	0	0	0	1	1	1	1.24	C7	1	1	1	0	0	1	1	1	1.4	E7
1	1	0	0	1	0	0	0	1.245	C8	1	1	1	0	1	0	0	0	1.405	E8
1	1	0	0	1	0	0	1	1.25	C9	1	1	1	0	1	0	0	1	1.41	E9
1	1	0	0	1	0	1	0	1.255	CA	1	1	1	0	1	0	1	0	1.415	EA
1	1	0	0	1	0	1	1	1.26	CB	1	1	1	0	1	0	1	1	1.42	EB
1	1	0	0	1	1	0	0	1.265	CC	1	1	1	0	1	1	0	0	1.425	EC
1	1	0	0	1	1	0	1	1.27	CD	1	1	1	0	1	1	0	1	1.43	ED
1	1	0	0	1	1	1	0	1.275	CE	1	1	1	0	1	1	1	0	1.435	EE
1	1	0	0	1	1	1	1	1.28	CF	1	1	1	0	1	1	1	1	1.44	EF
1	1	0	1	0	0	0	0	1.285	D0	1	1	1	1	0	0	0	0	1.445	F0
1	1	0	1	0	0	0	1	1.29	D1	1	1	1	1	0	0	0	1	1.45	F1
1	1	0	1	0	0	1	0	1.295	D2	1	1	1	1	0	0	1	0	1.455	F2
1	1	0	1	0	0	1	1	1.3	D3	1	1	1	1	0	0	1	1	1.46	F3
1	1	0	1	0	1	0	0	1.305	D4	1	1	1	1	0	1	0	0	1.465	F4
1	1	0	1	0	1	0	1	1.31	D5	1	1	1	1	0	1	0	1	1.47	F5
1	1	0	1	0	1	1	0	1.315	D6	1	1	1	1	0	1	1	0	1.475	F6
1	1	0	1	0	1	1	1	1.32	D7	1	1	1	1	0	1	1	1	1.48	F7
1	1	0	1	1	0	0	0	1.325	D8	1	1	1	1	1	0	0	0	1.485	F8
1	1	0	1	1	0	0	1	1.33	D9	1	1	1	1	1	0	0	1	1.49	F9
1	1	0	1	1	0	1	0	1.335	DA	1	1	1	1	1	0	1	0	1.495	FA
1	1	0	1	1	0	1	1	1.34	DB	1	1	1	1	1	0	1	1	1.5	FB
1	1	0	1	1	1	0	0	1.345	DC	1	1	1	1	1	1	0	0	1.505	FC
1	1	0	1	1	1	0	1	1.35	DD	1	1	1	1	1	1	0	1	1.51	FD
1	1	0	1	1	1	1	0	1.355	DE	1	1	1	1	1	1	1	0	1.515	FE
1	1	0	1	1	1	1	1	1.36	DF	1	1	1	1	1	1	1	1	1.52	FF

STARTUP TIMING

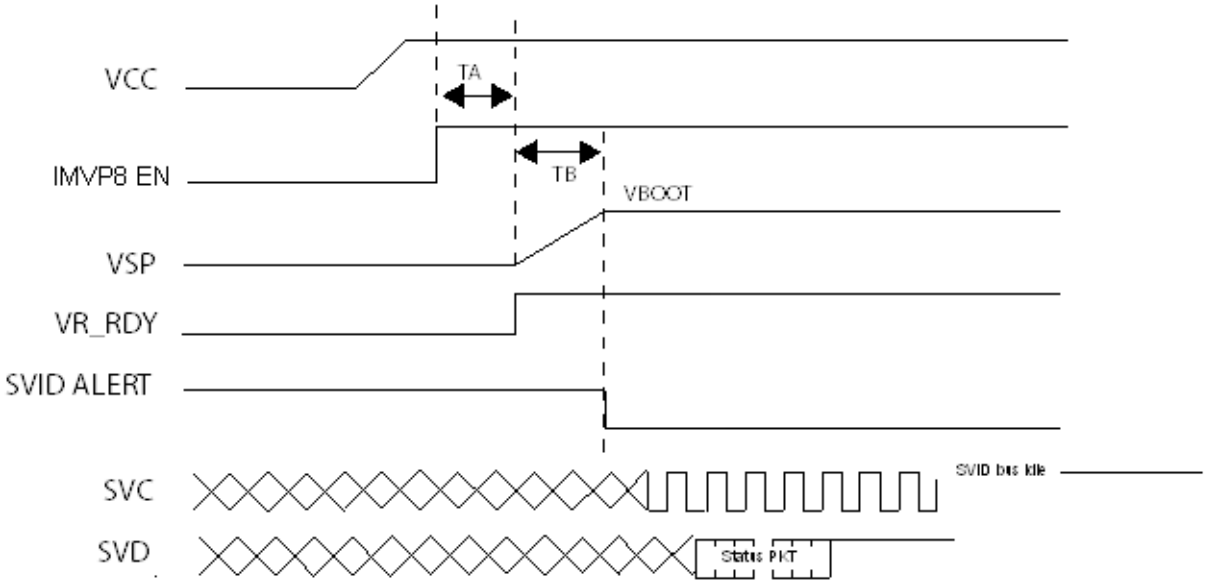


Figure 7.

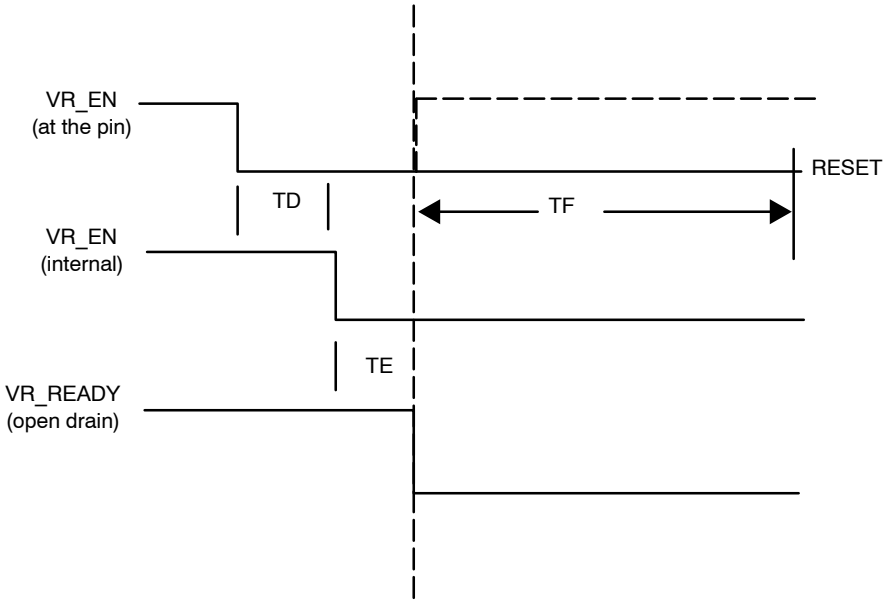
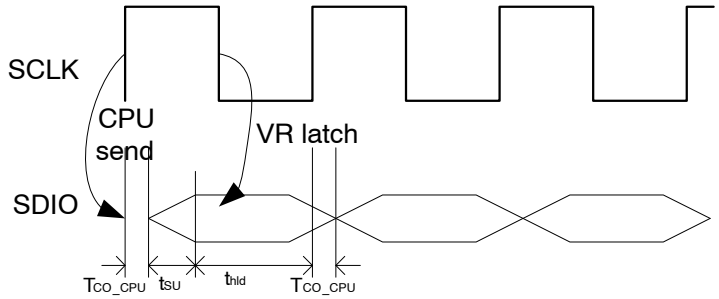


Figure 8.

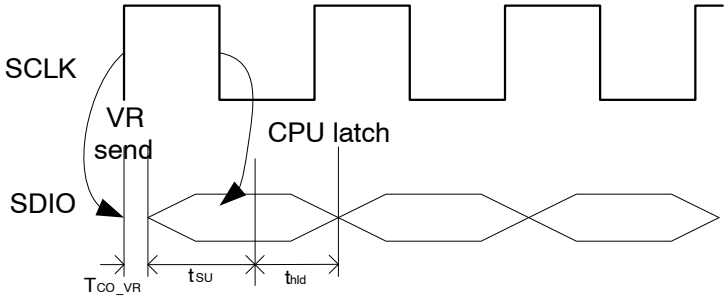
	MIN	TYP	MAX
TA			2.5 ms
TB			VID / Slow
TD	0 us		1 μs
TE			500 ns

SVID Timing Diagram



T_{co_CPU} = clock to data delay in CPU
$t_{su} = 0.5*T - T_{co_CPU}$
$t_{hld} = 0.5*T + T_{co_CPU}$

Figure 9. CPU Driving, Single Data Rate



T_{co_VR} = clock to data delay in VR
$t_{su} = T - 2*T_{fly} - T_{co_VR}$
$t_{hld} = 2*T_{fly} + T_{co_VR}$
T_{fly} propagation time on Serial VID bus

Figure 10. VR Driving, Single Data Rate

General Information

The NCP81218P is a three−rail IMVP8 controller with an Intel SVID control interface intended to provide VCORE (Address 00h), VGT (Address 01h), and VSA (Address 02h) or VGTUS (Address 03h). NCP81218P is optimized to meet Intel's IMVP8 specifications and implements PS0, PS1, PS2, PS3 and PS4 power−states.

Serial VID interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the NCP81218P (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the CPU. The SDIO is bi−directional, used for transferring data from the CPU to the NCP81218P and from the NCP81218P to the CPU. The ALERT# is an open drain output from the NCP81218P to signal to the CPU indicating that the Status Register should be read.

SCLK should have a 55 Ω pull−up resistor to the CPU I/O voltage Vccio (typically 1.0 V), placed close to the NCP81218P. SDIO should have 2 pull−up resistors of 110 Ω to Vccio, one placed close to the NCP81218P, the other close to the CPU. Alert# should have a 75 Ω pull−up resistor and a 43 Ω series resistor placed close to the CPU.

The SVID bus can operate at a maximum frequency of 43 MHz.

VID code changes are supported by the SVID interface with the following three options:

Option	SVID Command Code	Feature Description	Register Address (Indicating the slew rate of VID code change)
SetVID_Fast	01h	30 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	16, 8, 4 or 2 times slower than the SetVID_Fast rate. Binary format in mV/us. Fast/2 is the default.	25h
SetVID_Decay	03h	No control, VID code down	N/A

Supported Registers

The table of supported registers for Domains 00h, 01h, and 02/03h is shown below. The SVID register set for Domain 0Dh (PSYS) is smaller, and contains only registers 00h, 01h, 02h, 03h, 05h, 10h, 11h, 1Bh, 1Ch and 2Eh.

Index	Name	Description	Access	Default	
				00h/01h/02h/03h	0Dh
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number. 28h = NCP81218P	R	28h	28h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	05h	
03h	Product date code ID		R		
05h	Protocol ID	Identifies the SVID Protocol the controller supports. 05h = IMVP8	R	05h	05h
06h	Capability	Informs the Master of the controller's Capabilities Bit0 = Iout ADC (15h) = 1 Bit1 = Vout ADC (16h) = 0 Bit2 = Pout ADC (18h) = 0 Bit3 = I input ADC (19h) = 0 Bit4 = V input ADC (1Ah) = 1 Bit5 = P input ADC (1Bh) = 0 Bit6 = Temperature ADC (17h) = 1 Bit7 = 1 if (15h) is Iout = 1	R	D1h	N/A
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h	N/A
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R		N/A
17h	VR_Temp	8 bit binary word. Binary format in deg C, For example: 100C=64h.	R		N/A
1Ah	Input Voltage	8 bit binary word from ADC of input voltage measured at VRMP pin. LSB = 110 mV. Binary Code = 255 x VRMP/28.	R	N/A	N/A
1Bh	Input Power	Required for Input Power Domain Address 0Dh	R	N/A	
1Ch	Status2_last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h	00h
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h	N/A

Index	Name	Description	Access	Default	
				00h/01h/02h/03h	0Dh
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the SVID Interface	R/W	64h	N/A
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us.	R	1Eh	N/A
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/μs. FAST/2 is the default.	R	0Fh	N/A
26h	Vboot	Vboot is resistor programmed at startup. The controller will ramp to Vboot and hold at Vboot until it receives a new SetVID command to move to a different voltage.	R	00h	N/A
2Ah	SR_Slow selector	01h = Fast_SR/2 02h = Fast_SR/4 04h = Fast_SR/8 08h = Fast_SR/16	R/W	01h	N/A
2Bh	PS4 exit latency	Reflects the latency exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the start of output voltage ramp.	R	8Ch	N/A
2Ch	PS3 exit latency	Reflects the latency exiting PS3 state. Exit latency is defined as the time duration, in μs, from ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h	N/A
2Dh	EN to Ready for SVID command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh	N/A
2Eh	Pin Max	Input Power Sensor Scaling	RW	N/A	FFh
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format.	RW	FBh	N/A
31h	VID setting	Data register containing currently programmed VID voltage. VID data format.	RW	00h	N/A
32h	Pwr State	Register containing the current programmed power state.	RW	00h	N/A

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h = no margin
		01h = +1 VID step
		02h = +2 VID steps
		FFh = −1 VID step
		FEh = −2 VID steps.
			RW	00h	N/A

34h	MultiVR Config			01h	N/A
42h	IVID1−VID		RW	00h	N/A
43h	IVID1−I	Maximum instantaneous current for single phase operation. 2−phase rail: ICCMAX/2 1−phase rails: ICCMAX	RW		N/A
44h	IVID2−VID		RW	00h	N/A
45h	IVID2−I	Maximum instantaneous current for IVID 2 state 2−phase rail: 0.3 x ICCMAX 1−phase rails: 5/8 x ICCMAX	RW		N/A
46h	IVID3−VID		RW	00h	N/A
47h	IVID3−I	Maximum instantaneous current for DCM/CCM decision threshold	RW	03h	N/A

The table below specifies the ADDR_VBOOT pin pulldown resistor (1% tolerance required) needed to program all possible supply rail configurations. Four boot voltages are available for all rails except for the SA rail.

RAIL CONFIGURATION TABLE

ADDR_VBOOT Resistance	SYSTEM RAIL									Configuration
	CORE			GT			SA			
	PHASE COUNT	TSENSE_1PH a/b	Boot Voltage	PHASE COUNT	TSENSE_2PH	Boot Voltage	PHASE COUNT	a/b	Boot Voltage	
10k	1	a	0 V	2 or 1		0 V	1	b	1.05 V	1+2+1 IA+GT+SA
16.2k	1	a	1.2 V	2 or 1		1.2 V	1	b		
22.1k	1	a	1.05 V	2 or 1		1.05 V	1	b		
28.7k	1	a	1.0 V	2 or 1		1.0 V	1	b		
ADDR_VBOOT Resistance	CORE			GT			SA			Configuration
	PHASE COUNT	TSENSE_2PH	Boot Voltage	PHASE COUNT	TSENSE_1PH a/b	Boot Voltage	PHASE COUNT	a/b	Boot Voltage	
35.7k	2 or 1		0 V	1	a	0 V	1	b	1.05 V	2+1+1 IA+GT+SA
43.2k	2 or 1		1.2 V	1	a	1.2 V	1	b		
51.1k	2 or 1		1.05 V	1	a	1.05 V	1	b		
61.9k	2 or 1		1.0 V	1	a	1.0 V	1	b		
ADDR_VBOOT Resistance	CORE			GT			SA			Configuration
	PHASE COUNT	TSENSE_1PH a/b	Boot Voltage	PHASE COUNT	TSENSE_2PH	Boot Voltage	PHASE COUNT	a/b	Boot Voltage	
71.5k	1	b	0 V	2 or 1		0 V	1	a	1.05 V	1+2+1 SA+GT+IA
82.5k	1	b	1.2 V	2 or 1		1.2 V	1	a		
95.3k	1	b	1.05 V	2 or 1		1.05 V	1	a		
110k	1	b	1.0 V	2 or 1		1.0 V	1	a		
ADDR_VBOOT Resistance	CORE			GT			GTUS			Configuration
	PHASE COUNT	TSENSE PSYS a/b	Boot Voltage	PHASE COUNT	TSENSE_2PH	Boot Voltage	PHASE COUNT	TSENSE_1PH a/b	Boot Voltage	
127k	1	b	0 V	2 or 1		0 V	1	a	0 V	1+2+1 IA+GT+GTUS
143k	1	b	1.2 V	2 or 1		1.2 V	1	a	1.2 V	
165k	1	b	1.05 V	2 or 1		1.05 V	1	a	1.05 V	
187k	1	b	1.0 V	2 or 1		1.0 V	1	a	1.0 V	

IMVP8 requires thermal sensing for the CORE, GT, and VccGTUS rails. The last four configurations in the above table provide three temperature sense inputs to accomplish this by reconfiguring the PSYS pin as the temperature monitor for the Core rail (reported at address 00h). In these four configurations, the PSYS function must be provided by a separate device.

Start Up

Following the rise of V_{CC} above the UVLO threshold, externally programmed configuration data is collected, and the PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRVON is asserted (high) to activate the gate drivers. A digital counter steps the DAC up from

zero to the target voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level.

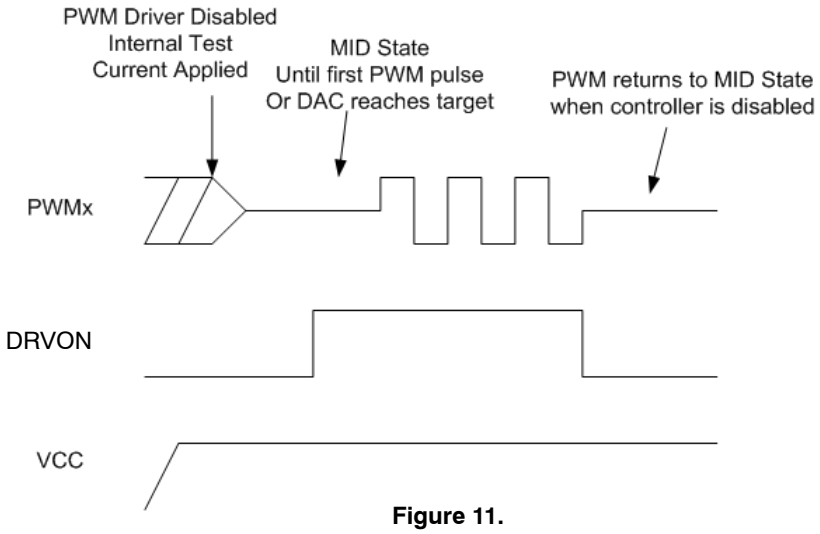


Figure 11.

Phase Count, Rail Disabling & PSYS Disabling Detection Sequence

During start−up, the number of operational phases of the 2−phase rail, and whether or not each single−phase rail becomes active and responds to an address call on the SVID bus, is determined by the internal circuitry monitoring the CSP inputs. Normally, the 2−phase rail operates with both phases. If CSP2_2ph is externally pulled to V_{CC} with a resistor during startup, the two−phase rail operates as a single−phase rail, and does not use PWM2_2ph and CSP2_2ph. Likewise, if CSP of either or both single−phase rails is pulled to V_{CC} during startup, it is disabled and will not respond to any address calls on the SVID bus.

Also, whether or not the PSYS function is active and responds to an address call on the SVID bus is determined by the internal circuitry monitoring the PSYS input. Tying the PSYS input to V_{CC} will cause the NCP81218P to not respond to any calls to address 0Dh on the SVID bus.

Switching Frequency

Switching frequencies between 200 kHz and 1.2 MHz are programmed at startup with pulldown resistors on pins 14 and 15. The 1a and 2−phase regulators (usually the Core and GT rails) are programmed to the same switching frequency by the pin 14 resistor, and the SA or Core rail (usually the 1b regulator) is programmed by the pin 15 resistor.

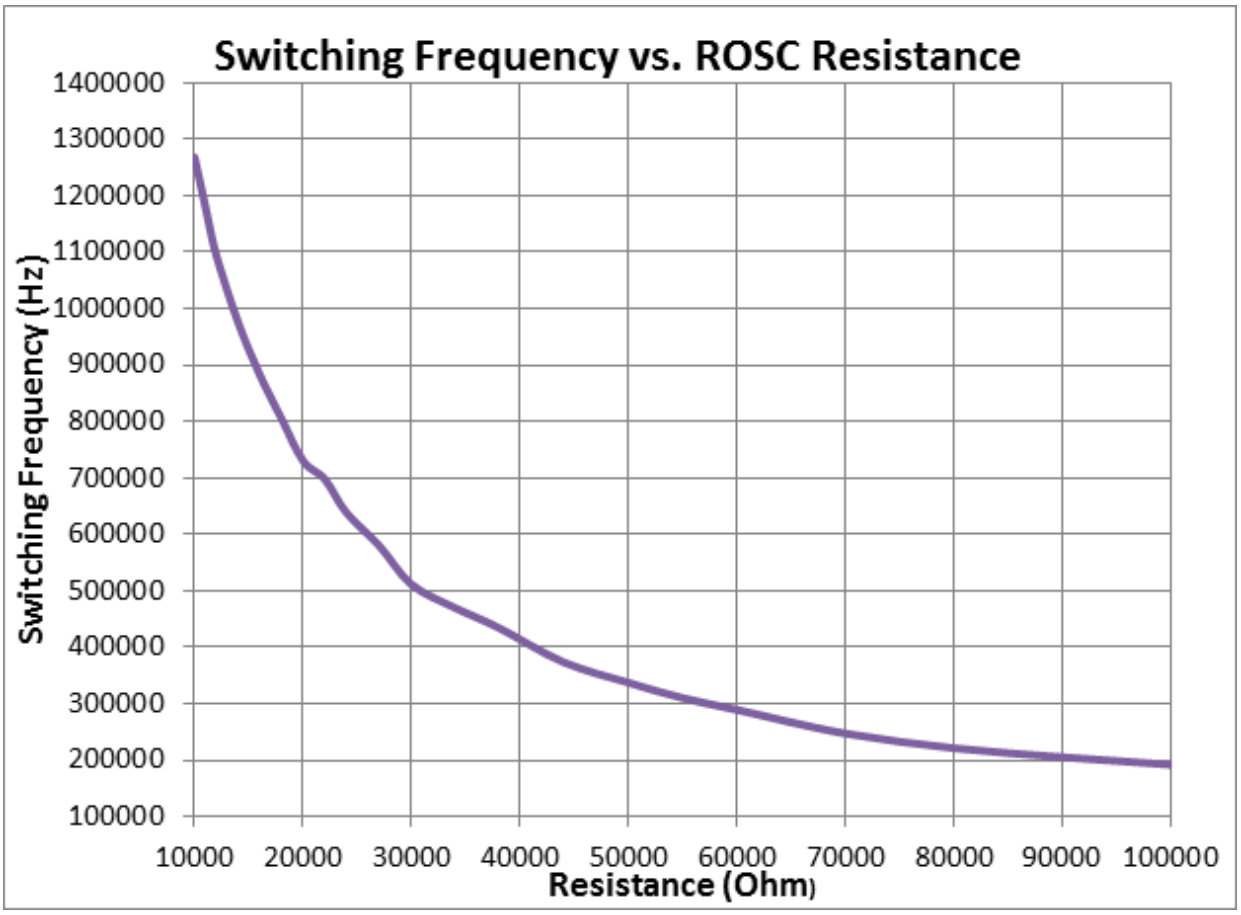


Figure 12.

The CORE/GT oscillator serves as the master clock for the 2−phase rail ramp generator when configured for 2−phase operation, and as a frequency stabilization clock for a single phase rail and for the 2−phase rail when it is configured for single phase operation. The SA/US oscillator serves as a frequency stabilization clock for the SA rail.

The formulas to calculate the switching frequency and programming resistances are:

$$R_{OSC} = 2 * 10^{+11} * Frequency^{-1.192}\ [\Omega] \quad \text{(eq. 1)}$$

$$Frequency = 3 * 10^{+9} * Frequency^{-0.838}\ [Hz] \quad \text{(eq. 2)}$$

Input Voltage Feed−Forward (VRAMP pin)

Ramp generator circuits are provided for both the dual−edge modulator (only when 2−phases are operating) and three RPM modulators. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

For 2−phase operation, the dual−edge PWM ramp amplitude is changed according to the following,

$$V_{RAMP_pp} = 0.1 * V_{VRMP} \quad \text{(eq. 3)}$$

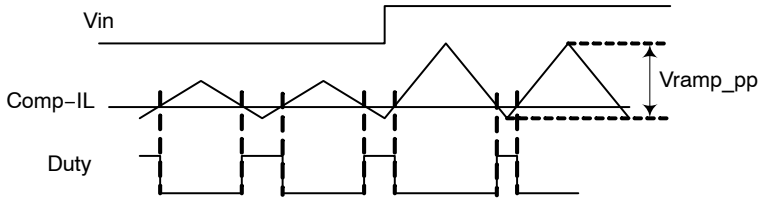


Figure 13.

Programming Two−Phase Rail ICC_MAX

The SVID interface provides the platform ICC_MAX value at register 21h for all all three rails. A resistor to ground on the ICCMAX_2ph pin programs the register for the 2−phase rail at the time the part is enabled. Current $I_{MXBIAS2}$ is sourced from this pin to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10k.

$$ICC_MAX_{21h} = \frac{R * I_{MXBIAS2} * 128\ A}{2\ V} \quad \text{(eq. 4)}$$

Programming TSENSE

Two temperature sense inputs are provided – one for the 2−phase rail, and the other for single−phase rail 1a. A precision current is sourced out the output of the TSENSE pins to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

When the NCP81218P is configured with a GTUS rail, the PSYS input is repurposed to a third TSENSE input reported at address 00h.

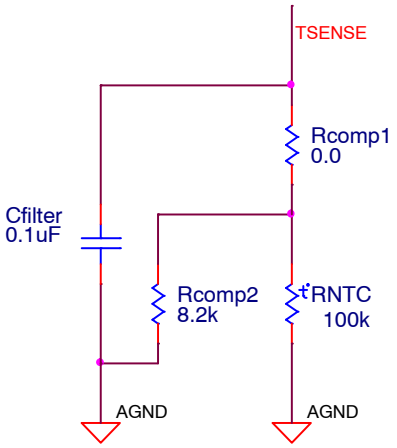


Figure 14.

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

Automatic CCM/DCM operation

In PS2 and PS3, all rails will operate in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) depending on load current in order to prevent loss of efficiency from negative inductor current.

SVID Power State	2ph Rail Max Operating Mode	Possible Efficiency Optimized Modes
PS0	Two−phase dual edge	−
PS1	Single−phase CCM RPM	−
PS2	Single−phase CCM RPM	Single−phase DCM RPM
PS3	Single−phase CCM RPM	Single−phase DCM RPM
PS4	Standby	

If a SetPS command is received, the controller will place itself in the lowest appropriate state. For example, if in PS3 the controller has automatically dropped into DCM RPM and receives a SetPS = 2 command, the PS register will be updated, but the controller will remain in DCM RPM mode. If while in PS2 or PS3 the current increases, the controller will move into CCM mode.

The controller changes to PS0 when any SetVID command is issued.

Two−Phase Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{DAC}) + (V_{DROOP} - V_{CSREF}) \quad \text{(eq. 5)}$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

Two−phase rail voltage compensation

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

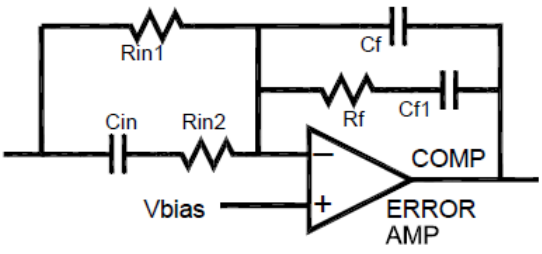


Figure 15.

Two−Phase Rail Differential Current Feedback Amplifiers

Each phase of the two−phase rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset due to leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance. The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

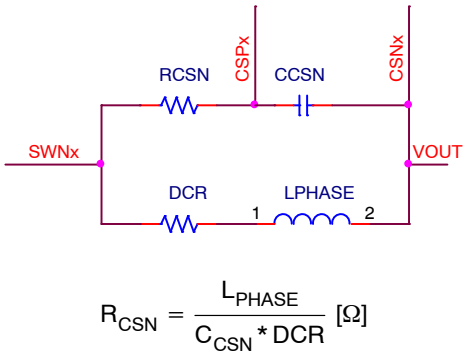


Figure 16.

Two−Phase Rail Total Current Sense Amplifier

The NCP81218P uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switchnodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages. The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. The Phase 1 inductor is chosen for the thermistor location so that the temperature of the inductor providing current in the PS1 power mode.

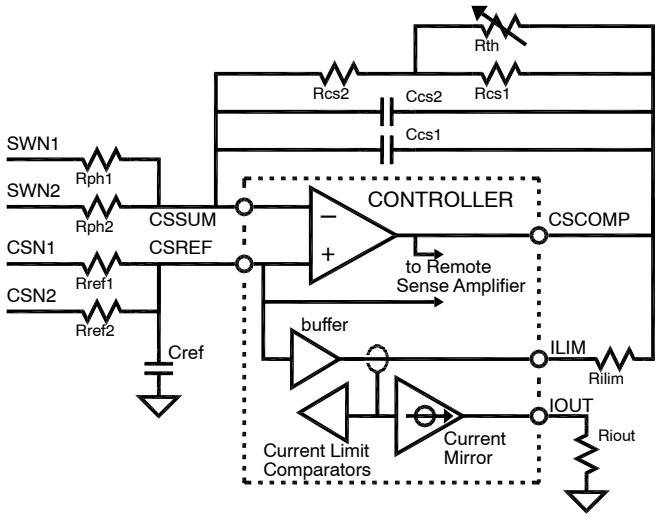


Figure 17.

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP-CSREF} = \frac{R_{CS2} + \frac{R_{CS1}*Rth}{R_{CS1}+Rth}}{Rph} * \left(Iout_{Total} * DCR\right) \quad \text{(eq. 6)}$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline.

The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_Z = \frac{DCR@25C}{2*\pi*L_{Phase}} [Hz] \quad \text{(eq. 7)}$$

$$F_P = \frac{1}{2*\pi*\left(Rcs2 + \frac{Rcs1*Rth@25C}{Rcs1+Rth@25C}\right)(Ccs1 + Ccs2)} [Hz] \quad \text{(eq. 8)}$$

The value of the C_{REF} capacitor (in nF) on the CSREF pin should be:

$$C_{REF} = \frac{0.02 * R_{PH}}{R_{REF}} [nF] \quad \text{(eq. 9)}$$

Two−Phase Rail Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81218P, a loadline is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current.

The loadline is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

Two−Phase Rail Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The NCP81218P generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to I_{CL0} and I_{CLM0} (I_{CL1} and I_{CLM1} in PS1, PS2 and PS3). The NCP81218P latches off if ILIM pin current exceeds I_{CL0} (I_{CL1} for PS1, PS2, and PS3) for t_{OCPDLY}, and latches off immediately if ILIM pin current exceeds I_{CLM0} (I_{CLM1} for PS1, PS2 and PS3). Set the value of the current limit resistor R_{LIMIT} according to the desired current limit $Iout_{LIMIT}$.

$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{LIMIT} * DCR\right) \quad \text{(eq. 10)}$$

Two−Phase Rail Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if desired.

$$R_{IOUT} = \frac{2.0\ V * R_{LIMIT}}{10 * \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{ICC_MAX} * DCR\right)} [\Omega] \quad \text{(eq. 11)}$$

Two−Phase Rail Programming DAC Feed−Forward Filter

The NCP81218P outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to current flowing into the charging output capacitors. In the following equations, Cout is the total output capacitance of the system.

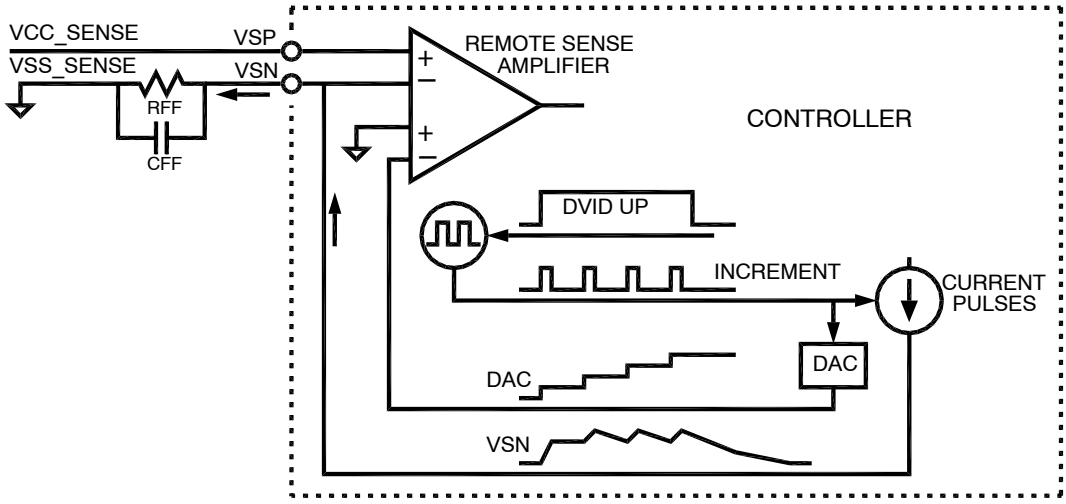


Figure 18.

$$R_{FF} = \frac{Loadline * Cout}{9.35 * 10^{-10}} [\Omega] \quad \text{(eq. 12)}$$

$$C_{FF} = \frac{200}{R_{FF}} [nF] \quad \text{(eq. 13)}$$

Two−Phase Rail PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (I_L*DCR*Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output.

During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Single−Phase Rails

The architecture of the two single−phase rails makes use of a digitally enhanced, high performance, current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions.

Features of the single−phase rails

- Supports SVID Addresses 00, 01, 02, 03
- Adjustable Vboot
- Programmable Slew Rate
- Dynamic VID Feed−Forward
- High performance RPM control system
- Programmable Droop Gain (Zero Droop Capable)
- Low Offset IOUT monitor
- Thermal Monitor
- Digitally Controlled Operating Frequency
- UltraSonic Operation

Single−phase Rail Frequency Programming

One of the two single−phase rails has frequency programmed by the ROSC_COREGT pin, and the other has frequency programmed by the ROSC_SAUS pin. ROSC_COREGT always controls the frequency of the IA and GT rails unless there are two GT rails. In that case, ROSC_COREGT controls the frequency of both GT rails, and ROSC_SAUS controls the frequency of the IA rail.

Single−phase Rail Remote Sense Error Amplifier

A high performance, high input impedance, differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks described in the Droop Compensation and DAC Feedforward Compensation sections. The remote sense error amplifier outputs a current proportional to the difference between the VSP, VSN and DAC voltages:

$$I_{COMP} = gm_{EA} \times \left[V_{DAC} - \left(V_{VSP} - V_{VSN}\right)\right] \quad \text{(eq. 14)}$$

Single−phase rail voltage compensation

The Remote Sense Amplifier output current is applied to a standard Type II compensation network formed by external tuning components CLF, RZ and CHF.

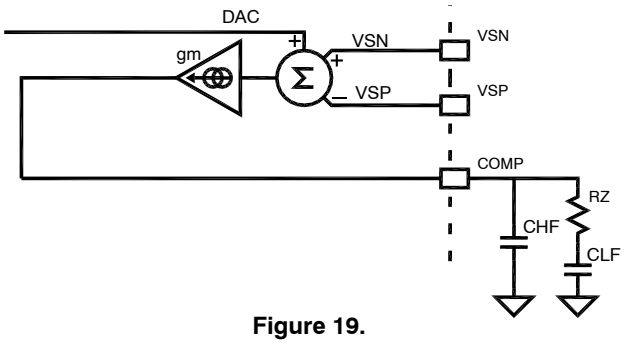


Figure 19.

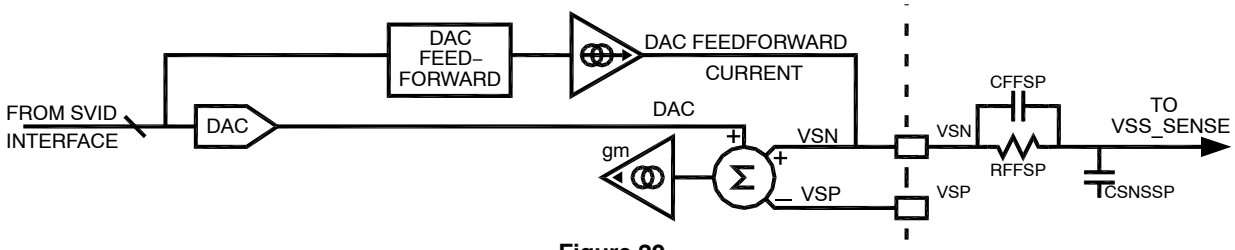


Figure 20.

$$R_{FFSP} = \frac{Loadline * Cout}{1.35 * 10^{-9}} \ [\Omega] \quad \text{(eq. 15)}$$

$$C_{FFSP} = \frac{200}{R_{FFSP}} \ [nF] \quad \text{(eq. 16)}$$

Single−phase Rail – Differential Current Feedback Amplifier

Each single−phase controller has a low offset, differential amplifier to sense output inductor current. An external lowpass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. To do this, the lowpass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

Single−phase Rail – Programming the DAC Feed−Forward Filter

The DAC feed−forward implementation for the single−phase rail is the same as for the 2−phase rail. The NCP81218P outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the Droop function response to inductor current flowing into the charging output capacitors. RFFSP sets the gain of the DAC feed−forward and CFFSP provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance of the system.

$$F_Z = \frac{DCR@25C}{2 * \pi * L} \ [Hz] \quad \text{(eq. 17)}$$

$$F_P = \frac{1}{2 * \pi * \frac{R_{PHSP} * \left(Rth + R_{CSSP}\right)}{R_{PHSP} + Rth + R_{CSSP}} * C_{CSSP}} \ [Hz] \quad \text{(eq. 18)}$$

Forming the lowpass filter with an NTC thermistor (Rth) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of RPHSP and RCSSP are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.. The CSP and CSN pins are high impedance

inputs, but it is recommended that the lowpass filter resistance not exceed 10 kΩ in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 mΩ for sufficient current accuracy. Recommended values for the external filter components are:

$$C_{CSSP} = \frac{L_{PHASE}}{\frac{R_{PHSP}*(Rth + R_{CSSP})}{R_{PHSP} + Rth + R_{CSSP}} * DCR} \text{ [F]} \quad \text{(eq. 19)}$$

- R_{PHSP} = 7.68 kΩ
- R_{CSSP} = 14.3 kΩ
- Rth = 100 kΩ, Beta = 4300

Using two parallel capacitors in the lowpass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} * Iout * DCR \quad \text{(eq. 20)}$$

To improve the noise immunity of the current feedback amplifier, it is recommended to use an RC low pass filter (R_F and C_F in Figure 21) on the CSN pin of the amplifier placed as close as possible to the controller. The bandwidth of this filter should be ~5 MHz with $R_F < 20\ \Omega$. To mitigate against noise due to excessive ringing that may be present on the inductor side of R_{PHSP}, it is recommended to use a capacitor in parallel with the inductor. The value of the capacitor should be chosen such that:

$$\sqrt{L \times C} < < \frac{1}{2 \times \pi \times \text{Ringing Frequency}} \quad \text{(eq. 21)}$$

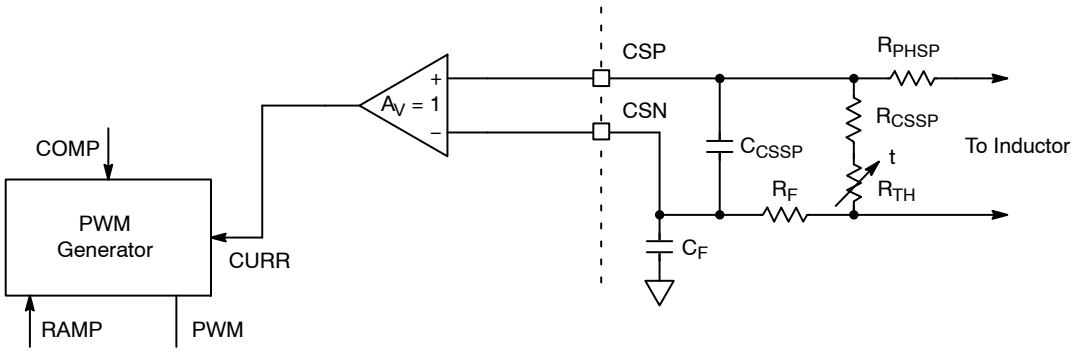


Figure 21.

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

Single−phase Rail – Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage (V_{DROOP}) proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81218P, a loadline is produced by adding V_{DROOP} to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced in proportion to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point by forcing current from the VSP pin that is proportional to the difference between the CSP and CSN voltages.

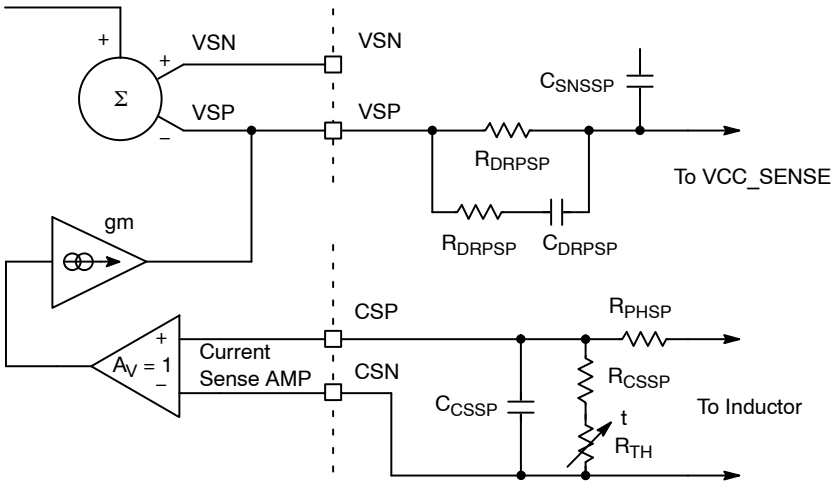


Figure 22.

$$V_{DROOP} = R_{DRPSP} \times gm_{VSP} \times \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} \times I_{OUT} \times DCR \quad \text{(eq. 22)}$$

$$R_{DRPSP} = \frac{Loadline}{gm_{VSP} \times DCR} \times \frac{R_{PHSP} + Rth + R_{CSSP}}{Rth + R_{CSSP}} \ [\Omega] \quad \text{(eq. 23)}$$

Single−phase Rail – Programming IOUT

The IOUT pin sources a current proportional to the voltage between the CSP and CSN pins. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A high−value pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if desired.

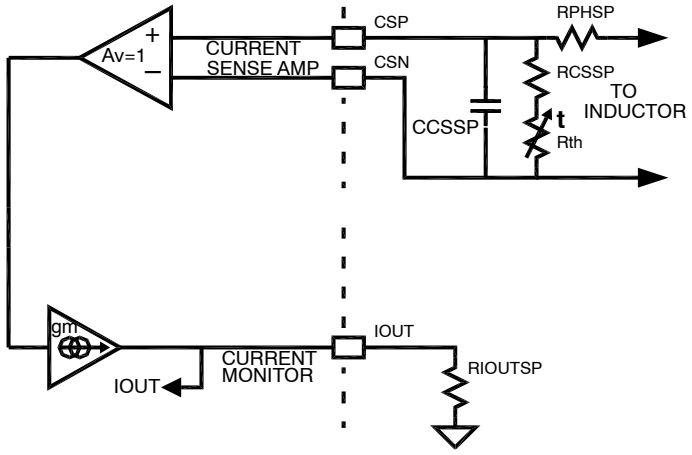


Figure 23.

$$R_{IOUTSP} = \frac{2\ V}{gm_{IOUT} \times \frac{Rth + R_{CSSP}}{R_{PHSP} + Rth + R_{CSSP}} \times ICCMax \times DCR} \quad \text{(eq. 24)}$$

Programming the Single−Phase Rail ICC_MAX

The internal SVID registers store the platform ICC_MAX values at location 21h for all three rails. Resistors to ground on the ICCMAX_1a and ICCMAX_1b pins program these registers for the single phase rails at the time the part is enabled. $I_{MXBIAS1A}$ and $I_{MXBIAS1B}$ currents are sourced from these pins to generate a voltage on the program resistors. The value in these registers is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10k.

$$ICC_MAX_{21h} = \frac{R * I_{MXBIAS1} * 64\ A}{2\ V} \quad \text{(eq. 25)}$$

Single−phase Rail Pulsewidth Modulator

A PWM pulse starts when the Error Amp output (COMP voltage) exceeds a trigger threshold including a scaled inductor current (I_L*DCR*Phase Current Gain Factor). The PWM pulse ends when scaled inductor current added to a compensating reset ramp exceeds the COMP voltage. Both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the COMP voltage increases with respect to the trigger threshold and reset ramp, to provide a highly linear and proportional response to the step load.

Disabling a Single−Phase Rail

If the NCP81218P is to provide fewer than three rails, either or both of the single−phase regulators can be disabled by pulling up their respective CSP pin to VCC. The two−phase regulator cannot be disabled.

PROTECTION FEATURES

Two−Phase Regulator Over Current Protection (OCP)

A programmable total phase current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents (I_{CL0}, I_{CLM0}, I_{CL1}, and I_{CLM1}). When the 2−phase rail is operating in PS0, if the ILIM pin current exceeds I_{CL0}, an internal latch−off timer starts. If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds I_{CLM0}, the controller shuts down immediately. When operating in PS1, PS2, or PS3, the ILIM pin current limits are I_{CL1} and I_{CLM1}. To recover from an OCP fault, the EN pin or V_{CC} voltage must be cycled low.

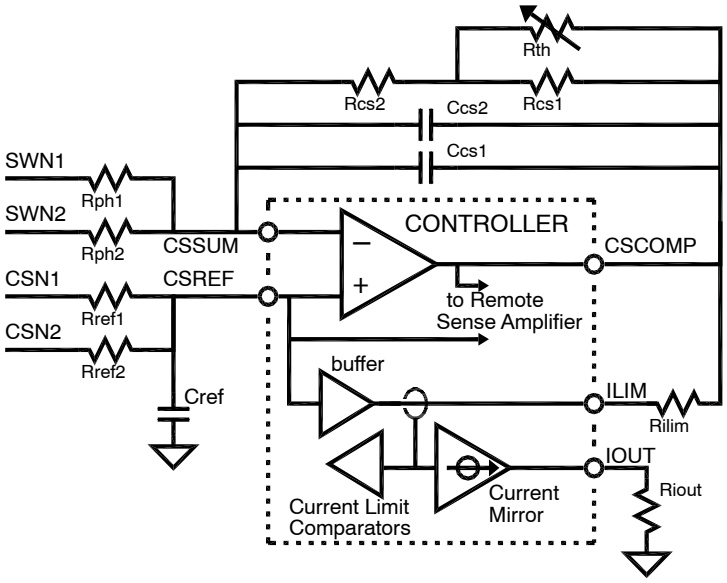


Figure 24.

Use Equation 10 to calculate the ILIM resistor value.

Single−phase Rail Over Current Protection (OCP)

The current limit threshold is programmed with a resistor (R_{ILIMSP}) from the ILIM pin to ground. The current limit latches the single−phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold Voltage (V_{CL}). Set the value of the current limit resistor based on the equation shown below.

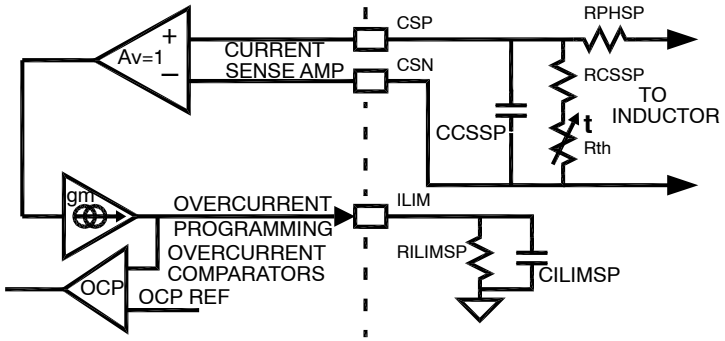


Figure 25.

$$R_{ILIMSP} = \frac{V_{CL}}{gm_{ILIM} \times \frac{R_{th}+R_{CSSP}}{R_{PHSP}+R_{th}+R_{CSSP}} \times Iout_{LIMIT} \times DCR} \ [\Omega] \quad \text{(eq. 26)}$$

$$C_{ILIMSP} = \frac{5 * 10^{+7}}{R_{ILIMSP}} \ [pF] \quad \text{(eq. 27)}$$

A capacitor (C_{ILIMSP}) in parallel with the ILIM pin resistor creates a time delay to give some tolerance for output currents that momentarily exceed the current limit. The C_{ILIMSP} value given in the equation below will give up to a 50 μs delay with a 150% overload depending on the load current prior to overload.

To recover from an OCP fault, the EN pin or V_{CC} voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

NCP81218P monitors the 5 V V_{CC} supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The 2−phase rail output voltage is monitored for undervoltage at the output of the differential amplifier. If the

2−phase rail output falls more than V_{UVM2} below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.The single−phase rail outputs are monitored for undervoltage at the CSN inputs. If the CSN voltage falls more than V_{UVM1} below the DAC voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The 2−phase output voltage is monitored for OVP at the output of the differential amplifier and also at the CSREF pin. The single−phase regulator outputs are monitored for overvoltage at the VSP & VSN inputs, and also at the CSN inputs. During normal operation, if an output voltage exceeds the DAC voltage by V_{OVP}, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP Threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the NCP81218P will stay in this mode until the V_{CC} voltage or EN is toggled.

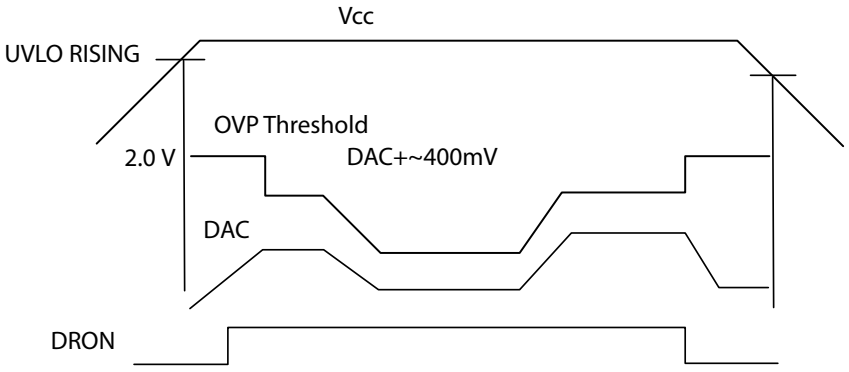


Figure 26. OVP Threshold Behavior

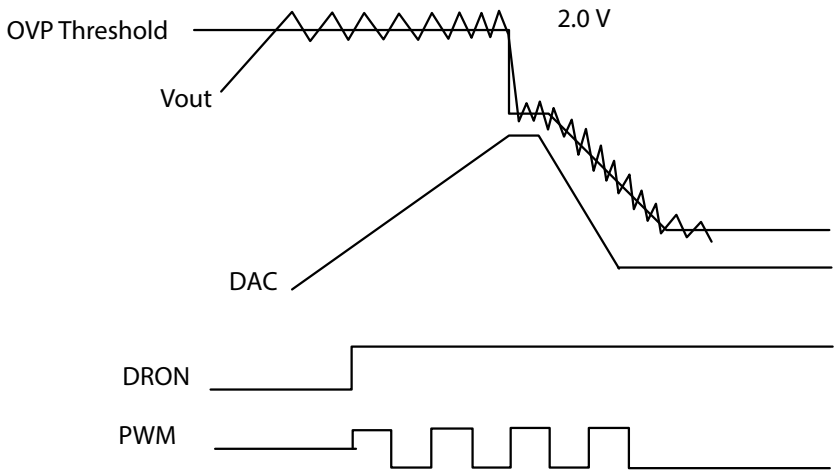


Figure 27. OVP Behavior at Startup

During start up, the OVP threshold is set to the Absolute Over Voltage Threshold. This allows the controller to start up without false triggering OVP.

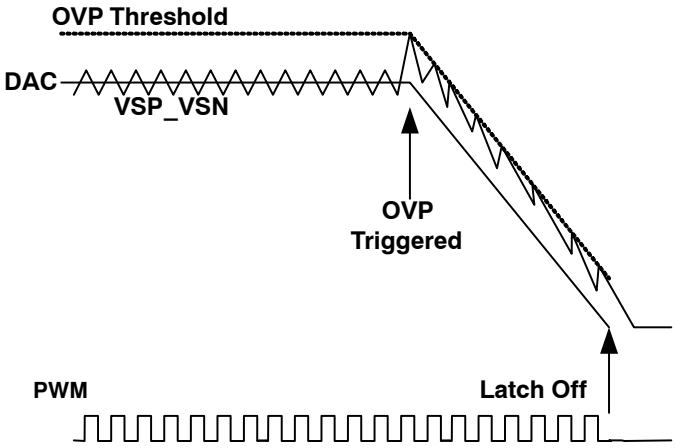
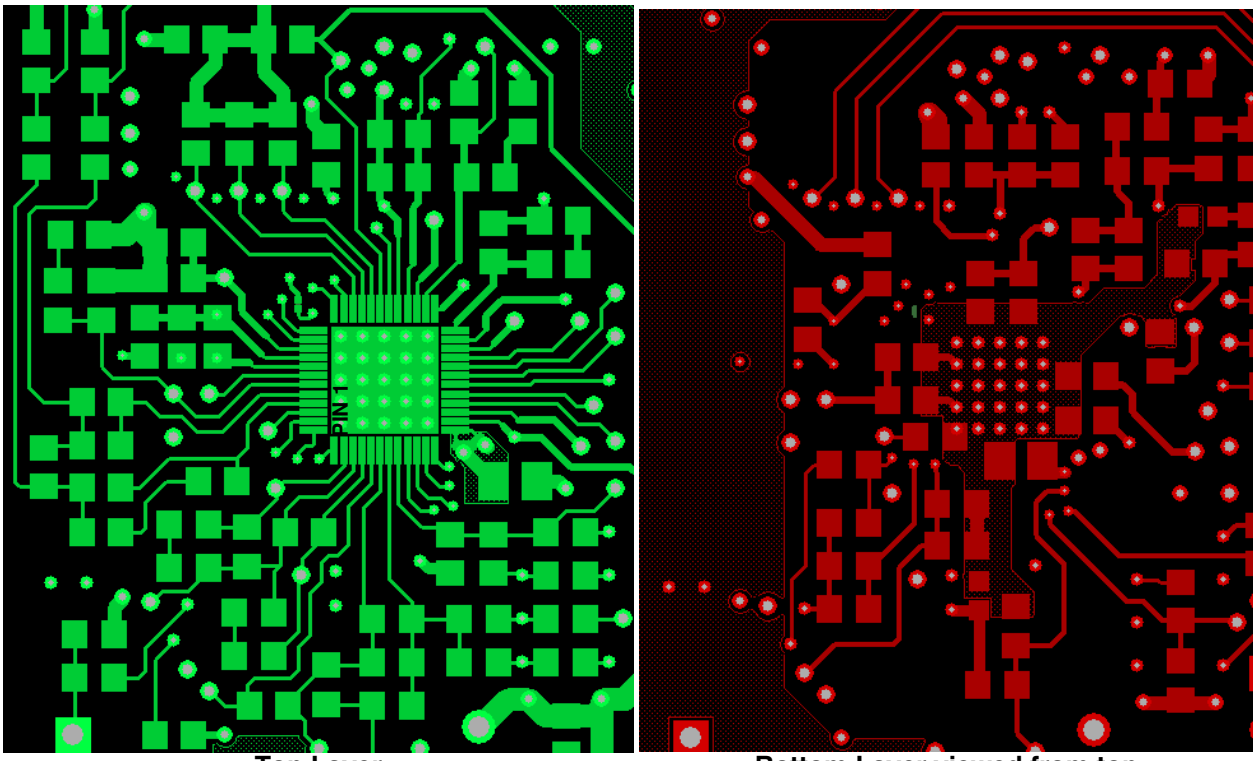


Figure 28. OVP During Normal Operation Mode

TYPICAL PCB LAYOUT

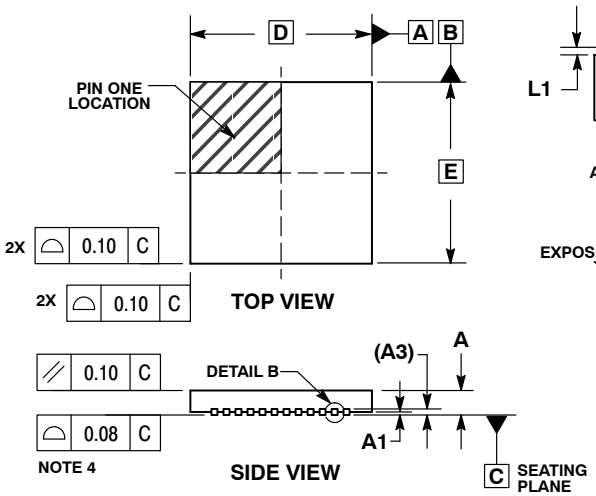


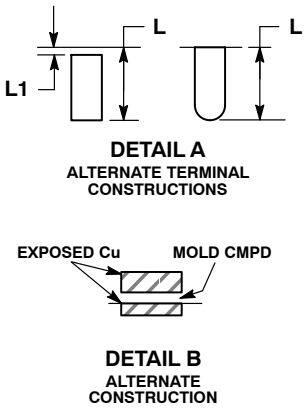
Top Layer Bottom Layer viewed from top

Figure 29.

PACKAGE DIMENSIONS

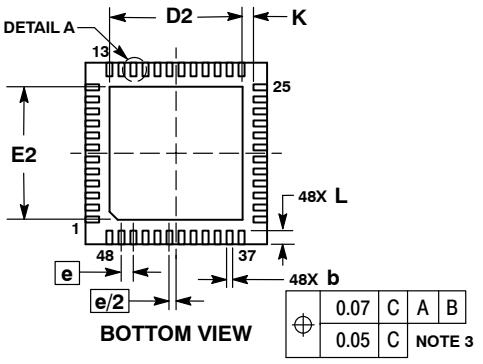
QFN48 6x6, 0.4P
CASE 485BA
ISSUE A



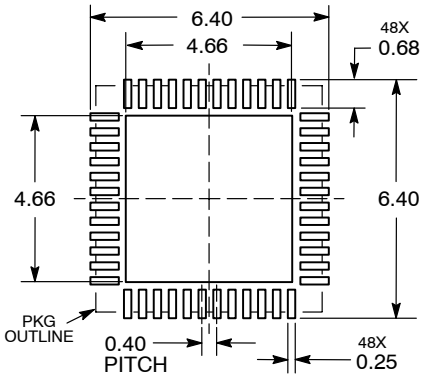


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.40	4.60
E	6.00 BSC	
E2	4.40	4.60
e	0.40 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	0.00	0.15



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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