Onsemi

QFN16 CASE 485G

Precise Low Voltage Synchronous Buck Controller with Power Saving Mode

NCP81147

The NCP81147 is a simple single phase solution with differential phase current sensing, power saving operation, and gate drivers to provide accurately regulated power.

The adaptive non overlap gate drive and power saving operation circuit provide a low switching loss and high efficiency solution for server, notebook, and desktop systems. A high performance operational error amplifier is provided to simplify compensation of the system. The NCP81147 features also include soft-start sequence, accurate overvoltage and over current protection, UVLO for VCC and VCCP, and thermal shutdown.

Features

- High Performance Operational Error Amplifier
- Internal Soft-Start/Stop
- ±0.5% Internal Voltage Accuracy, 0.8 V voltage reference
- OCP accuracy, Four Re-entry Times Before Latch
- "Lossless" Differential Inductor Current Sensing
- Internal High Precision Current Sensing Amplifier
- Oscillator Frequency Range of 100 kHz 1000 kHz
- 20 ns Adaptive FET Non-overlap Time of Internal Gate Driver
- 5.0 V to 12 V Operation
- Support 1.5 V to 19 V Vin
- V_{out} from 0.8 V to 3.3 V (5 V with 12 V_{CC})
- Chip Enable through OSC pin
- Latched Over Voltage Protection (OVP)
- Internally Fixed OCP Threshold
- Guaranteed Startup Into Pre-Charged Loads
- Thermally Compensated Current Monitoring
- Thermal Shutdown Protection
- Integrated MOSFET Drivers
- Integrated BOOST Diode with internal $R_{bst} = 2.2 \Omega$
- · Automatic Power Saving Mode to Maximize Efficiency During Light Load Operation
- Sync Function
- Remote Ground Sensing
- This is a Pb-Free Device*

Applications

Desktop and Server Systems

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN CONNECTIONS ROSC/EN GND CSP 200 16 15 14 |13| VCCP 1 12 CSN/VO 11 LG 2 FBG 10 3 VSEN LX 4 9 BOOT FB 6 7 8 5 PGOOD SYNC 5 COMP (Top View)

MARKING DIAGRAMS



81147 = Specific Device Code

- = Assembly Location = Wafer Lot
- = Year

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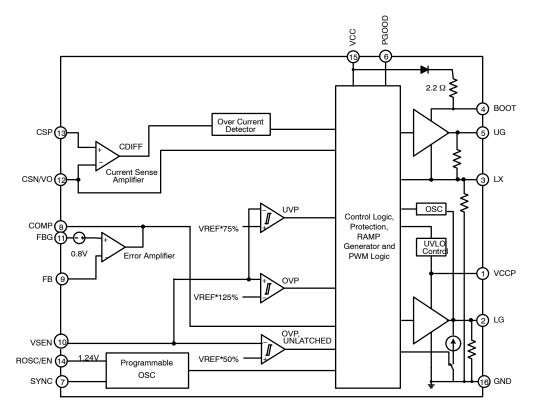
- Υ W = Work Week
- = Pb-Free Package

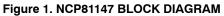
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NCP81147MNTXG	QFN16 (Pb-Free)	3,000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.





PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	VCCP	Power supply for bottom gate MOSFET drivers
2	LG	Bottom gate MOSFET driver pin
3	LX	Switch node
4	BOOT	Supply rail for the floating top gate driver
5	UG	Top gate MOSFET driver pin
6	PGOOD	Power Good. It is an open-drain output, set free after SS (with 3x clock delay) as long as the output voltage monitored through VSEN is within specifications.
7	SYNC	Synchronization Pin. The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used.
8	COMP	Output of the error amplifier
9	FB	Inverting input to the error amplifier
10	VSEN	Output Voltage Sense
11	FBG	Remote Ground Sense
12	CSN/VO	Inductor differential sense inverting input
13	CSP	Inductor differential sense non-inverting input
14	ROSC/EN	Programs the switching frequency; EN: Pull-low to disable the device
15	VCC	Supply rail for the controller internal circuitry
16	GND	Ground reference
	THERMAL PAD	Connects with the silicon substrate for good thermal contact with the PCB. Connect to GND plane.

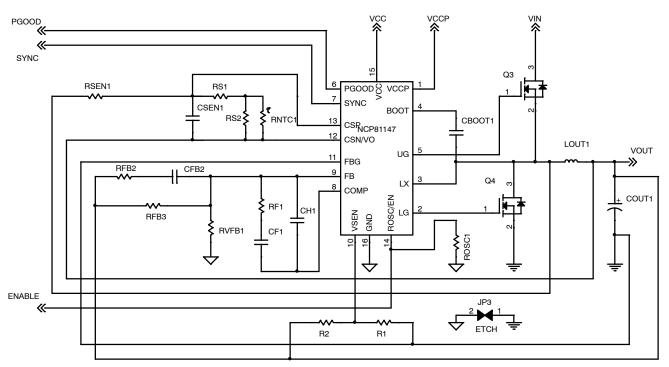


Figure 2. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	V _{MAX}	V _{MIN}	Unit
VCC, VCCP	Controller Power Supply Voltages to GND	15	-0.3	V
BOOT	Boost Supply Voltage Input	35V wrt/GND 40 V <100 ns wrt/GND 15 wrt/LX	-0.3	V
UG	High–Side Driver Output (Top Gate)	35 40 V ≤ 50 ns wrt/GND 15 wrt/LX	–0.3 wrt/LX –5 V < 200 ns	V
LX	Switching Node (Bootstrap Supply Return)	35 40 < 100 ns	_5 _10 V < 200 ns	V
LG	Low–Side Driver Output (Bottom Gate)	15	_0.3 _5 V < 200 ns	V
	All Other Pins	6	−0.3, −1 V < 1 μs	V
PGOOD	PGOOD	7	−0.3, −1 V < 1 μs	V
SYNC	SYNC	7	−0.3, −1 V < 1 μs	V
CSP, CSN/VO with V _{CC} = 12 V	Current Sense Amplifier	10	–0.3, –1 V < 1 μs	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Symbol	Rating	Тур	Unit
R_{\thetaJA}	Thermal Resistance, Junction-to-Ambient	60	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	18	°C/W
TJ	Operating Junction Temperature Range	-40 to +125	°C
T _A	Operating Ambient Temperature Range	-40 to +85	°C
T _{STG}	Maximum Storage Temperature Range	-55 to +150	°C
MSL	Moisture Sensitivity Level QFN Package	1	-

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $-40^{\circ}C < T_A < 85^{\circ}C$; 4.5 V < VCC < 13.2 V; $C_{VCC} = 0.1 \ \mu F$

Parameter	Test Conditions	Min	Тур	Max	Unit
SUPPLY OPERATING CONDITIONS			אני	шил	
VCC Voltage Range		4.5	_	13.2	V
VCCP Voltage Range		4.5	_	13.2	V
dV/dt on VCC (Note 1)		-10	_	10	V/µs
dV/dt on VCCP (Note 1)		-10	_	10	V/µs
VCC AND BOOT INPUT SUPPLY CURREN	T				
VCC Operating Current	V_{CC} = 5 V, EN = High V_{CC} = 12 V, EN = High	-	-	5.0	mA
VCC Supply Current	V_{CC} = 5 V, EN = Low V_{CC} = 12 V, EN = Low	-	-	400	uA
VCCP INPUT SUPPLY CURRENT					
VCCP Operating Current UG and LG Open	V _{CCP} = 5 V, EN = High V _{CCP} = 12 V, EN = High	-	3.5	5.0	mA
VCCP Supply Current	V_{CCP} = 5 V, EN = Low V_{CCP} = 12 V, EN = Low	-	-	200	μΑ
VCC SUPPLY VOLTAGE			-		
VCC UVLO Start Threshold	V _{CC} Rising	-	-	4.50	V
VCC UVLO Hysteresis	V _{CC} Rising or Falling	-	300	-	mV
VCCP SUPPLY VOLTAGE					
VCCP UVLO Start Threshold		-	-	4.2	V
VCCP UVLO Hysteresis		-	200	-	mV
ERROR AMPLIFIER COMP					
Open Loop DC Gain (Note 1)		-	120	-	dB
Open Loop Unity Gain Bandwidth (Note 1)		15	18	-	MHz
Slew Rate (Note 1)	COMP pin to GND with 100 pF load	-	8.0	-	V/μs
VREF					
Internal Reference Voltage		-	0.800	-	V
Output Voltage Accuracy	V _{out} to FBG excluding external resistor divider tolerance	-1.5	-	1.5	%
CURRENT SENSE AMPLIFIERS					
Common Mode Input Voltage Range (Note 1, GNG, output within 10mV)	$V_{CC} \le 7.5 V$	-0.3	_	3.5	V
Common Mode Input Voltage Range (Note 1, GNG, output within 10 mV)	V _{CC} > 7.5 V	-0.3	-	5.5	V

ELECTRICAL CHARACTERISTICS (continued) Unless otherwise stated: $-40^{\circ}C < T_A < 85^{\circ}C$; 4.5 V < VCC < 13.2 V; $C_{VCC} = 0.1 \ \mu F$

OSC Gain (Note 1) - 10 Disable threshold R _{OSC} /EN pin, V _{dis_th} - - 0 Minimum Pulse Width F _{sw} = 200 kHz, OSC open - 90 Minimum Turn Off Time (LG on) F _{sw} = 200 kHz, OSC open 250 350 4 Magnitude of the PWM Ramp V _{IN} = 5 V or 12 V - 1.50 4 Mainimum Duty Cycle OSC/EN = OPEN 80 - 2 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - 5 SOFT-START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 5 Soft FF Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 120 0 OVER CURRENT PROTECTION - 120 2 5 5 - 0 Synchronization Input VIL, square wave - - - 0 2 5 - 10 OVP Threshold VSEN rising above 1.25 * Vref 110 125 1	Parameter	Test Conditions	Min	Тур	Max	Unit
OSC Gain (Note 1) Image: Constraint of the second sec	R (with no ROSC Resistor Def	aults to 200 kHz)				
Disable threshold ROSC/EN pin, Vdis th I I I Disable threshold ROSC/EN pin, Vdis th - 90 I Minimum Pulse Width Faw = 200 kHz, OSC open 250 350 4 Magnitude of the PWM Ramp Vin = 5 V or 12 V - 1.50 I Maximum Duty Cycle OSC/EN = OPEN 80 - 12 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - 12 SOFT-START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 SOFT-OFF Soft OFF bleeding resistor Rdis - 120 I Socond Over Current Threshold CSP-CSN, 4xMasking 17 20 I Second Over Current Threshold CSP-CSN, Immediate action - 30 I I Synchronization Input VIL, square wave - - - I I OVP Threshold VSEN faling above 1.25 * Vreft 110 125 1 I I <t< td=""><td>equency Accuracy</td><td>R_{OSC} open</td><td>-15</td><td>-</td><td>15</td><td>%</td></t<>	equency Accuracy	R _{OSC} open	-15	-	15	%
MODULATORS (PWM Comparators) $ 90$ Minimum Pulse Width $F_{sw} = 200 kHz, OSC open$ $ 90$ Minimum Turn Off Time (LG on) $F_{sw} = 200 kHz, OSC open$ 250 350 4 Magnitude of the PWM Ramp $V_{IN} = 5 V \text{ or } 12 V$ $ 1.50$ Maximum Duly Cycle $OSC/EN = OPEN$ 80 $ 1.50$ Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 300 $ 1.50$ SOFT-START Soft Start Time @ 200 kHz $1024 clock cycles, OSC/EN open$ $ 5.12$ Soft OFF bleeding resistor R_{dis} $ 120$ $0VER CURRENT PROTECTION$ First Over Current Threshold CSP-CSN, 4xMasking 17 20 3 Synchronization Input V/L, square wave 2.5 $ 5$ Synchronization Input V/L, square wave 2.5 $ -$ <td< td=""><td>Note 1)</td><td></td><td>-</td><td>10</td><td>-</td><td>kHz / μA</td></td<>	Note 1)		-	10	-	kHz / μA
Minimum Pulse Width F _{BW} = 200 kHz, OSC open - 90 Minimum Turn Off Time (LG on) F _{SW} = 200 kHz, OSC open 250 350 4 Magnitude of the PWM Ramp V _{IN} = 5 V or 12 V - 1.50 1 Maximum Duty Cycle OSC/EN = OPEN 80 - 1 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - 1 SOFT -START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 S SOFT -OFF Soft OFF bleeding resistor R _{clis} - 120 OVER CURRENT PROTECTION First Over Current Threshold CSP-CSN, 4xMasking 17 20 2 Synchronization Input VIL, square wave - - - Synchronization Input VIL, square wave 2.5 - OVP Threshold VSEN falling above 1.25 * V _{ref} 110 125 1 OVP Threshold VSEN falling below 0.75 * V _{ref} 70 75 3 OVP Threshold VSE	shold	R _{OSC} /EN pin, V _{dis_th}	-	-	0.75	V
Minimum Turn Off Time (LG on) FBW = 200 kHz, OSC open 250 350 4 Magnitude of the PWM Ramp VIN = 5 V or 12 V - 1.50 1 Maximum Duty Cycle OSC/EN = OPEN 80 - 1 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - 1 SOFT-START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 5 SOFT-OFF Soft OFF bleeding resistor Rdis - 120 5 Second Over Current Threshold CSP-CSN, 4xMasking 17 20 5 Synchronization Input VIL, square wave - - - 0 Synchronization Input VIL, square wave 2.5 - 10 125 10 OVET Threshold VSEN rising above 1.25 * Vref 110 125 1 10 OVPT Threshold VSEN failing below 0.75 * Vref 70 75 3 1 OVPT Threshold VSEN failing below 0.75 * Vref 70 75 </td <td>RS (PWM Comparators)</td> <td></td> <td></td> <td></td> <td></td> <td>-</td>	RS (PWM Comparators)					-
Magnitude of the PWM Ramp VIN = 5 V or 12 V - 1.50 Maximum Duty Cycle OSC/EN = OPEN 80 - 1 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - 1 SOFT-START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 0 Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 120 0 OVER CURRENT PROTECTION Rdis - 120 0 Second Over Current Threshold CSP-CSN, 4xMasking 17 20 2 Synchronization Input VIL, square wave - - - Synchronization Input VIL, square wave 2.5 - 0 PROTECTION AND PGOOD Uruput Voltage Logic Low, Sinking 4 mA - - - 0 OVP Threshold VSEN rising above 1.25 * Vref 110 125 1 0 UVP Threshold VSEN failing below 0.75 * Vref 70 75 3 0 Dewer Go	lse Width	F _{sw} = 200 kHz, OSC open	-	90	-	ns
Maximum Duty Cycle OSC/EN = OPEN 80 - 1 Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - I SOFT-START - SOFT-START - 5 - SOFT-OFF Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 SOFT-OFF Soft OFF bleeding resistor Rdis - 120 S OVER CURRENT PROTECTION - - 30 - Synchronization Input CSP-CSN, 4xMasking 17 20 - Synchronization Input VIL, square wave - - - Synchronization Input VIL, square wave - - - - Output Voltage Logic Low, Sinking 4 mA - - - 0 0 Output Voltage Logic Low, Sinking 4 mA - - - 0 0 OVP Threshold VSEN failing below 0.75 * Vref 100 125 1 Unlatched Overvoltage Threshold	rn Off Time (LG on)	F _{sw} = 200 kHz, OSC open	250	350	450	ns
Minimum Skip mode frequency In light load, maximum time for LG to turn on after HG turns off 30 - SOFT-START	f the PWM Ramp	V _{IN} = 5 V or 12 V	-	1.50	-	V
after HG turns off Image: Margin after HG turns off SOFT-START Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 SOFT-OFF Soft OFF bleeding resistor Rdis - 120 Soft Start Time @ 200 kHz 300 Soft Start Time @ 200 kHz	uty Cycle	OSC/EN = OPEN	80	-	95	%
Soft Start Time @ 200 kHz 1024 clock cycles, OSC/EN open - 5.12 SOFT-OFF Soft OFF bleeding resistor Rdis - 120 OVER CURRENT PROTECTION First Over Current Threshold CSP-CSN, 4xMasking 17 20 2 Second Over Current Threshold CSP-CSN, Immediate action - 30 3 SYNC PIN Synchronization Input VIL, square wave - - - 1 Synchronization Input VIL, square wave - - - 1 0 PROTECTION AND PGOOD Output Voltage Logic Low, Sinking 4 mA - - - 0 OVP Threshold VSEN rising above 1.25 * Vref 110 125 1 UVP Threshold VSEN falling below 0.75 * Vref 70 75 1 Unlatched Overvoltage Threshold Vth_disoff with respect to 0.5 Vref 40 50 0 Power Good Low Delay (Note 1) - - - - 2 ERO CURRENT DETECTION (LX Pin) Ime to capture LX voltag	ip mode frequency		30	-	_	kHz
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Soft OFF bleeding resistor Rdis - 120 OVER CURRENT PROTECTION First Over Current Threshold CSP-CSN, 4xMasking 17 20 3 Second Over Current Threshold CSP-CSN, 1mmediate action - 30 30 SYNC PIN Synchronization Input VIL, square wave - - - 5 Synchronization Input VIL, square wave 2.5 - 5 - 5 PROTECTION AND PGOOD Utput Voltage Logic Low, Sinking 4 mA - - 6 OVP Threshold VSEN rising above 1.25 * Vref 110 125 1 UVP Threshold VSEN falling below 0.75 * Vref 70 75 4 Over Good High Delay (Note 1) - - - - Power Good Low Delay (Note 1) - - - - - ZERO CURRENT DETECTION (LX Pin) Time to capture LX voltage once LG is < 1.0 V	ne @ 200 kHz	1024 clock cycles, OSC/EN open	-	5.12	-	ms
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Second Over Current Threshold CSP-CSN, Immediate action - 30 SYNC PIN Synchronization Input VIL, square wave -	RENT PROTECTION			.		
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Synchronization InputVIH, square wave2.5-PROTECTION AND PGOODOutput VoltageLogic Low, Sinking 4 mA0OVP ThresholdVSEN rising above $1.25 \times V_{ref}$ 1101251UVP ThresholdVSEN falling below $0.75 \times V_{ref}$ 70753Unlatched Overvoltage ThresholdVth_disoff with respect to $0.5 V_{ref}$ 40506Power Good High Delay (Note 1)Power Good Low Delay (Note 1)ZERO CURRENT DETECTION (LX Pin)Blanking Time after LG is < 1.0 V Detection (Note 1)Time to capture LX voltage once LG is < 1.0 V Capture Time for LX Voltage (Note 1)Time to capture LX voltage once LG is < 1.0 V Negative LX detection voltage V_{bdls} 1503004Positive LX detection voltage V_{bdhs} 0.20.5-Time for V _{th} adjustment and settling time (Note 1)300 kHz3.0Initial Negative Current DetectionLX-GND, Includes $\pm 2 \text{ mV Offset Range}$ -1.0						
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Output VoltageLogic Low, Sinking 4 mA0OVP ThresholdVSEN rising above $1.25 * V_{ref}$ 1101251UVP ThresholdVSEN falling below $0.75 * V_{ref}$ 70753Unlatched Overvoltage ThresholdVsEN falling below $0.75 * V_{ref}$ 40506Power Good High Delay (Note 1)4Power Good Low Delay (Note 1)4ZERO CURRENT DETECTION (LX Pin)4Blanking Time before Zero Current Detection (Note 1)Blanking Time after LG is < 1.0 V (must be within dead time limits)Capture Time for LX Voltage (Note 1)Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)Negative LX detection voltage V_{bdls} 0.20.5Time for V _{th} adjustment and settling time (Note 1)300 kHz3.0-3.0-Initial Negative Current DetectionLX-GND, Includes ± 2 mV Offset Range-1.0-	tion Input	VIH, square wave	2.5	_	_	V
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UVP ThresholdVSEN falling below $0.75 * V_{ref}$ 707575Unlatched Overvoltage Threshold V_{th_disoff} with respect to $0.5 V_{ref}$ 405060Power Good High Delay (Note 1)Power Good Low Delay (Note 1)ZERO CURRENT DETECTION (LX Pin)Blanking Time before Zero Current Detection (Note 1)Blanking Time after LG is < 1.0 V (must be within dead time limits)Capture Time for LX Voltage (Note 1)Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)Negative LX detection voltage V_{bdls} 0.20.5-Time for V_{th} adjustment and settling time (Note 1)300 kHz3.0-5Initial Negative Current DetectionLX-GND, Includes ± 2 mV Offset Range-1.0	ge	Logic Low, Sinking 4 mA	-	_	0.4	V
Unlatched Overvoltage Threshold V_{th_disoff} with respect to 0.5 V_{ref} 405060Power Good High Delay (Note 1) <td>old</td> <td>VSEN rising above 1.25 * V_{ref}</td> <td>110</td> <td>125</td> <td>140</td> <td>%</td>	old	VSEN rising above 1.25 * V _{ref}	110	125	140	%
Power Good High Delay (Note 1)Power Good Low Delay (Note 1)ZERO CURRENT DETECTION (LX Pin)Blanking Time before Zero Current Detection (Note 1)Blanking Time after LG is < 1.0 V Capture Time for LX Voltage (Note 1)Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)Negative LX detection voltageVbdls1503004Positive LX detection voltageVbdhs0.20.5-Time for Vth adjustment and settling time (Note 1)300 kHz3.0-3.0Initial Negative Current DetectionLX-GND, Includes ± 2 mV Offset Range-1.0	old	VSEN falling below 0.75 * V _{ref}	70	75	80	%
Power Good High Delay (Note 1)Power Good Low Delay (Note 1)Power Good Low Delay (Note 1)ZERO CURRENT DETECTION (LX Pin)Blanking Time before Zero Current Detection (Note 1)Blanking Time after LG is < 1.0 V (must be within dead time limits)-Capture Time for LX Voltage (Note 1)Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)Negative LX detection voltageV bdls1503004Positive LX detection voltageV bdhs0.20.5-Time for V (Note 1)300 kHz3.0-3Initial Negative Current DetectionLX-GND, Includes ± 2 mV Offset Range-1.0	vervoltage Threshold	V_{th} disoff with respect to 0.5 V_{ref}	40	50	60	%
ZERO CURRENT DETECTION (LX Pin) Blanking Time before Zero Current Detection (Note 1) Blanking Time after LG is < 1.0 V	High Delay (Note 1)	-	-	-	50	μs
Blanking Time before Zero Current Detection (Note 1) Blanking Time after LG is < 1.0 V -	Low Delay (Note 1)		-		1	μs
Detection (Note 1) -	RENT DETECTION (LX Pin)		I	1		
Image: Negative LX detection voltage Vmust be within dead time limits) Negative LX detection voltage Vbdls Positive LX detection voltage Vbdhs O.2 0.5 Time for Vth adjustment and settling time (Note 1) 300 kHz Initial Negative Current Detection LX-GND, Includes ± 2 mV Offset Range		Blanking Time after LG is < 1.0 V	-	_	40	ns
Positive LX detection voltage Vbdhs 0.2 0.5 1 Time for Vth adjustment and settling time (Note 1) 300 kHz 3.0 - 3.0 - 3.0 Initial Negative Current Detection LX-GND, Includes ± 2 mV Offset Range - 1.0 1.0	e for LX Voltage (Note 1)		-	-	20	ns
Time for V _{th} adjustment and settling time (Note 1) 300 kHz 3.0 - 3.0 Initial Negative Current Detection LX–GND, Includes ± 2 mV Offset Range - 1.0	detection voltage	V _{bdls}	150	300	450	mV
(Note 1) Initial Negative Current Detection LX-GND, Includes ± 2 mV Offset Range - 1.0	detection voltage	V _{bdhs}	0.2	0.5	1.0	V
	adjustment and settling time	300 kHz	3.0	-	3.7	μs
	ve Current Detection oltage Set Point (Note 1)	LX-GND, Includes ± 2 mV Offset Range	-	1.0	-	mV
V _{th} adjustable Range (Note 1) -16 0	le Range (Note 1)		-16	0	15	mV
HIGH SIDE DRIVER UG	DRIVER UG		-	-	-	-
$R_{H TG}$ Output Resistance, Sourcing $V_{BOOT} - V_{LX} = 12 V$, $C_{load} = 3 nF$, $V_{CC} = 12 V$ - 2.5	ut Resistance, Sourcing	V_{BOOT} – V_{LX} = 12 V, C_{load} = 3 nF, V_{CC} =12 V	-	2.5	5	Ω

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated: $-40^{\circ}C < T_A < 85^{\circ}C$; 4.5 V < VCC < 13.2 V; $C_{VCC} = 0.1 \ \mu F$

Parameter	Test Conditions	Min	Тур	Max	Unit
HIGH SIDE DRIVER UG		-	-		
R _{H_TG} Output Resistance, Sinking	$V_{BOOT} - V_{LX}$ = 12V, V_{CC} =12 V	-	2.0	2.5	Ω
Tr _{DRVH} Transition Time	C_{LOAD} = 2 nF, V_{CC} =12 V	-	16	-	ns
Tf _{DRVH} Transition Time	C_{LOAD} = 2 nF, V_{CC} =12 V	-	11	-	ns
Tpdh _{DRVH} Propagation Delay (Notes 1, 2)	Driving High, $C_{LOAD} = 3 \text{ nF}$, V _{CC} = 12 V, V _{CCP} =12 V	-	15	30	ns
UG Internal Resistor to LX	Unbiased, BOOT – LX = 0	-	45	-	kΩ
LOW SIDE DRIVER LG					
R _{H_BG} Output Resistance, Sourcing	V_{LX} = GND, C_{load} = 3 nF, V_{CC} =12 V	-	2.0	3.0	Ω
R _{L_BG} Output Resistance, Sinking	$V_{LX} = V_{CC}, V_{CC} = 12 V$	-	1.0	1.5	Ω
Tr _{DRVL} Transition Time	C_{LOAD} = 3 nF, V_{CC} =12 V	-	16	-	ns
Tf _{DRVL} Transition Time	C_{LOAD} = 3 nF, V_{CC} =12 V	-	11	-	ns
Tpdh _{DRVL} Propagation Delay (Notes 1, 2)	Driving High, C_{LOAD} = 3 nF, V_{CCP} = 12 V, V_{CCP} = 12 V	10	20	35	ns
LX Internal Resistor to GND		-	45	_	kΩ

T _{sd} Thermal Shutdown (Note 1)	150	180	_	°C
T _{sdhys} Thermal Shutdown Hysteresis (Note 1)	-	50	-	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design.

2. For propagation delays, "tpdh" refers to the specified signal going high "tpdl" refers to it going low. Reference Gate Timing Diagram.

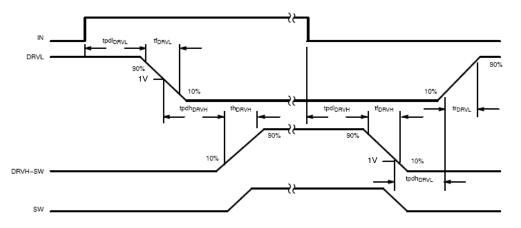


Figure 3. Gate Timing Diagram

Switching Frequency

Connecting a resistor from ROSC/EN to an external voltage source V_{pu} will configure the switching frequency. Normal range would be 100 kHz to 1 MHz. With no resistor connected to the pin, the oscillator frequency is 200 kHz. The switching frequency will follow the relationship:

$$F_{SW} = 200 \text{ kHz} - \frac{V_{pu} - 1.240}{R_{OSC}} \cdot 10 \frac{\text{kHz}}{\mu\text{A}} \tag{eq. 1}$$

When R_{osc} = infinity (no resistor connected), F_{sw} = 200 kHz; when V_{pu} = ground, the frequency programmed will be higher than 200 kHz. Pulling R_{osc} /EN pin to ground solidly with a less than 10 k Ω resistor will result in the part being disabled.

Soft-Start

Soft–Start will begin if VCC, VCCP are both above their UVLO thresholds and EN pin is set free. IC initially waits a fixed delay time and then ramps the reference in 5.12 ms (1024 clock cycles when R_{osc} open) in closed–loop regulation. After soft–start, PGOOD signal will be released with 3 clock cycles delay.

Protection active during soft-start:

- Overvoltage Protection always enabled;
- Undervoltage Protection is enabled after reference voltage ramps up to 80% of the final value. During soft-start, a UVP fault will initiate a complete soft restart.

Synchronization Function

Synchronize through the SYNC pin. Synchronization function allows different converters to share the same input filter reducing the resulting RMS current and reducing the need for total caps to sustain the load. Synchronized systems also exhibit higher EMI noise immunity and better regulation.

The device synchronizes to the Falling edge of the SYNC pin external input signal (eg. high side gate signal, switch node signal, distribution clock signal), and locks the phase of an internal ramp signal correspondingly with a fixed delay time. The external signal has to sit within a 0-40% frequency window above the local frequency configured by the R_{osc} resistor to allow the synchronization function working properly.

Power Good

The PGOOD pin is an open drain connection with no internal pullup resistor. An active high output signals the normal operation of the converter. PGOOD is pulled low during soft-start cycle, and if there is an overvoltage or undervoltage fault. If the voltage on the VSEN pin is within $\pm 10\%$ of Vref (0.8 V) then the PGOOD pin will not be pulled low.

Overvoltage Protection (OV)

If the voltage on the VSEN pin exceeds the overvoltage threshold (1000 mV or 125% Vref), the NCP81147 will latch an overvoltage fault. During an overvoltage fault event the UG pin will be pulled low, and the LG pin will stay high until the voltage on the VSEN pin goes below 400 mV or 50% V_{ref} , then a soft-bleeding resistor will be connected from switch node to ground to continuously discharge the output voltage softly. To clear the overvoltage fault, toggling VCC or EN is needed.

Undervoltage Protection (UV)

If the voltage on the FB pin falls below the undervoltage threshold after the softstart cycle completes, the NCP81147 will latch an undervoltage fault. During an undervoltage fault, both the UG and LG pins will be pulled low. Toggling VCC power or EN will reset the undervoltage protection.

PreOVP Protection

If the NCP81147 is powered on but not enabled, the VSEN pin will be monitored for preOVP condition. If the VSEN exceeds the preset threshold, the device will force LG pin high to protect the load. The PreOVP function will be disabled when the device is enabled and the normal OV function will operate instead.

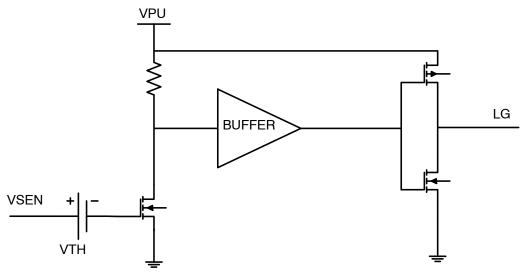


Figure 4. PreOVP circuit

Vin Detection

During the soft start after the VSEN pin exceeds 80% V_{ref}, UV protection will be enabled; If a UV fault is triggered in the softstart, it will restart SS after a fixed delay. The UV protection is to avoid IC to startup without Vin or with insufficient Vin voltage.

Overcurrent Protection

NCP81147 measures the differential current sensing signal through CSP and CSN/VO pin. There are two current protection levels: OCP1 and OCP2. If the differential voltage across pin CSP and CSN/VO is over 20 mV (but below 30 mV) for four consecutive cycles, OCP1 will be tripped. Both UG and LG will be forced to low to turn off the high side and low side FETs, it is a latched condition; If the differential voltage across pin CSP and CSN is over 30 mV,

OCP2 will be tripped, the UG and LG will be pulled low and latched immediately. Toggling VCC power or EN will reset the Overcurrent protection.

The current sensing R/C network should be selected to match the inductor time constant as below,

$$(\text{RCS1}//\text{RCS2}) \cdot \text{C} = \frac{\text{L}}{\text{DCR}}$$

(Notes: the actual RC network time constant may be slightly higher)

Thus, OCP1 and OCP2 levels can be configured as,

$$OCP1 = \frac{20 \text{ mV}}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$
$$OCP2 = \frac{30 \text{ mV}}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$

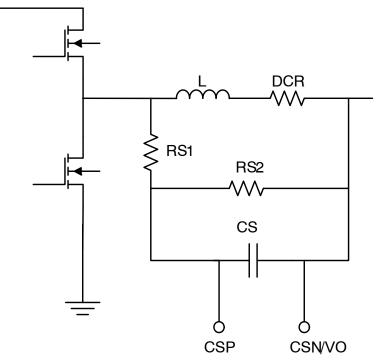


Figure 5. Differential Current Sense Network

Light Load Operation

In the light load condition, NCP81147 will work in a diode emulation mode with bottom gate turning off if the inductor current is below zero. The system therefore works in discontinuous conduction mode (DCM). The zero current detection is done by sensing switch node and automatically adjusted to minimize the low side FET body diode conduction time (right after LG turns off) in diode emulation mode.

If the load reduces further, COMP signal will be close or below the internal ramp bottom triggering minimum on time operation, the system will start skipping pulses, working in a reduced frequency range. NCP81147 has an internal ultrasonic timer to keep the device from working in an audio frequency and below. This timer initiates after high side gate off signal and expires after ~30 μ s.

Normally high side gate signal will reset this ultrasonic timer repeatedly before it expires. In a very light load or load release, if there is no high side gate pulses until the timer expires, the low side MOSFET(s) will be forced to turn on to discharge the output. Through properly compensated network the comp signal will climb up to generate next burst of switching pulses and the converter will regulate the output voltage to its target level. This can last a few cycles or continuously depending on the system load level.

In light load operation, if synchronization is enabled, NCP81147 will also check the SYNC pin input signal cycle by cycle. If the external sync signal is within the synchronization frequency range, the NCP81147 will interleave its switching pulses with it after a proper delay. In this way, the ripple variation during transition between the discontinuous and continuous current mode can be minimized.

Voltage Feedback

The NCP81147 allow the output voltage to be adjusted from 0.8 V to 5 V via an external resistor divider network (R1, R2). The controller will regulate the output voltage to maintain the FB pin voltage to 0.8 V reference voltage. The relation between the resistor divider network and the output voltage is as below;

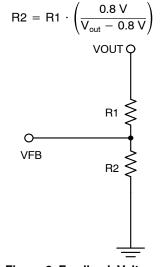
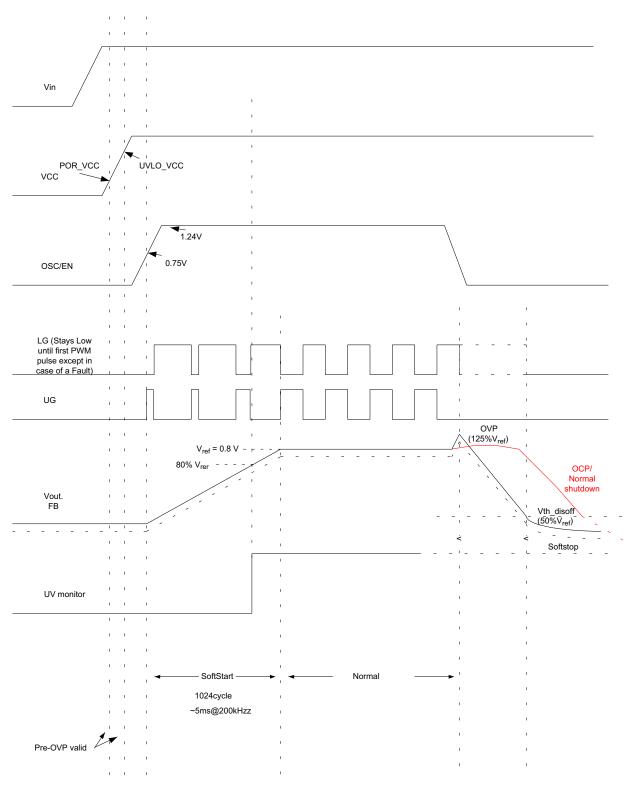
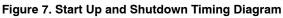


Figure 6. Feedback Voltage





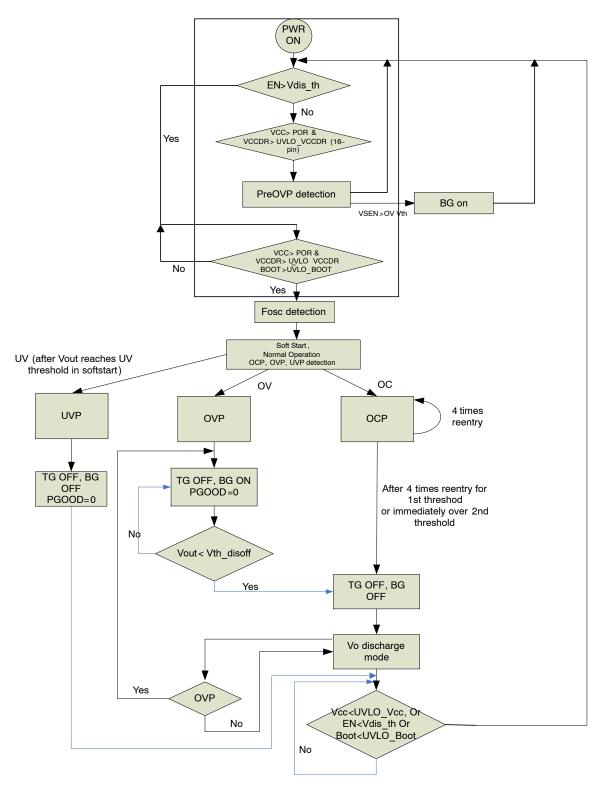
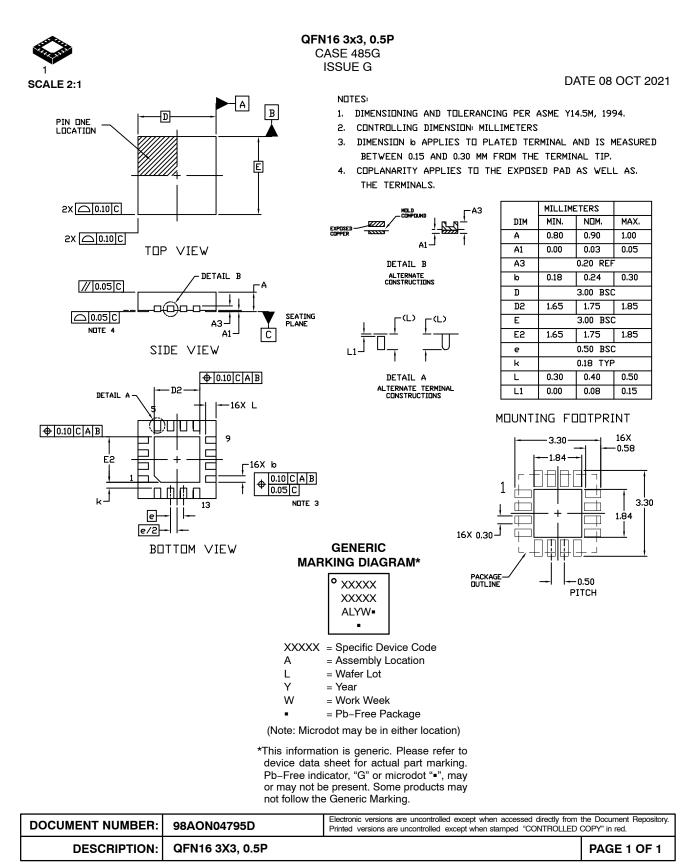


Figure 8. State Diagram

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