NCP81140

Multiple-Phase Controller with SVID Interface for Desktop and Notebook CPU Applications

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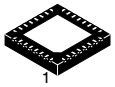

QFN32
CASE 510AT

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information page 18 of this data sheet.

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The NCP81140 Multi−Phase buck solution is optimized for Intel® VR12.5 compatible CPUs with user configurations of 4/3/2/1 phases. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing the fastest initial response to dynamic load events at reduced system cost. It has the capability to shed to single phase during light load operation and can auto frequency scale in light load conditions while maintaining excellent transient performance.

High performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate digital current monitoring.

Features

- Meets Intel® VR12.5 Specifications
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- “Lossless” DCR Current Sensing for Current Balancing
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 280 kHz – 600 kHz
- Startup into Pre−Charged Loads While Avoiding False OVP
- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- VR−RDY Output with Internal Delays
- These are Pb−Free Devices

Applications

- Desktop and Notebook Processors

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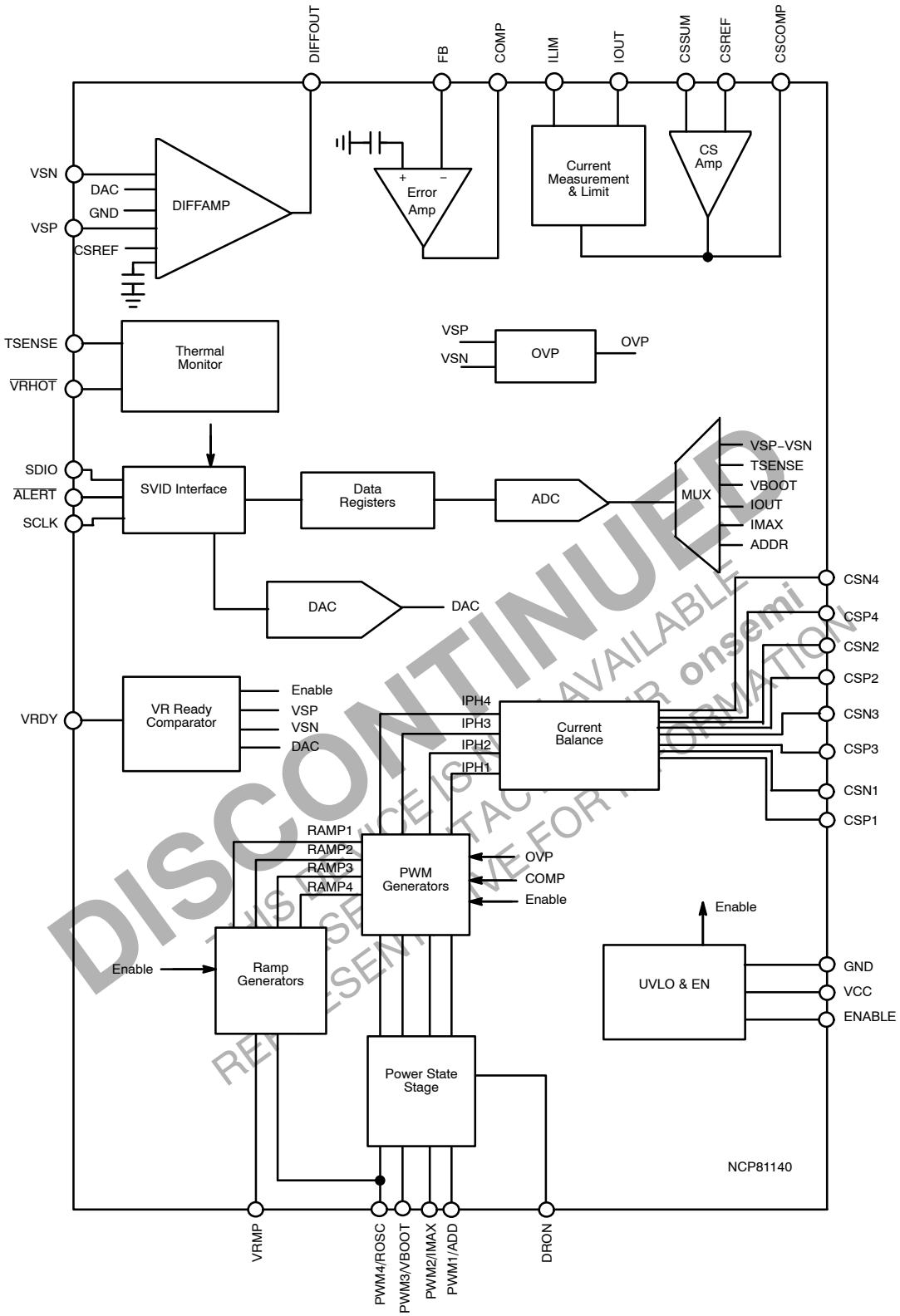

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Figure 1. Block Diagram for NCP81140

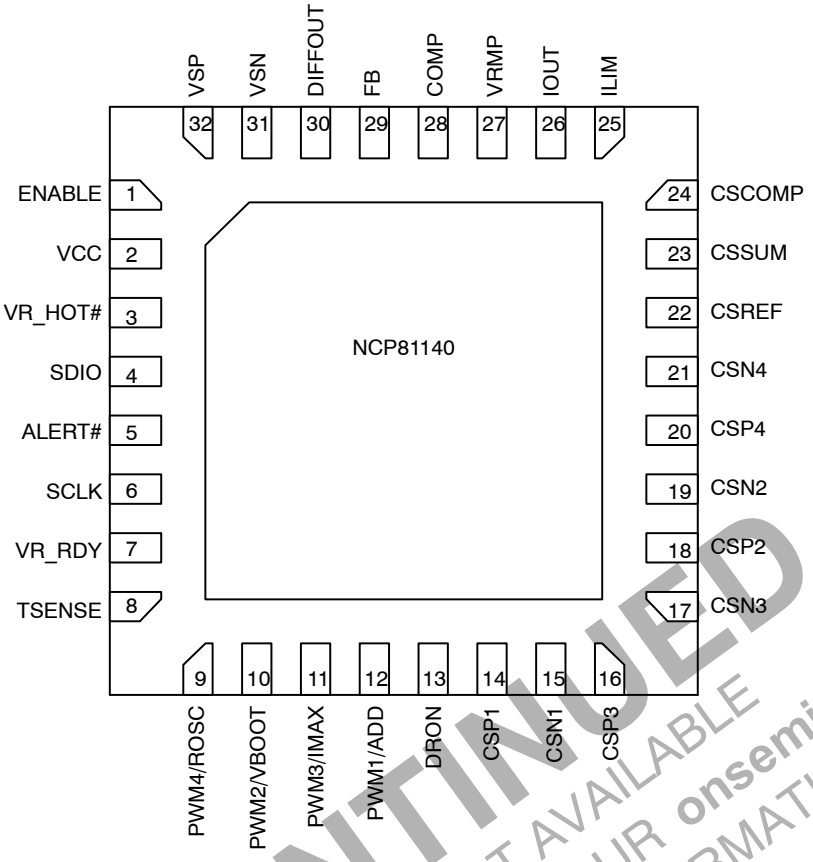

Figure 2. NCP81140 Pin Configurations

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NCP81140 PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	ENABLE	Logic input. Logic high enables the output and logic low disables the output.
2	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
3	VR_HOT#	Thermal logic output for over temperature
4	SDIO	Serial VID data interface
5	ALERT#	Serial VID ALERT#.
6	SCLK	Serial VID clock
7	VR_RDY	Open drain output. High indicates that the output is regulating
8	TSENSE	Temp Sense input for the multiphase converter
9	PWM4/ROSC	Phase 4 PWM output. A resistance from this pin to ground programs the oscillator frequency
10	PWM2/VBOOT	Phase 2 PWM output. Also as VBOOT input pin to adjust the boot−up voltage. During start up it is used to program VBOOT with a resistor to ground
11	PWM3/IMAX	Phase 3 PWM output. Also as ICC_MAX Input Pin. During start up it is used to program ICC_MAX with a resistor to ground
12	PWM1/ADD	Phase 1 PWM output. Also as Address program pin. A resistor to ground on this pin programs the SVID address of the device
13	DRON	Bidirectional gate drive enable output
14	CSP1	Non−inverting input to current balance sense amplifier for phase 1
15	CSN1	Inverting input to current balance sense amplifier for phase 1
16	CSP3	Non−inverting input to current balance sense amplifier for phase 3

NCP81140 PIN DESCRIPTIONS

Pin No.	Symbol	Description
17	CSN3	Inverting input to current balance sense amplifier for phase 3. Pull this Pin to VCC, configure as 1−phase operation
18	CSP2	Non−inverting input to current balance sense amplifier for phase 2
19	CSN2	Inverting input to current balance sense amplifier for phase 2. Pull this Pin to VCC, configure as 2−phase operation
20	CSP4	Non−inverting input to current balance sense amplifier for phase 4
21	CSN4	Inverting input to current balance sense amplifier. Pull this Pin to VCC, configure as 3−phase operation
22	CSREF	Total output current sense amplifier reference voltage input, a capacitor on this pin is used to ensure CSREF voltage signal integrity
23	CSSUM	Inverting input of total current sense amplifier
24	CSCOMP	Output of total current sense amplifier
25	ILIM	Over current shutdown threshold setting. Resistor to CSCOMP to set threshold
26	IOUT	Total output current monitor.
27	VRMP	Feed−forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope
28	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators
29	FB	Error amplifier voltage feedback
30	DIFFOUT	Output of the differential remote sense amplifier
31	VSN	Inverting input to differential remote sense amplifier
32	VSP	Non−inverting input to the differential remote sense amplifier
33	FLAG / GND	Power supply return (QFN Flag)

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ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	V_{MAX}	V_{MIN}
COMP	VCC + 0.3 V	−0.3 V
CSCOMP	VCC + 0.3 V	−0.3 V
VSN	GND + 300 mV	GND − 300 mV
DIFFOUT	VCC + 0.3 V	−0.3 V
VR_RDY	VCC + 0.3 V	−0.3 V
VCC	6.5 V	−0.3 V
IOUT	2.0 V	−0.3 V
VRMP	+25 V	−0.3 V
All Other Pins	VCC + 0.3 V	−0.3 V

*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 1)	$R_{\theta JA}$	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to 125	°C
Operating Ambient Temperature Range		−40 to 100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Max Power Dissipation	Pd	110 to 131	mW
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

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ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current	@ 1.3 V	−27		+27	μA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 kΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V − 2.5 V, CL = 20 pF to GND, DC Load = 10k to GND		20		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5			V
Minimum Output Voltage	I_{SINK} = 2.0 mA			1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current	VSP, VSN = 1.3 V	−15		15	uA
VSP Input Voltage Range		−0.3		3.0	V
VSN Input Voltage Range		−0.3		0.3	V
−3dB Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND		10		MHz
Closed Loop DC gain	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		−300		300	μV
Input Bias Current	CSSUM = CSREF= 1 V	−10		10	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
CURRENT BALANCE AMPLIFIER					
Maximum CSCOMP Output Voltage	I_{source} = 2 mA	3.5			V
Minimum CSCOMP Output Voltage	I_{sink} = 500 μA			0.1	V
Input Bias Current	CSP_{1-4} = CSN_{1-4} = 1.2	−50		50	nA
Common Mode Input Voltage Range	CSPx = CSNx	0		2.3	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100		100	mV
Input Offset Voltage Matching	CSPx = CSNx = 1.2 V, Measured from the average	−1.5		1.5	mV
Current Sense Amplifier Gain	0 V < CSPx − CSNx < 0.1 V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSP−CSN = 10 mV to 30 mV	−3		3	%
−3dB Bandwidth			8		MHz
INPUT SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	EN = high, PS0,1,2 Mode		25		mA
	EN = high, PS3 Mode		15		mA
	EN = low		30		μA

3. Guaranteed by design or characterization data, not in production test.

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Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT SUPPLY					
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			V
VCC UVLO Hysteresis			160		mV
UVLO Threshold	VRMP rising			4.2	V
	VRMP failing	3			V
DAC SLEW RATE					
Soft Start Slew Rate			5		mv/μs
Slew Rate Slow			5		mv/μs
Slew Rate Fast			20		mv/μs
ENABLE INPUT					
Enable High Input Leakage Current	External 1k pull−up to 3.3 V			1.0	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.3	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		90		mV
Enable Delay Time	Measure time from Enable transitioning HI to when DRON goes high			5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0			V
Output Low Voltage	Sinking 500 μA			0.1	V
Rise Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		156		ns
Fall Time			55		ns
Internal Pull Down Resistance	EN = Low		70		kΩ
IOUT OUTPUT					
Input Referred Offset Voltage	Ilimit to CSREF	−3.5		+3.5	mV
Output Source Current	Ilimit sink current = 80 μA			850	μA
Current Gain	($IOUT_{CURRENT}$) / ($ILIMIT_{CURRENT}$), R_{ILIM} = 20k, R_{IOUT} = 5.0k , DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	
OSCILLATOR					
Switching Frequency Range		290		590	KHz
4 Phase Operation				590	kHz
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Absolute Over Voltage Threshold During Soft Start	CSREF	2.75	2.9	3	V
Over Voltage Threshold Above DAC	VSP rising	350	400	425	mV
Over Voltage Delay	VSP rising to PWMx low		50		ns
Under Voltage	Ckt in development		300		mV
Under−voltage Delay	Ckt in development		5		μs

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Parameter	Test Conditions	Min	Typ	Max	Unit
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS0) Rlim = 20k	9.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	(PS0) Rlim = 20k	13.5	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS1, PS2, PS3) Rlim = 20k, N = number of phases in PS0 mode		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	(PS1, PS2, PS3) Rlim = 20k, N = number of phases in PS0 mode		15/N		μA
MODULATORS (PWM Comparators)					
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP = 12.0 V		2.5		V
PWM Ramp Duty Cycle Matching	COMP = 2 V, PWM Ton matching		1		%
PWM Phase Angle Error	Between adjacent phases at 25°		5		°
Ramp Feed−forward Voltage range		5		20	V
VR_HOT#					
Output Low Voltage	$I_{\_VRHOT}$ = −4 mA			0.3	V
Output Leakage Current	High Impedance State	−1.0		1.0	μA
TSENSE					
Alert# Assert Threshold			491		mV
Alert# De−assert Threshold			513		mV
VRHOT Assert Threshold			472		mV
VRHOT Rising Threshold			494		mV
TSENSE Bias Current		115	120	125	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1		+1	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			±1		%
Conversion Time			30		μs
Round Robin			90		μs
VR_RDY, (Power Good) OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA			0.3	V
Rise Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%		100		ns
Fall Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%		10		ns
Output Voltage at Power−up	VR_RDY pulled up to 5 V via 2 kΩ		1.0		V
Output Leakage Current When High	VR_RDY = 5.0 V	−1.0		1.0	μA
VR_RDY Delay (rising)	DAC=TARGET to VR_RDY		5		μs
VR_RDY Delay (falling)	From OCP or OVP		5		μs

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Parameter	Test Conditions	Min	Typ	Max	Unit
PWM OUTPUTS					
Output High Voltage	Sourcing 500 μA	V_{CC} − 0.2	–	–	V
Output Mid Voltage	No Load, SetPS = 02	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA			0.7	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo = GND to VCC		10		ns
PHASE DETECTION					
CSN Pin Threshold Voltage			4.5		V
Phase Detect Timer			50		μs

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STATE TRUTH TABLE

STATE	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	DRON Pin	Method of Reset
POR 0 < VCC < UVLO	N/A	N/A	N/A	Resistive pull down	
Disabled EN < threshold UVLO > threshold	Low	Low	Disabled	Low	
Start up Delay & Calibration EN > threshold UVLO > threshold	Low	Low	Disabled	Low	
DRON Fault EN > threshold UVLO > threshold DRON < threshold	Low	Low	Disabled	Resistive pull up	Driver must release DRON to high
Soft Start EN > threshold UVLO > threshold DRON > High	Low	Operational	Active / No latch	High	
Normal Operation EN > threshold UVLO >threshold DRON > High	High	Operational	Active / Latching	High	N/A
Over Voltage	Low	N/A	DAC + 150 mV	High	
Over Current	Low	Operational	Last DAC Code	Low	
V_{OUT} = 0 V	Low: if Reg34h:bit0 = 0; High:if Reg34h:bit0 = 1	Clamped at 0.9 V	Disabled	High, PWM outputs in low state	

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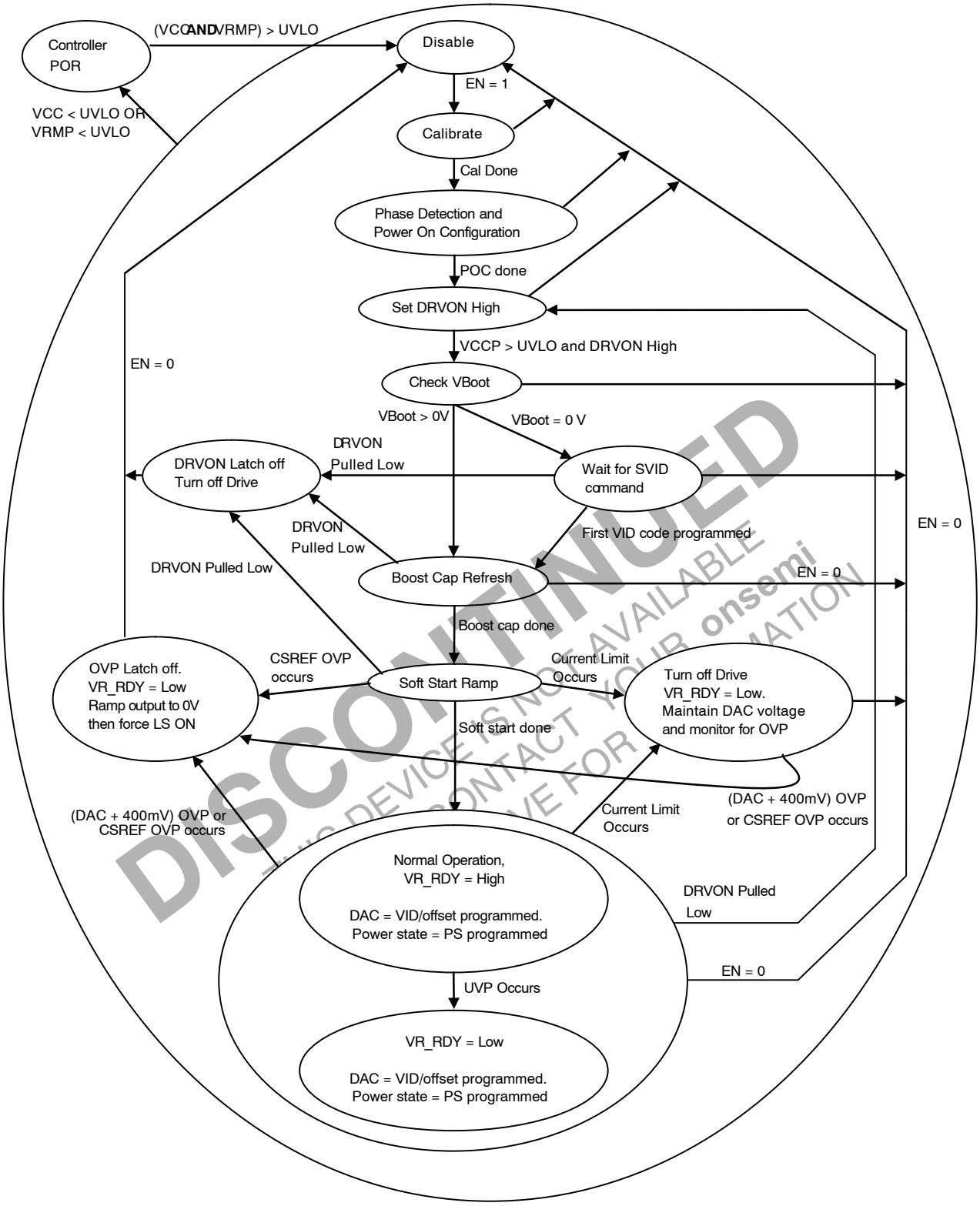

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Figure 3.

General

The NCP81140 is a four phase dual edge modulated multiphase PWM controller, designed to meet the Intel VR12.5 specifications with a serial SVID control interface. It is designed to work in notebook, desktop, and server applications.

Serial VID interface (SVID)

For SVID Interface communication details please contact Intel Inc.

BOOT VOLTAGE PROGRAMMING

The NCP81140 has a Vboot voltage that can be externally programmed. The Boot voltage for the NCP81140 is set using VBOOT pin on power up. A 10uA current is sourced from the VBoot pin and the resulting voltage is measured. This is compared with the thresholds in table below. This value is set on power up and cannot be changed after the initial power up sequence is complete.

BOOT VOLTAGE TABLE

R	VBoot	Phase Number in PS1
30.1k	0 V	1
49.9k	1.65 V	1
69.8k	1.70 V	1
90.9k	1.75 V	1
130k	0 V	2
150k	1.65 V	2
169k	1.70 V	2
Open	1.75 V	2

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

Addressing Programming

The NCP81140 supports 9 possible SVID device addresses. Pin 12 (PWM1/ADDR) is used to set the SVID address. On power up a 10uA current is sourced from this pin through a resistor connected to this pin and the resulting voltage is measured. Table below provides the resistor values for each corresponding SVID address. The address value is latched at startup.

SVID Address Table

Resistor Value	SVID Address
10k	0000
22k	0001
36k	0010
51k	0011
68k	0100
91k	0101
120k	0110
160k	0111
220k	1000

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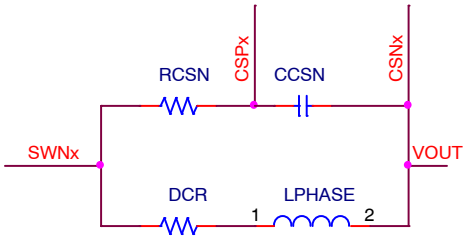
Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

Figure 4.

Total Current Sense Amplifier

The NCP81140 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground, the capacitor is used to ensure that the CSREF voltage signal integrity. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

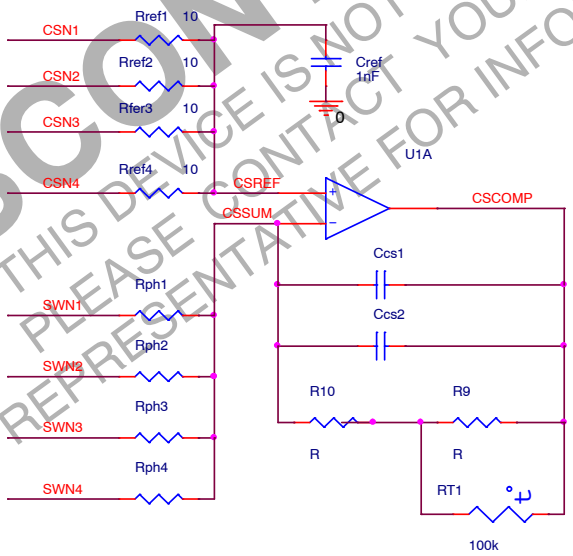


Figure 5.

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1 + Rth}}{Rph} * \left(Iout_{Total} * DCR\right)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100mV across the current limit programming resistor at full load. The values of Rcs1

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and Rcs2 are set based on the 100k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_z = \frac{DCR@25°C}{2 * PI * L_{Phase}}$$

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{LIMIT} * DCR\right) \over 10\mu \quad \text{or} \quad R_{LIMIT} = \frac{IV_{CSCOMP-CSREF@ILIMIT}}{10\mu}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0\ V * R_{LIMIT}}{10 * \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{ICC\_MAX} * DCR\right)}$$

Programming ICC_MAX

A resistor to Ground is monitored on startup and this sets the ICC_MAX value. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10k.

$$ICC\_MAX = \frac{R * 10\ \mu A * 256\ A}{2\ V}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.

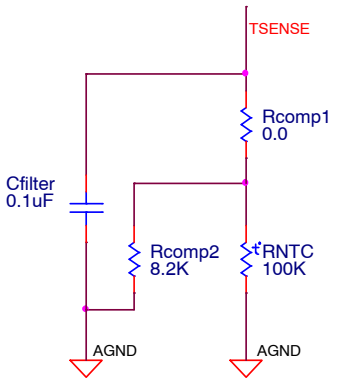

Figure 6.

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Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 280 kHz to 650 kHz on the NCP81140 The graph below lists the resistor options and associated frequency setting.

NCP81140 Operating Frequency vs. R_{osc}

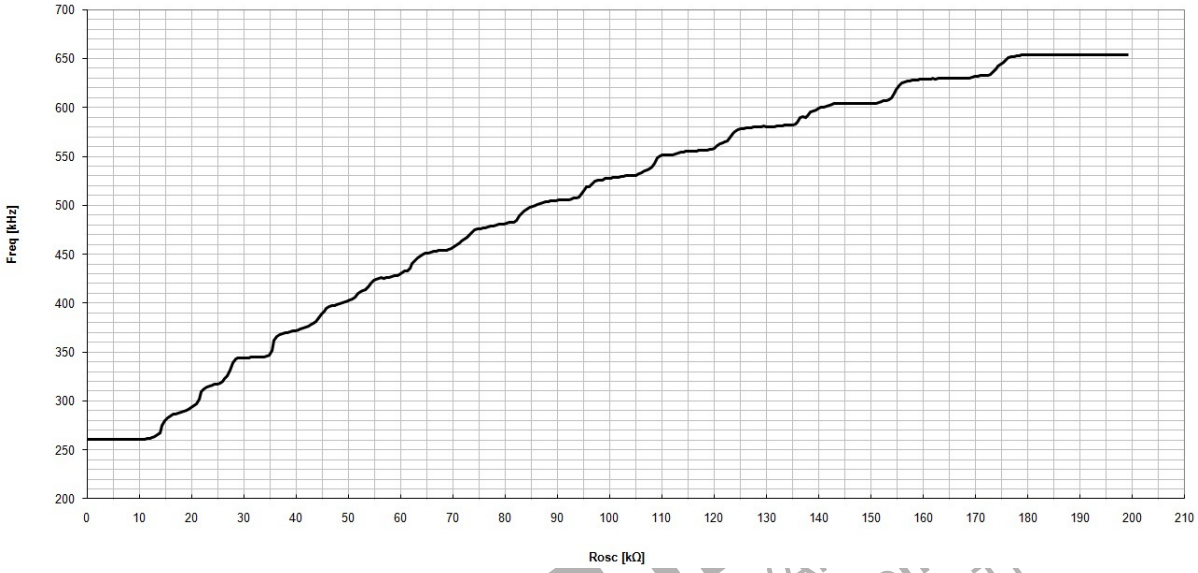


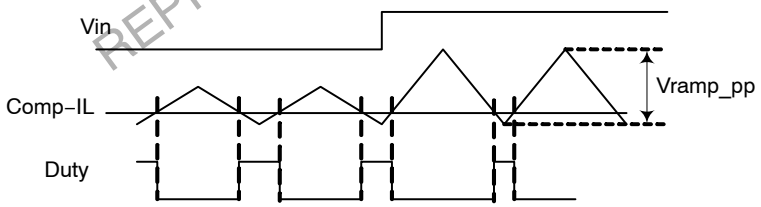
Figure 7. NCP81140 R_{osc} vs. Frequency

The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.
The PWM ramp time is changed according to the following,

$$V_{RAMPpk\Leftarrow pkPP} = 0.1 * V_{VRMP}$$



PWM Comparators

The noninverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (I_L*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

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PHASE DETECTION SEQUENCE

During start−up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the CSN Pins. Normally, NCP81140 operates as a 4−phase Vcore PWM controller. Connecting CSN4 pin to V_{CC} programs 3−phase operation, connecting CSN2 and CSN4 pin to V_{CC} programs 2−phase operation, connecting CSN2, CSN3 and CSN4 pin to V_{CC} programs 1−phase operation. Prior to soft start, while ENABLE is high, CSN4 to CSN2 pins sink approximately 50 μA. An internal comparator checks the voltage of each pin versus a threshold of 4.5 V. If the pin is tied to V_{CC}, its voltage is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval, which takes 30 μs. After this time, if the remaining CSN outputs are not pulled to V_{CC}, the 50 μA current sink is removed, and NCP81140 functions as normal 4 phase controller. If the CSNs are pulled to V_{CC}, the 50 μA current source is removed, and the outputs are driven into a high impedance state.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the NCP5901 and NCP5911 .Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

PROTECTION FEATURES

Under voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81140 monitors the VCC Shunt supply. The gate driver monitors both the gate driver V_{CC} and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off it's startup sequence. In this case the PWM is set to the MID state to begin soft start.

Gate Driver UVLO Restart

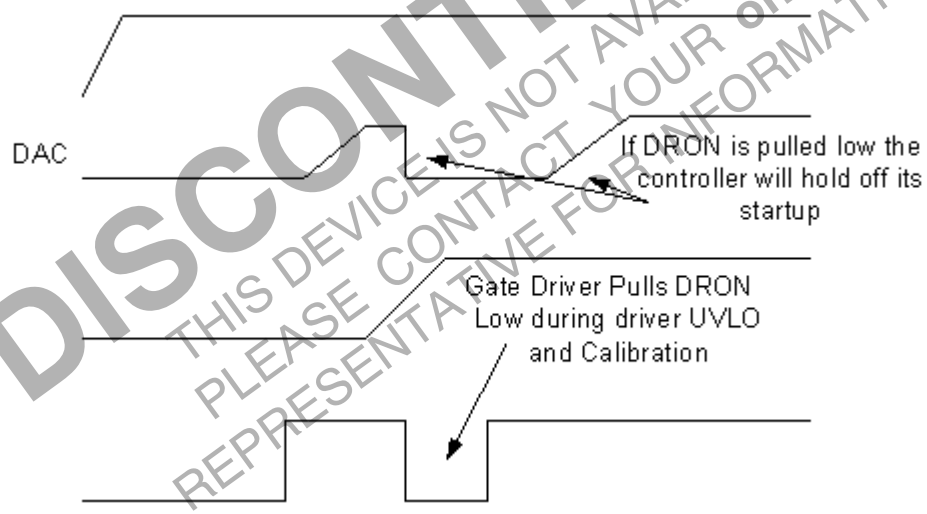

Figure 8.

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Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected, if the controller is enabled the PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state.

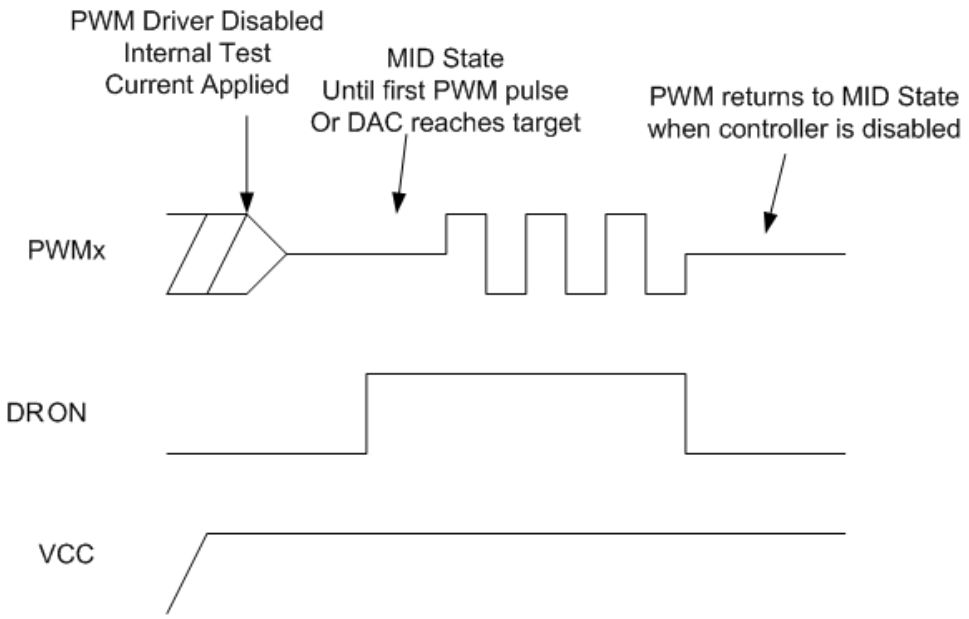

Figure 9.

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Over Current Latch− Off Protection

The NCP81140 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs (shut down immediately for 150% load current) after which the outputs will remain disabled until the V_{CC} voltage or EN is toggled.

On startup a clim1/clim2 current limit protection is enabled once the output voltage has exceeded 250 mV or if the internal DAC voltage has increased above 300 mV, this allow for protection again a Vout short to ground. This is necessary because the voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry.

The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equation:

$$R_{ILIM} = \frac{I_{LIM} * DCR * R_{CS}/R_{PH}}{I_{CL}}$$

Where I_{CL} = 10 μA

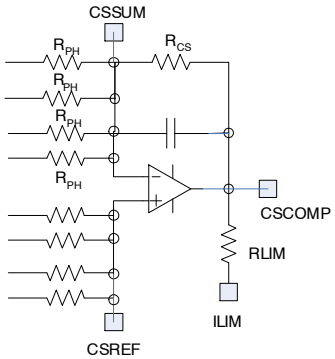

Figure 10.

Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low.

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the DAC will be ramped down to 0 V. At the same time, the high side gate drivers are all turned off and the low side gate drivers are all turned on until the voltage falls to new DAC voltage 0.2 V. The part will stay in this mode until the V_{CC} voltage or EN is toggled.

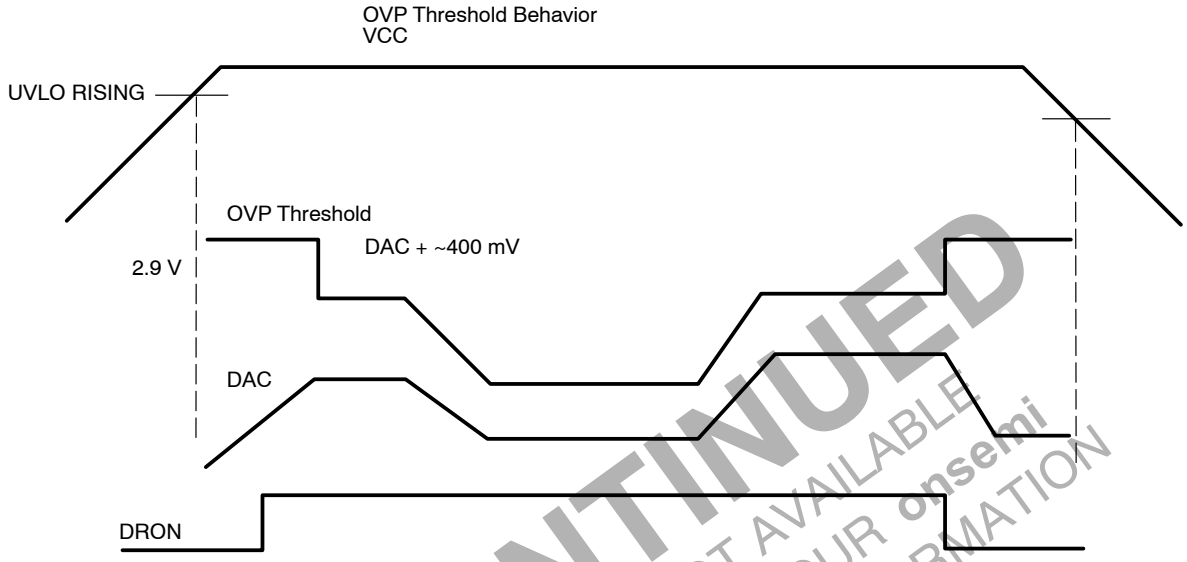

Figure 11. OVP Threshold Behavior

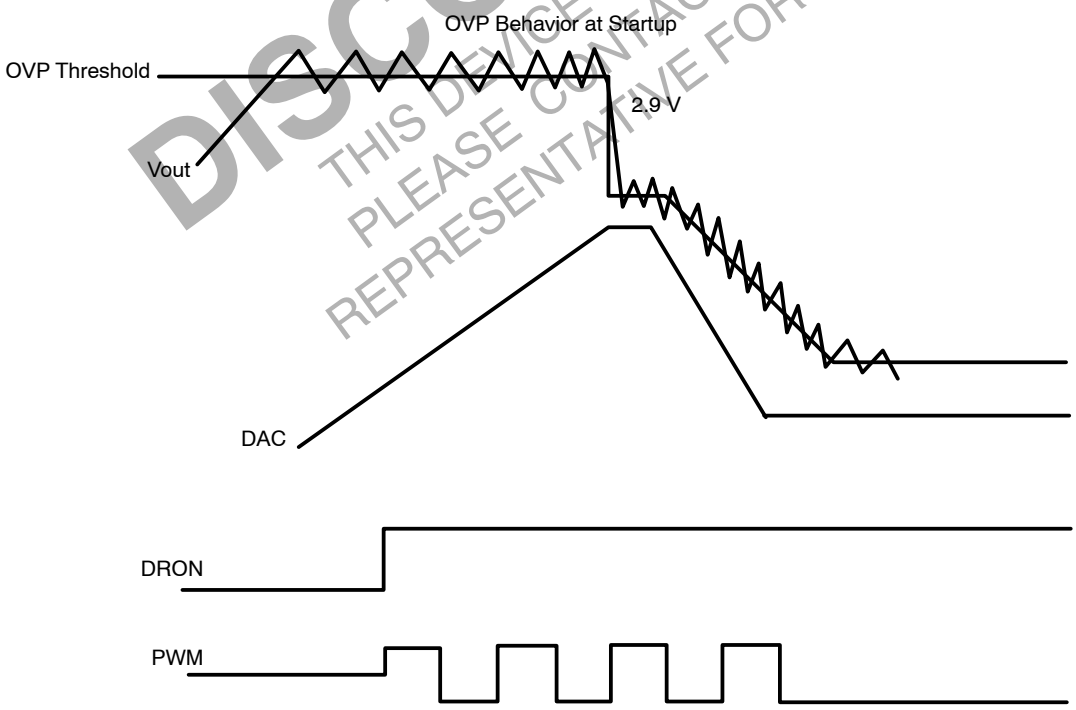

Figure 12. OVP Behavior at Startup

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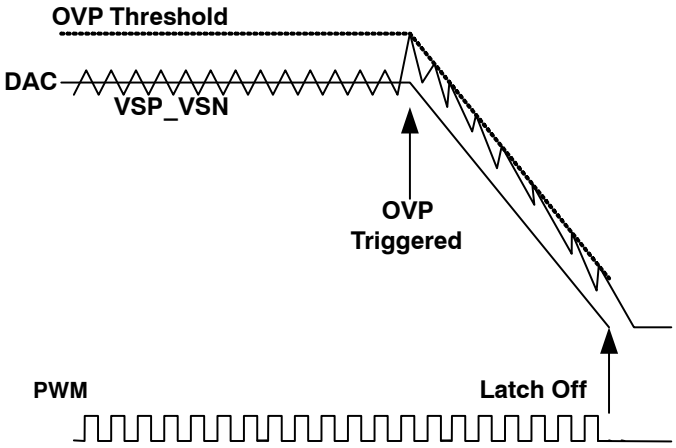

Figure 13. OVP During Normal Operation Mode

During start up, the OVP threshold is set to 2.9 V. This allows the controller to start up without false triggering the OVP.

ORDERING INFORMATION

Device	Package	Shipping†
NCP81140MNTXG	QFN32 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
2	Document Discontinued.	3/10/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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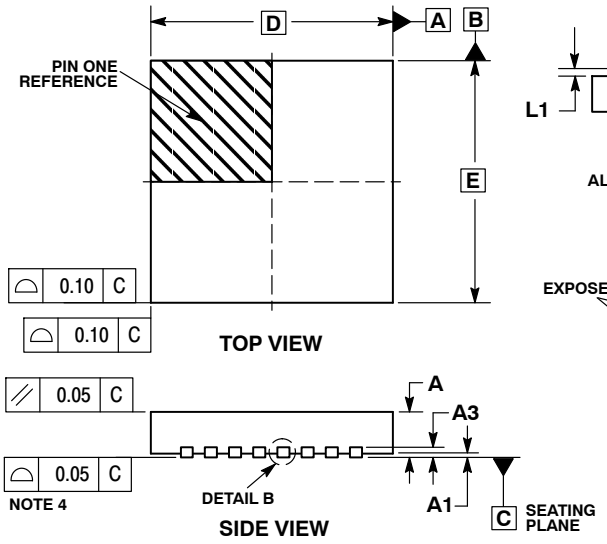
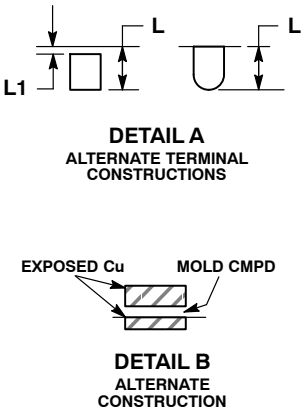
PACKAGE DIMENSIONS

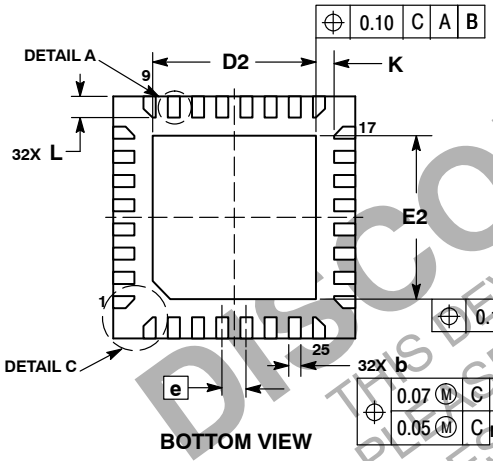
WQFN32 4x4, 0.4P
CASE 510AT
ISSUE O

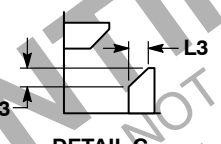




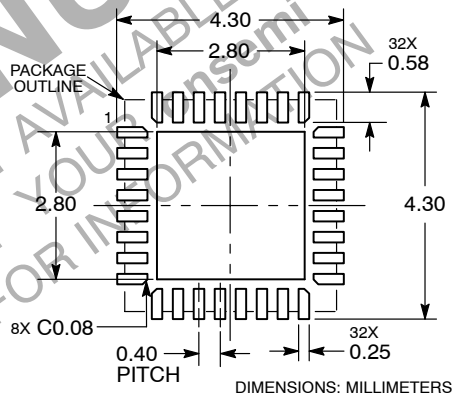
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	---	0.15
L3	0.17 REF	





RECOMMENDED MOUNTING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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