# NCP5395

*Product Preview*

# 2/3/4-Phase Controller with On Board Gate Drivers for CPU Applications

The NCP5395 provides up to a four−phase buck solution which combines differential voltage sensing, differential phase current sensing, adaptive voltage positioning, and on board gate drivers. Dual−edge pulse−width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to dynamic load events. Dual−edge multiphase modulation reduces the total bulk and ceramic output capacitance required to meet transient regulation specifications.

The on board gate drivers includes adaptive non overlap and power saving operation. A high performance operational error amplifier is provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic $V_{ID}$ performance.

**Features**

- Meets Intel's VR11.1 Specifications
- Meets AMD 6 Bit Code Specifications
- Dual−edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Internal Soft Start
- Dynamic Reference Injection (Patent #US07057381)
- DAC Range from 0.5 V to 1.6 V
- DAC Feed Forward Function (Patient Pending)
- ±0.5% DAC Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- Phase−to−Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Oscillator Frequency Range of 125 kHz − 1 MHz
- Latched Over Voltage Protection (OVP)
- Guaranteed Startup into Pre−Charged Loads
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Thermally Compensated Current Monitoring
- Thermal Shutdown Protection
- Adaptive−Non−Overlap Gate Drive Circuit
- Output Disable Control Turn Off of Both Phase Pair MOSFETs
- This is a Pb−Free Device

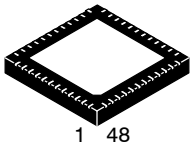
**Applications**

- Desktop Processors

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

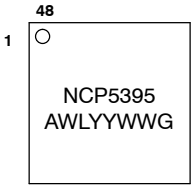
**ON Semiconductor®**

**http://onsemi.com**

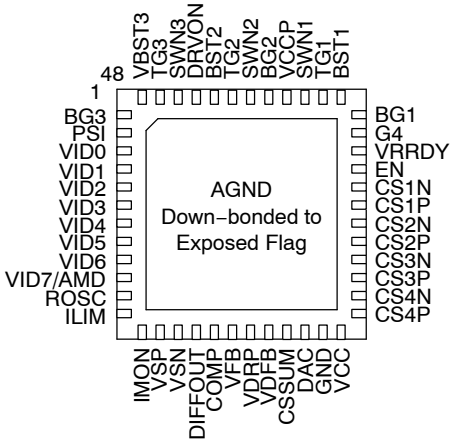



**QFN48**
**CASE 485K**
**PLASTIC**

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP5395MNR2G | QFN48 (Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2008

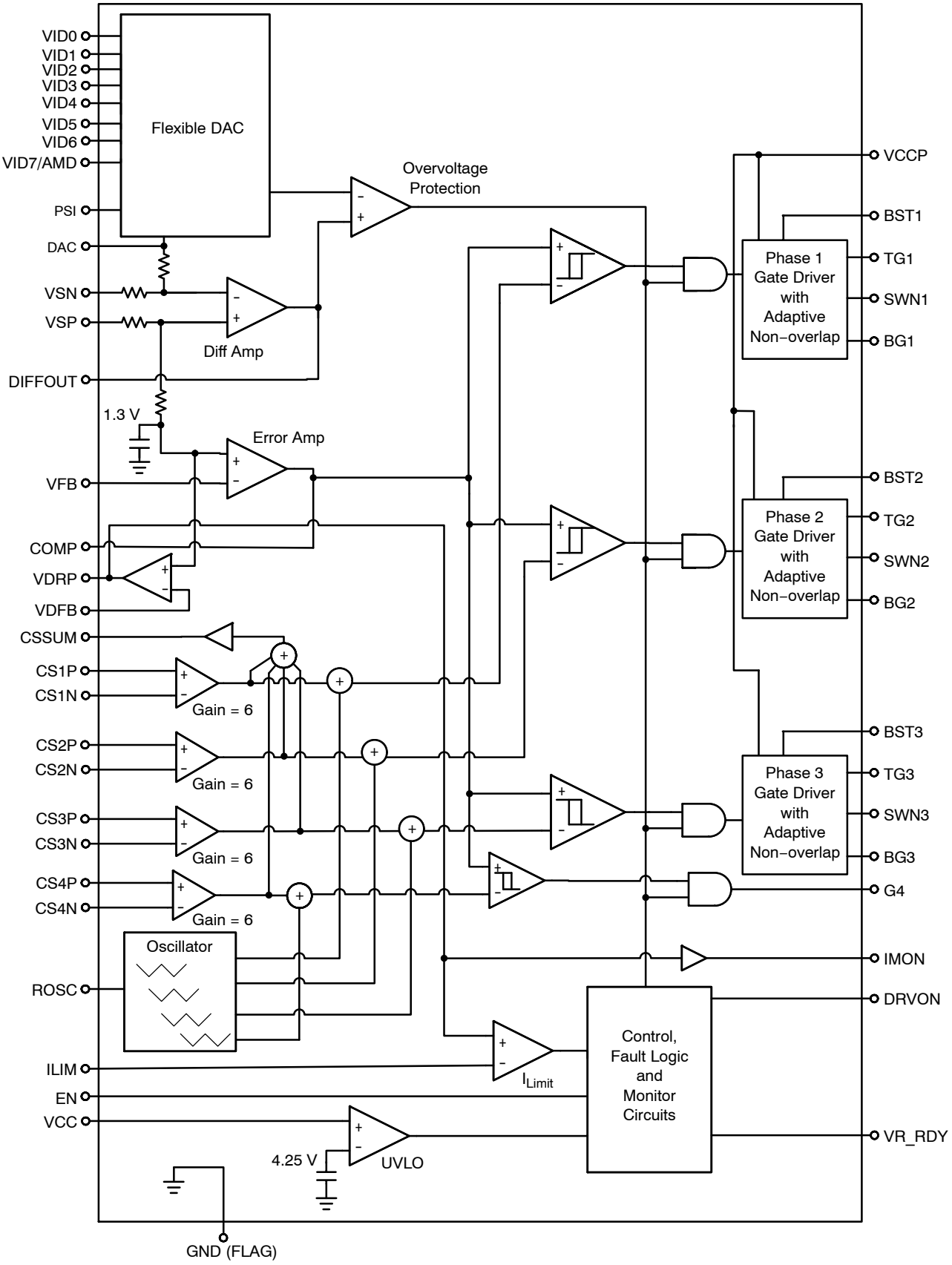



**Figure 1. NCP5395 Functional Block Diagram**

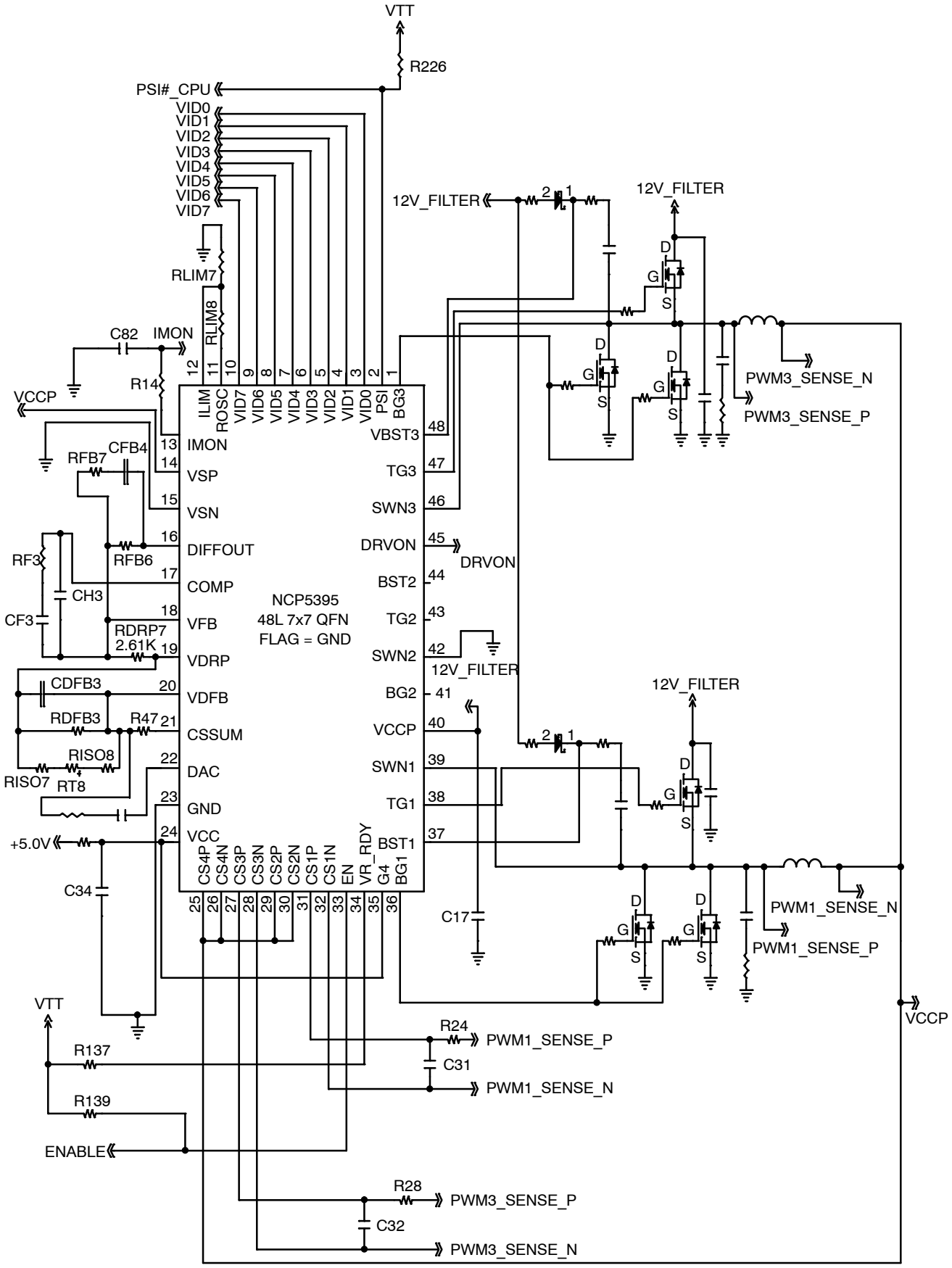



**Figure 2. Typical 2 Phase Application**

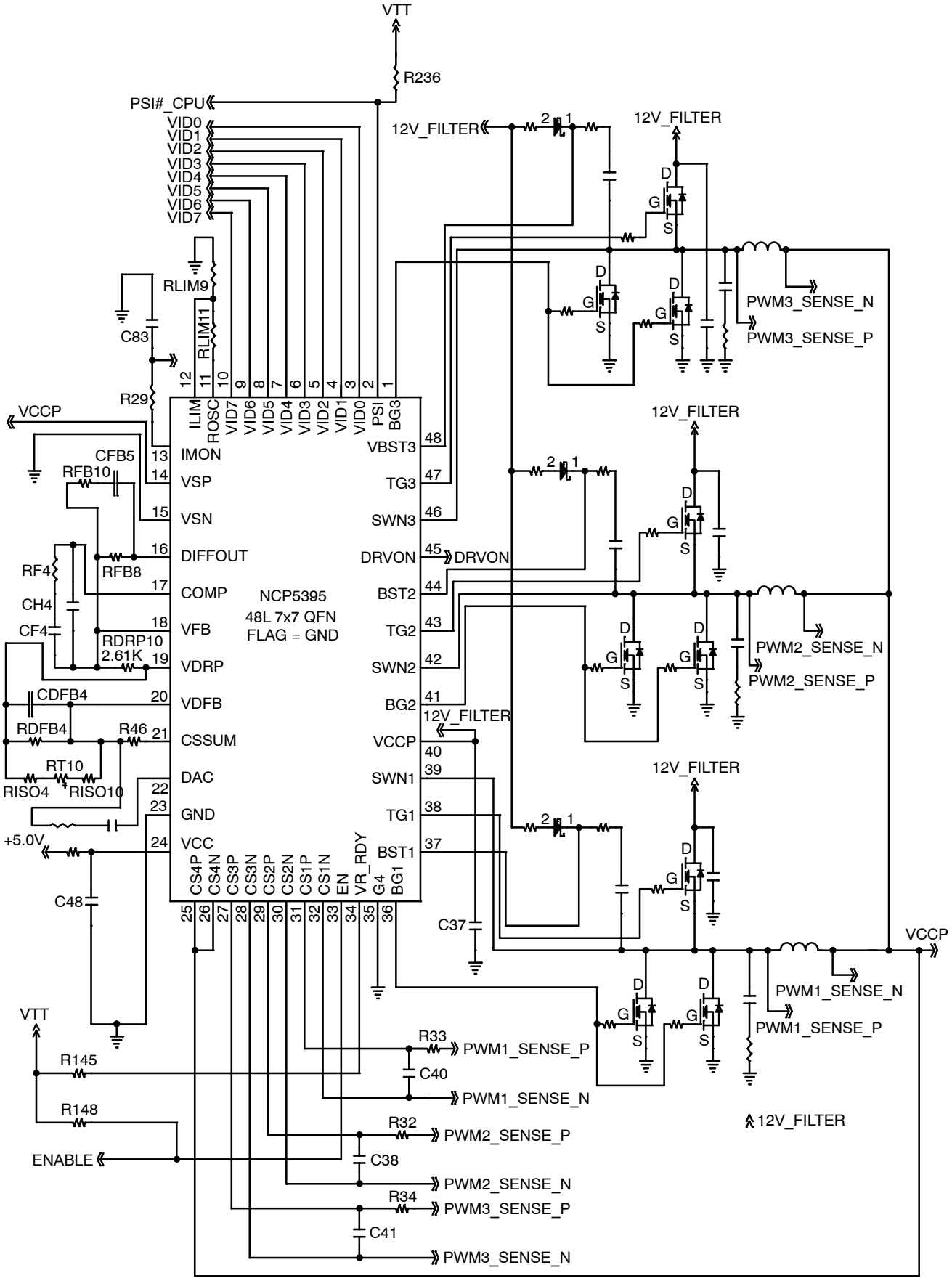



**Figure 3. Typical 3 Phase Application**

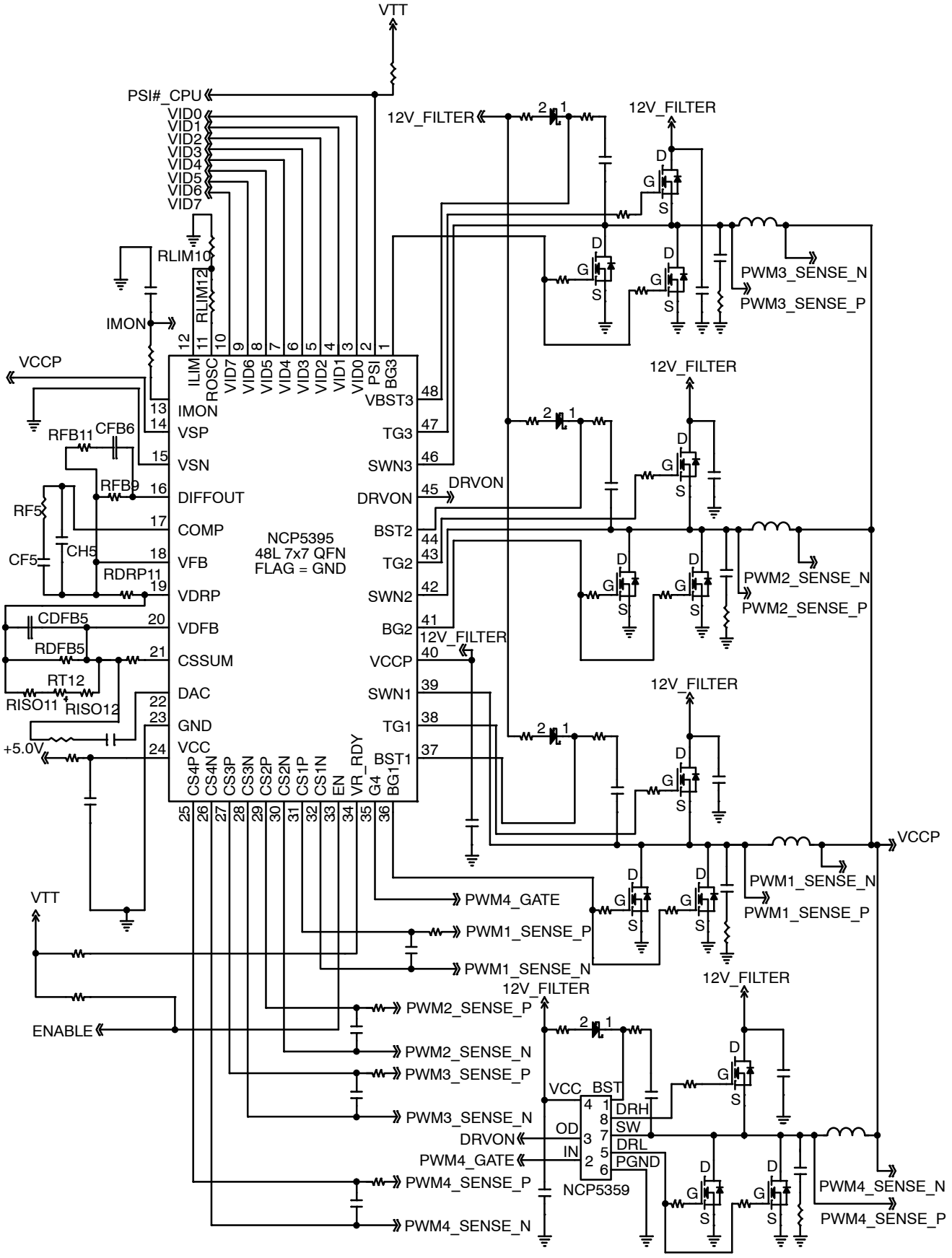



**Figure 4. Typical 4 Phase Application**

**Table 1. Pin Descriptions**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | BG3 | Low side gate drive #3 |
| 2 | PSI | Selects DAC Decode. |
| 3 | VID0 | Voltage ID DAC input |
| 4 | VID1 | Voltage ID DAC input |
| 5 | VID2 | Voltage ID DAC input |
| 6 | VID3 | Voltage ID DAC input |
| 7 | VID4 | Voltage ID DAC input |
| 8 | VID5 | Voltage ID DAC input |
| 9 | VID6 | Voltage ID DAC input |
| 10 | VID7/AMD | Voltage ID DAC input. Pull to $V_{CC}$ (5 V) to enable AMD 6−bit DAC code. |
| 11 | ROSC | A resistance from this pin to ground programs the oscillator frequency and provides a 2 V reference for programming the ILIM voltage. |
| 12 | ILIM | Over current shutdown threshold setting. ILIM = VDRP − 1.3 V. Resistor divide ROSC to set threshold |
| 13 | IMON | 0 to 1 Volt analog signal proportional to the output load current. VSN referenced Clamped to 1.1 Vmax |
| 14 | VSP | Non−inverting input to the internal differential remote sense amplifier |
| 15 | VSN | Inverting input to the internal differential remote sense amplifier |
| 16 | DIFFOUT | Output of the differential remote sense amplifier |
| 17 | COMP | Output of the compensation amplifier |
| 18 | VFB | Compensation amplifier voltage feedback |
| 19 | VDRP | Voltage output signal proportional to current used for current limit and output voltage droop |
| 20 | VDFB | Droop Amplifier Voltage Feedback |
| 21 | CSSUM | Inverted Sum of the Differential Current Sense inputs |
| 22 | DAC | DAC output used to provide feed forward for dynamic VID |
| 23 | GND | Ground |
| 24 | VCC | Power for the internal control circuits with UVLO monitor |
| 25 | CS4P | Non−inverting input to current sense amplifier #4 |
| 26 | CS4N | Inverting input to current sense amplifier #4 |
| 27 | CS3P | Non−inverting input to current sense amplifier #3 |
| 28 | CS3N | Inverting input to current sense amplifier #3 |
| 29 | CS2P | Non−inverting input to current sense amplifier #2 |
| 30 | CS2N | Inverting input to current sense amplifier #2 |
| 31 | CS1P | Non−inverting input to current sense amplifier #1 |
| 32 | CS1N | Inverting input to current sense amplifier #1 |
| 33 | EN | Threshold sensitive input. High = startup, Low =shutdown. |
| 34 | VR_RDY | Open collector output. High indicates that the output is regulating |
| 35 | G4 | PWM output pulse to gate driver. |
| 36 | BG1 | Low side gate drive #1 |
| 37 | BST1 | Upper MOSFET floating bootstrap supply for driver#1 |
| 38 | TG1 | High side gate drive #1 |
| 39 | SWN1 | Switch Node #1 |
| 40 | VCCP | Power $V_{CC}$ for gate drivers with UVLO monitor |
| 41 | BG2 | Low side gate drive #2 |
| 42 | SWN2 | Switch Node #2 |
| 43 | TG2 | High side gate drive #2 |
| 44 | BST2 | Upper MOSFET floating bootstrap supply for driver#2 |
| 45 | DRVON | Bidirectional Gate Drive Enable |
| 46 | SWN3 | Switch Node #3 |
| 47 | TG3 | High side gate drive #3 |
| 48 | BST3 | Upper MOSFET floating bootstrap supply for driver#3 |
| FLAG | GND | Power supply return (QFN Flag) |

**ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL INFORMATION** | | | |
| Controller Power Supply Voltages to GND | $V_{CC}$ | −0.3, 7 | V |
| Driver Power Supply Voltages to GND | $V_{CCP}$ | −0.3, 15 | V |
| High−Side Gate Driver Supplies: BSTx to SWNx | $V_{BST} - V_{SWN}$ | 35 V wrt/GND<br>40 V ≤ 50 ns wrt/GND<br>−0.3, 15 wrt/SWN | V |
| High−Side FET Gate Driver Voltages: TGx to SWNx | $V_{TG} - V_{SWN}$ | BOOT + 0.3 V<br>35 V ≤ 50 ns wrt/GND<br>−0.3, 15 wrt/SWN<br>−2 V (200 ns) | V |
| Switch Node: SWNx | $V_{SWN}$ | 35<br>40 V ≤ 50 ns wrt/GND<br>−5 VDC<br>−10 V (200 ns) | V |
| Low−Side Gate Drive: BGx | $V_{BG}$ − AGND | $V_{CC}$ + 0.3 V<br>−0.3 VDC (200 ns) | V |
| Logic Inputs | $V_{LOGIC}$ | −0.3, 6 | V |
| GND | $V_{GND}$ | 0 | V |
| V− | | GND ±300 | mV |
| Imon Out | $V_{IMON}$ | 1.1 | V |
| All Other Pins | | −0.3, 5.5 | V |
| **THERMAL INFORMATION** | | | |
| Thermal Characteristic<br>QFN Package (Note 1) | $R_{\theta JA}$ | TBD | °C/W |
| Operating Junction Temperature Range (Note 2) | $T_J$ | 0 to 125 | °C |
| Operating Ambient Temperature Range | $T_{AMB}$ | 0 to +70 | °C |
| Maximum Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |
| Moisture Sensitivity Level<br>QFN Package | MSL | 1 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*All signals referenced to GND unless noted otherwise.

*The maximum package power dissipation must be observed.

1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. Operation at −40°C to 0°C guaranteed by design, not production tested.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMPLIFIER** | | | | | |
| Input Bias Current | | −200 | – | 200 | nA |
| Open Loop DC Gain | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 100 | – | dB |
| Open Loop Unity Gain Bandwidth | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 18 | – | MHz |
| Open Loop Phase Margin | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 70 | – | ° |
| Slew Rate | $\Delta V_{in}$ = 100 mV, G = −10V/V, $\Delta V_{out}$ = 1.5 V − 2.5 V, $C_L$ = 60 pF to GND, DC Load = ±125 μA to GND | – | 10 | – | V/μs |
| Maximum Output Voltage | 10 mV of Overdrive, $I_{SOURCE}$ = 2.0 mA | 3.0 | – | – | V |
| Minimum Output Voltage | 10 mV of Overdrive, $I_{SINK}$ = 500 μA | – | – | 75 | mV |
| Output Source Current | 10 mV of Overdrive, $V_{out}$ = 3.5 V | 1.5 | 2.0 | – | mA |
| Output Sink Current | 10 mV of Overdrive, $V_{out}$ = 0.1 V | 0.75 | 1.0 | – | mA |
| **DIFFERENTIAL SUMMING AMPLIFIER** | | | | | |
| V+ Input Pull down Resistance | DRVON = low<br>DRVON = high | –<br>– | 0.6<br>6.0 | –<br>– | kΩ |
| V+ Input Bias Voltage | DRVON = low<br>DRVON = high | –<br>– | 0.5<br>0.86 | –<br>– | V |
| Input Voltage Range (Note 4) | | −0.3 | – | 3.0 | V |
| −3 dB Bandwidth | $C_L$ = 80 pF to GND, $R_L$ = 10 kΩ to GND | – | 15 | – | MHz |
| Closed Loop DC gain VS to Diffout (Note 4) | VS+ to VS− = 0.5 V to 1.6 V | 0.98 | 1.0 | 1.02 | V/V |
| Maximum Output Voltage | 10 mV of Overdrive, $I_{SOURCE}$ = 2 mA | 3.0 | – | – | V |
| Minimum Output Voltage | 10 mV of Overdrive, $I_{SINK}$ = 1 mA | – | – | 0.5 | V |
| Output Source Current | 10 mV of Overdrive, $V_{out}$ = 3 V | 1.5 | 2.0 | – | mA |
| Output Sink Current | 10 mV of Overdrive, $V_{out}$ = 0.2 V | 1.0 | 1.5 | – | mA |
| **INTERNAL OFFSET VOLTAGE** | | | | | |
| Offset Voltage to the (+) Pin of the Error Amp & the VDRP Pin | | −2 | 0 | +2 | mV |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VDROOP AMPLIFIER** | | | | | |
| Input Bias Current | | −200 | – | 200 | nA |
| Inverting Voltage Range | | 0 | 1.3 | 3.0 | V |
| Open Loop DC Gain | $C_L$ = 20 pF to GND including ESD<br>$R_L$ = 1 kΩ to GND | – | 100 | – | dB |
| Open Loop Unity Gain Bandwidth | $C_L$ = 20 pF to GND including ESD<br>$R_L$ = 1 kΩ to GND | – | 18 | – | MHz |
| Open Loop Phase Margin | $C_L$ = 20 pF to GND including ESD<br>$R_L$ = 1 kΩ to GND | – | 70 | – | ° |
| Slew Rate | $C_L$ = 20 pF to GND including ESD<br>$R_L$ = 1 kΩ to GND | – | 10 | – | V/μs |
| Maximum Output Voltage | 10 mV of Overdrive,<br>$I_{SOURCE}$ = 4.0 mA | 3.0 | – | – | V |
| Minimum Output Voltage | 10 mV of Overdrive,<br>$I_{SINK}$ = 1.0 mA | – | – | 1.0 | V |
| Output Source Current | 10 mV of Overdrive,<br>$V_{out}$ = 3.0 V | 4.0 | – | – | mA |
| Output Sink Current | 10 mV of Overdrive,<br>$V_{out}$ = 1.0 V | 1.0 | – | – | mA |
| **CSSUM AMPLIFIER** | | | | | |
| Current Sense Input to CSSUM Gain | −75 mV < CS < 75 mV | −3.793 | −3.70 | −3.608 | V/V |
| Current Sense Input to $V_{DRP}$ −3 dB Bandwidth | $C_L$ = 10 pF to GND,<br>$R_L$ = 10 kΩ to GND | – | 12 | – | MHz |
| Current Summing Amp Output Offset Voltage | CSx − CSNx = 0, CSx = 1 V | −8.0 | – | +8.0 | mV |
| Maximum CSSUM Output Voltage | CSx − CSxN = −0.2 V<br>(all phases) $I_{SOURCE}$ = 1 mA | 3.0 | – | – | V |
| Minimum CSSUM Output Voltage | CSx − CSxN = 0.7 V<br>(all phases) $I_{SINK}$ = 1 mA | – | – | 0.3 | V |
| Output Source Current | $V_{out}$ = 3.0 V | 1.0 | – | – | mA |
| Output Sink Current | $V_{out}$ = 0.3 V | 4.0 | – | – | mA |
| **PSI** | | | | | |
| Enable High Input Leakage Current | External 1k Pull−up to 3.3 V | – | – | 1.0 | μA |
| Threshold | | 450 | 600 | 770 | mV |
| Delay | | – | 100 | – | ns |
| **DRVON** | | | | | |
| Output High Voltage | Sourcing 500 μA | 3.0 | – | – | V |
| Output Low Voltage | Sinking 500 μA | – | – | 0.7 | V |
| Delay Time | Propagation delays | – | 10 | – | ns |
| Rise Time | $C_L$ (PCB) = 20 pF,<br>ΔVo = 10% to 90% | – | 10 | – | ns |
| Fall Time | $C_L$ (PCB) = 20 pF,<br>ΔVo = 10% to 90% | – | 10 | – | ns |
| Internal Pull−Down Resistance | | 35 | 70 | 140 | kΩ |
| $V_{CC}$ Voltage when DRVON Output Valid | | – | – | 2.0 | V |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CURRENT SENSE AMPLIFIERS** | | | | | |
| Input Bias Current | CSx = CSxN = 1.4 V | −50 | – | 50 | nA |
| Common Mode Input Voltage Range | | −0.3 | – | 2.0 | V |
| Differential Mode Input Voltage Range | | −120 | – | 120 | mV |
| Current Sharing Output Voltage | CSx = CSxN = 1.00 V, | −TBD | – | TBD | mV |
| Current Sense Input to PWM Gain | 0 V < CSx − CSxN < 0.1 V, | 5.4 | 5.7 | 6.0 | V/V |
| Current Sense Input to CSSUM Gain | 0 V < CSx − CSxN < 0.1 V | −3.793 | −3.7 | −3.608 | V/V |
| **IMON** | | | | | |
| $V_{DRP}$ to IMON Gain | 1.325 V > $V_{DRP}$ > 1.75 V | 1.89 | 2.0 | 2.02 | V/V |
| Current Sense Input to $V_{DRP}$ −3 dB Bandwidth | $C_L$ = 30 pF to GND,<br>$R_L$ = 100 kΩ to GND | – | 4.0 | – | MHz |
| $V_{DRP}$ to IMON Output Slew Rate | $C_L$ = 30 pF to GND,<br>Load = 100k to GND | – | TBD | – | V/μs |
| Output Referred Offset Voltage | $V_{DRP}$ = 1.5 V, $I_{SOURCE}$ = 0 mA | −TBD | – | TBD | mV |
| Minimum Output Voltage | $V_{DRP}$ = 1.3 V, $I_{SINK}$ = 25 μA | – | – | 0.1 | V |
| Maximum Output Voltage | $I_{out}$ = 300 μA | 1.0 | – | – | V |
| Output Sink Current | $V_{out}$ = 0.3 V | 175 | – | – | μA |
| Maximum Clamp Voltage | IMON − VSN $V_{DRP}$ = HIGH<br>$R_{LOAD}$ = Open | 1.1 | – | 1.15 | V |
| **OSCILLATOR** | | | | | |
| Switching Frequency Range | | 100 | – | 1100 | kHz |
| Switching Frequency Accuracy | 200 kHz < $F_{SW}$ < 600 kHz | – | – | 5.0 | % |
| Switching Frequency Accuracy | 100 kHz < $F_{SW}$ < 1 MHz | – | – | 10 | % |
| Switching Frequency Accuracy (2ph or 4ph) | $R_{OSC}$ = 69.8k | TBD | – | TBD | kHz |
| | $R_{OSC}$ = 16.2k | 475 | – | 525 | |
| | $R_{OSC}$ = 7.5k | TBD | – | TBD | |
| Switching Frequency Accuracy (3ph) | $R_{OSC}$ = 69.8k | TBD | – | TBD | kHz |
| | $R_{OSC}$ = 16.2k | 494 | – | 546 | |
| | $R_{OSC}$ = 7.5k | TBD | – | TBD | |
| ROSC Output Voltage | | 1.93 | 2.00 | 2.05 | V |
| **MODULATORS (PWM Comparators)** | | | | | |
| Minimum Pulse Width | Fsw = 800 kHz | – | 30 | – | ns |
| Magnitude of the PWM Ramp | | TBD | 1.0 | TBD | V |
| 0% Duty Cycle | COMP Voltage when the PWM Outputs Remain LO | TBD | 150 | TBD | mV |
| 100% Duty Cycle | COMP Voltage when the PWM Outputs Remain HI | – | 1.15 | – | V |
| PWM Phase Angle Error | Between Adjacent Phases | −TBD | – | TBD | ° |
| **VR_RDY (Power Good) OUTPUT** | | | | | |
| VR_RDY Output Saturation Voltage | $I_{PGD}$ = 10 mA | – | – | 0.4 | V |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VR_RDY (Power Good) OUTPUT** | | | | | |
| VR_RDY Rise Time | External pull−up of 1 KΩ to 1.25 V, $C_{TOT}$ = 45 pF, ΔVo = 10% to 90% | − | 100 | 150 | ns |
| VR_RDY Output Voltage at Power−up | VR_RDY pulled up to 5 V via 2 kΩ, $t_{R(VCC)} \le 3 \times t_{R(5V)}$ 100 μs ≤ $t_{R(VCC)}$ ≤ 20 ms | − | − | 1.0 | V |
| VR_RDY High − Output Leakage Current | VR_RDY = 5.5 V via 1 K | − | − | 0.1 | μA |
| VR_RDY Upper Threshold Voltage (INTEL) | VCore Increasing, DAC = 1.3 V | − | 300 | 250 | mV (below DAC) |
| VR_RDY Lower Threshold Voltage (INTEL) | VCore Decreasing, DAC = 1.3 V | 390 | 350 | 300 | mV (below DAC) |
| VR_RDY Lower Threshold Voltage (AMD) | VCore Increasing, DAC = 1.3 V | − | TBD | TBD | mV (below DAC) |
| VR_RDY Lower Threshold Voltage (AMD) | VCore Decreasing, DAC = 1.3 V | TBD | TBD | TBD | mV (below DAC) |
| VR_RDY Rising Delay | VCore Increasing | − | TBD | − | μs |
| VR_RDY Falling Delay | VCore Decreasing | − | 5.0 | − | μs |
| **PWM G4 OUTPUT** | | | | | |
| Output High Voltage | Sourcing 500 μA | 3.0 | − | − | V |
| Mid Output Voltage | | 1.4 | 1.5 | 1.6 | |
| Output Low Voltage | Sinking 500 μA | − | − | 0.7 | V |
| Delay + Rise Time | $C_L$ (PCB) = 50 pF, ΔVo = $V_{CC}$ to GND | − | 10 | 15 | ns |
| Delay + Fall Time | $C_L$ (PCB) = 50 pF, ΔVo = GND to $V_{CC}$ | − | 10 | 15 | ns |
| Tri−State Output Leakage | Gx = 2.5 V, x = 1−4 | − | − | 1.5 | μA |
| Output Impedance − HI or LO State | Max Resistance to $V_{CC}$ (HI) or GND (LO) | − | 75 | 150 | Ω |
| Minimum $V_{CC}$ for Valid PWM Output Level | | − | − | 2.0 | V |
| PWM 4 2/3/4 Phase Detection | | | | | |
| 2 Phase Mode | Note Gate 4 tied to $V_{CC}$ | 3.2 | − | $V_{CC}$ | V |
| 4 Phase Mode | Note Gate Driver will pull to 1.5 V | 1.2 | − | 2.8 | V |
| 3 Phase Mode | Note Gate 4 tied to GND | 0 | − | 0.8 | V |
| **DIGITAL SOFT−START** | | | | | |
| Soft−Start Ramp Time | DAC = 0 to DAC = 1.1 V | 1.0 | − | 1.3 | ms |
| VR11 $V_{boot}$ time | Not used in Legacy Startup | 400 | 500 | 600 | μs |
| **VID7/VR11/AMD/LEGACY INPUT** | | | | | |
| VID Threshold | | 450 | 600 | 770 | mV |
| VR11 Input Bias Current | | −100 | − | 100 | nA |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VID7/VR11/AMD/LEGACY INPUT** | | | | | |
| Delay Before Latching VID Change (VID Deskewing) | Measured from the Edge of the 1st VID Change | 200 | – | 300 | ns |
| AMD Upper Threshold | Note: When above this threshold the controller will ramp directly to VID without stopping at $V_{boot}$ | – | – | 2.9 | V |
| AMD Lower Threshold | | 2.4 | – | – | V |
| **ENABLE INPUT** | | | | | |
| Enable High Input Leakage Current | Pull−up to 1.3 V | – | – | 200 | nA |
| VR11.1 Threshold | | 450 | 600 | 770 | mV |
| AMD Upper Threshold | | – | 1.3 | 1.5 | V |
| AMD Lower Threshold | | 0.9 | 1.1 | – | V |
| AMD Total Hysteresis | Rising− Falling Threshold | – | 200 | – | mV |
| Enable Delay Time | Measure time from Enable transitioning HI to when SS begins | – | 3.5 | – | ms |
| **CURRENT LIMIT** | | | | | |
| ILIM to VDRP Gain | | 0.99 | 1.00 | 1.01 | V/V |
| ILIM to VRDP Gain in PSI 4 Phase | | – | 0.25 | – | V/V |
| ILIM to VDRP Gain in PSI 3 Phase | | – | 0.333 | – | V/V |
| ILIM to VDRP Gain in PSI 2 Phase | | – | 0.5 | – | V/V |
| ILIM Pin Input Bias Current | | – | 0.1 | 1.0 | μA |
| ILIM Pin Working Voltage Range | | 0.1 | – | 2.0 | V |
| ILIM accuracy | Measured with respect to the ILIM setting | −10 | – | 10 | mV |
| Delay | | – | – | 120 | ns |
| **OVERVOLTAGE PROTECTION** | | | | | |
| VR11 Over Voltage Threshold | | DAC+ 160 | DAC+ 190 | DAC+ 210 | mV |
| AMD Over Voltage Threshold | | DAC+ 210 | DAC+ 235 | DAC+ 260 | mV |
| Delay | | – | – | 100 | ns |
| **UNDERVOLTAGE PROTECTION** | | | | | |
| $V_{CC}$ UVLO Start Threshold | | 4.0 | 4.25 | 4.5 | V |
| $V_{CC}$ UVLO Stop Threshold | | 3.8 | 4.05 | 4.3 | V |
| $V_{CC}$ UVLO Hysteresis | | – | 200 | – | mV |
| **DAC OUTPUT** | | | | | |
| DAC Output Variation | $I_{SOURCE}$ = 200 μA, All VIDs | −3.0 | 0 | 3.0 | % |
| DAC Output Variation | $I_{SINK}$ = 200 μA, All VIDs | −3.0 | 0 | 3.0 | % |
| Output Source Current | $V_{out}$ = 1.6 V | 0 | – | 5.0 | mA |
| Output Sink Current | $V_{out}$ = 0.3 V | 5.0 | – | 16 | mA |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VID INPUTS** | | | | | |
| Threshold | | 450 | 600 | 770 | mV |
| VR11 Mode Leakage | | −100 | – | 100 | nA |
| AMD Mode Input Bias Current | | 10 | – | 25 | μA |
| Delay before Latching VID Change (VID Deskewing) | Measured from the edge of the 1st VID change | 200 | – | 300 | ns |
| Delay Before Responding to Invalid or Shutdown Codes (Remove Spec) | Note: DAC must hold the last valid VID during this period | – | – | – | μs |
| **DIGITAL DAC SLEW RATE LIMITER** | | | | | |
| Slew Rate Limit (Intel Mode) | | 12.5 | – | 15 | mV/μs |
| Slew Rate Limit (AMD Mode) | | 3.125 | – | 3.75 | mV/μs |
| Soft−Start Slew Rate | | – | 0.84 | – | mV/μs |
| **INPUT SUPPLY CURRENT** | | | | | |
| $V_{CC}$ Operating Current | EN Low, No PWM | 20 | – | 40 | mA |
| **PHASE SHEDDING** | | | | | |
| CS referred ph shed bias | CS2 through CS4 | – | 66 | – | mV |
| **$V_{CCP}$ SUPPLY VOLTAGE** | | | | | |
| $V_{CCP}$ UVLO Start Threshold | | 8.2 | 9.0 | 9.5 | V |
| $V_{CCP}$ UVLO Stop Threshold | | 7.2 | 8.0 | 8.5 | V |
| $V_{CCP}$ UVLO Hysteresis | | – | 1.0 | – | V |
| $V_{CCP}$ POR | Voltage at which the Driver OVP becomes active | TBD | 3.2 | TBD | |
| **BOOST PIN UVLO** | | | | | |
| BOOST $V_{CC}$ UVLO Start Threshold | | 3.5 | | 4.0 | V |
| BOOST $V_{CC}$ UVLO Stop Threshold | | 3.3 | | 3.8 | V |
| BOOST $V_{CC}$ UVLO Hysteresis | | | 200 | | mV |
| **BOOST SUPPLY CURRENT** | | | | | |
| $I_{VCCP_NORM}$ Quiescent Supply Current in Normal Operation | EN = $V_{CC}$, PWM = OSC, $F_{SW}$ = 100k, $C_{LOAD}$ = 0 p, $V_{CCP}$ = 12 V | – | – | 42 | mA |
| $I_{VCC_SBC}$ Standby Current | EN = GND; No switching, $V_{CCP}$ = 12 V | 20 | – | 40 | mA |
| $I_{BST1}$ Quiescent Supply Current in Normal Operation | IN = $V_{CCP}$, $V_{CCP}$ = 12 V | – | 10 | TBD | mA |
| $I_{BST2}$ Quiescent Supply Current in Normal Operation | IN = GND, $V_{CCP}$ = 12 V | – | 10 | TBD | mA |
| $I_{BST3}$ Quiescent Supply Current in Normal Operation | IN = GND, $V_{CCP}$ = 12 V | – | 10 | TBD | |
| $I_{BST1_SD}$ Standby Current | IN = $V_{CCP}$, $V_{CCP}$ = 12 V | – | 0.25 | – | mA |
| $I_{BST2_SD}$ Standby Current | IN = GND, $V_{CCP}$ = 12 V | – | 0.25 | – | mA |
| $I_{BST3_SD}$ Standby Current | IN = GND, $V_{CCP}$ = 12 V | – | 0.25 | – | mA |
| **STARTUP HIGH SIDE SHORT TRIP (Active only during 1st power on)** | | | | | |
| $V_{swx}$ Output Overvoltage Trip Threshold at Startup | Power Startup time, $V_{CC}$ > 9 V | 1.75 | – | 2.0 | V |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

## ELECTRICAL CHARACTERISTICS

$0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75 < V_{CC} < 5.25$ V; All DAC Codes; $C_{VCC}$ = 0.1 μF unless otherwise noted.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HIGH SIDE DRIVER** | | | | | |
| $R_{H_TG}$ Output Resistance, Sourcing | $V_{BST} - V_{SW}$ = 12 V | – | 1.8 | 4.2 | Ω |
| $R_{H_TG}$ Output Resistance, Sinking | $V_{BST} - V_{SW}$ = 12 V | – | 1.0 | 2.2 | |
| $Tr_{DRVH}$ Transition Time | $C_{LOAD}$ = 3 nF, $V_{BST} - V_{SW}$ = 12 V | – | 16 | – | ns |
| $Tf_{DRVH}$ Transition Time | $C_{LOAD}$ = 3 nF, $V_{BST} - V_{SW}$ = 12 V | – | 11 | – | ns |
| $Tpdh_{DRVH}$ Propagation Delay (Note 4) | Driving High, $C_{LOAD}$ = 3 nF, $V_{CCP}$ = 12 V | – | 20 | – | ns |
| $Tpdh_{DRVH}$ Propagation Delay (Note 4) | Driving Low, $C_{LOAD}$ = 3 nF, $V_{CCP}$ = 12 V | – | 20 | – | ns |
| **LOW SIDE DRIVER** | | | | | |
| $R_{H_BG}$ Output Resistance, Sourcing | SW = GND | – | TBD | 4.2 | Ω |
| $R_{L_BG}$ Output Resistance, Sinking | SW = $V_{CC}$ | – | TBD | 2.2 | Ω |
| $Tr_{DRVH}$ Transition Time | $C_{LOAD}$ = 3 nF | – | 16 | – | ns |
| $Tf_{DRVH}$ Transition Time | $C_{LOAD}$ = 3 nF | – | 11 | – | ns |
| $Tpdh_{DRVH}$ Propagation Delay (Note 4) | Driving High, $C_{LOAD}$ = 3 nF, $V_{CCP}$ = 12 V | – | 20 | – | ns |
| $Tpdh_{DRVH}$ Propagation Delay (Note 4) | Driving Low, $C_{LOAD}$ = 3 nF, $V_{CCP}$ = 12 V | – | 20 | – | ns |
| $V_{NCDT}$ Negative Current Detector Threshold | (Note 3) | – | −1.0 | – | mV |
| **THERMAL SHUTDOWN** | | | | | |
| Tsd Thermal Shutdown (Note 3) | | 150 | 170 | – | °C |
| Tsdhys Thermal Shutdown Hysteresis (Note 3) | | – | 20 | – | °C |
| **VRM 11 DAC** | | | | | |
| System Voltage Accuracy | 1.0 V < DAC < 1.6 V<br>0.8 V < DAC < 1.0 V<br>0.5 V < DAC < 0.8 V | –<br>–<br>– | –<br>–<br>– | ±0.5<br>±5.0<br>±8.0 | %<br>mV<br>mV |

3. Design guaranteed.
4. For propagation delays, “tpdh” refers to the specified signal going high “tpdl” refers to it going low. Reference Gate Timing Diagram.
5. Guaranteed by design; not tested in production.
6. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10
7. No DAC offset is implemented for AMD operation.

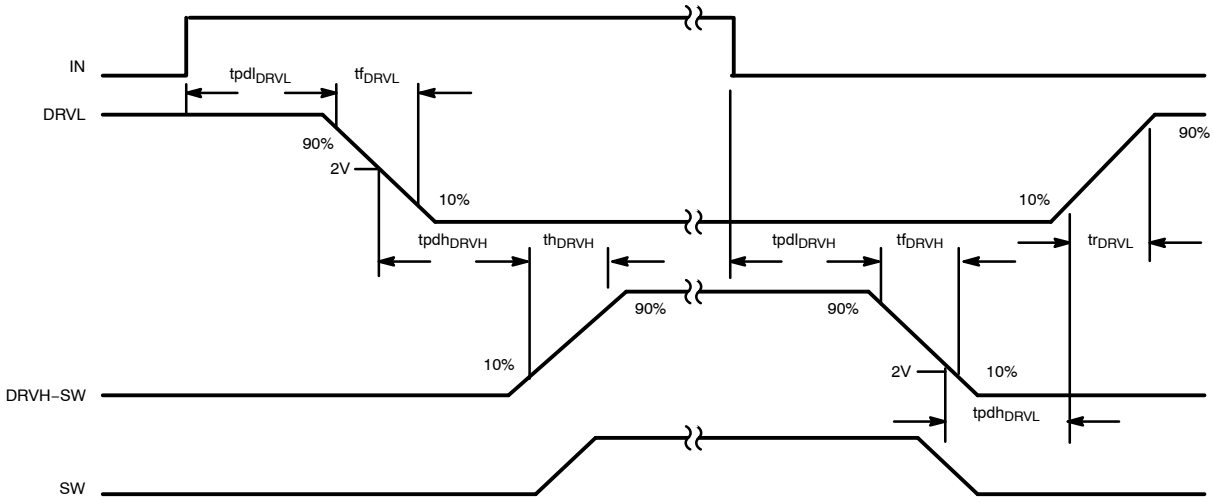



**Figure 5. Timing Diagram**

**Table 2. VRM11 $V_{ID}$ CODES**

| $V_{ID7}$ 800 mV | $V_{ID6}$ 400 mV | $V_{ID5}$ 200 mV | $V_{ID4}$ 100 mV | $V_{ID3}$ 50 mV | $V_{ID2}$ 25 mV | $V_{ID1}$ 12.5 mV | $V_{ID0}$ 6.25 mV | Voltage (V) | HEX |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 00 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 01 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.60000 | 02 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.59375 | 03 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.58750 | 04 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.58125 | 05 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.57500 | 06 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.56875 | 07 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.56250 | 08 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.55625 | 09 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.55000 | 0A |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.54375 | 0B |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.53750 | 0C |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.53125 | 0D |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.52500 | 0E |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.51875 | 0F |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.51250 | 10 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.50625 | 11 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.50000 | 12 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.49375 | 13 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.48750 | 14 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.48125 | 15 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.47500 | 16 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.46875 | 17 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.46250 | 18 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.45625 | 19 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.45000 | 1A |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.44375 | 1B |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.43750 | 1C |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.43125 | 1D |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.42500 | 1E |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.41875 | 1F |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.41250 | 20 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.40625 | 21 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.40000 | 22 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.39375 | 23 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.38750 | 24 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.38125 | 25 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.37500 | 26 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.36875 | 27 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.36250 | 28 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1.35625 | 29 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.35000 | 2A |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.34375 | 2B |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.33750 | 2C |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.33125 | 2D |

**Table 2. VRM11 $V_{ID}$ CODES**

| $V_{ID7}$ 800 mV | $V_{ID6}$ 400 mV | $V_{ID5}$ 200 mV | $V_{ID4}$ 100 mV | $V_{ID3}$ 50 mV | $V_{ID2}$ 25 mV | $V_{ID1}$ 12.5 mV | $V_{ID0}$ 6.25 mV | Voltage (V) | HEX |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.32500 | 2E |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.31875 | 2F |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.31250 | 30 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.30625 | 31 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.30000 | 32 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.29375 | 33 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.28750 | 34 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.28125 | 35 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.27500 | 36 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.26875 | 37 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.26250 | 38 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.25625 | 39 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.25000 | 3A |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.24375 | 3B |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.23750 | 3C |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.23125 | 3D |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.22500 | 3E |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.21875 | 3F |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.21250 | 40 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.20625 | 41 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.20000 | 42 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.19375 | 43 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.18750 | 44 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.18125 | 45 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.17500 | 46 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.16875 | 47 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.16250 | 48 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.15625 | 49 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.15000 | 4A |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.14375 | 4B |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.13750 | 4C |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.13125 | 4D |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.12500 | 4E |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.11875 | 4F |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.11250 | 50 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.10625 | 51 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.10000 | 52 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.09375 | 53 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.08750 | 54 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.08125 | 55 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.07500 | 56 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.06875 | 57 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.06250 | 58 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.05625 | 59 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.05000 | 5A |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.04375 | 5B |

**Table 2. VRM11 $V_{ID}$ CODES**

| $V_{ID7}$ 800 mV | $V_{ID6}$ 400 mV | $V_{ID5}$ 200 mV | $V_{ID4}$ 100 mV | $V_{ID3}$ 50 mV | $V_{ID2}$ 25 mV | $V_{ID1}$ 12.5 mV | $V_{ID0}$ 6.25 mV | Voltage (V) | HEX |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.03750 | 5C |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.03125 | 5D |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.02500 | 5E |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.01875 | 5F |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.01250 | 60 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.00625 | 61 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.00000 | 62 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.99375 | 63 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.98750 | 64 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.98125 | 65 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.97500 | 66 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.96875 | 67 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.96250 | 68 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.95625 | 69 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.95000 | 6A |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.94375 | 6B |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.93750 | 6C |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.93125 | 6D |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.92500 | 6E |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.91875 | 6F |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.91250 | 70 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.90625 | 71 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.90000 | 72 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.89375 | 73 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.88750 | 74 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.88125 | 75 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.87500 | 76 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.86875 | 77 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.86250 | 78 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.85625 | 79 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.85000 | 7A |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.84375 | 7B |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.83750 | 7C |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.83125 | 7D |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.82500 | 7E |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.81875 | 7F |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.81250 | 80 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.80625 | 81 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.80000 | 82 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.79375 | 83 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.78750 | 84 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.78125 | 85 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.77500 | 86 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0.76875 | 87 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0.76250 | 88 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.75625 | 89 |

**Table 2. VRM11 $V_{ID}$ CODES**

| $V_{ID7}$ 800 mV | $V_{ID6}$ 400 mV | $V_{ID5}$ 200 mV | $V_{ID4}$ 100 mV | $V_{ID3}$ 50 mV | $V_{ID2}$ 25 mV | $V_{ID1}$ 12.5 mV | $V_{ID0}$ 6.25 mV | Voltage (V) | HEX |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.75000 | 8A |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0.74375 | 8B |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0.73750 | 8C |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0.73125 | 8D |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.72500 | 8E |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0.71875 | 8F |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.71250 | 90 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.70625 | 91 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.70000 | 92 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.69375 | 93 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.68750 | 94 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.68125 | 95 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.67500 | 96 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.66875 | 97 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.66250 | 98 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.65625 | 99 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.65000 | 9A |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.64375 | 9B |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.63750 | 9C |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.63125 | 9D |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.62500 | 9E |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.61875 | 9F |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.61250 | A0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.60625 | A1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.60000 | A2 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.59375 | A3 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.58750 | A4 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.58125 | A5 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.57500 | A6 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.56875 | A7 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.56250 | A8 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.55625 | A9 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.55000 | AA |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.54375 | AB |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.53750 | AC |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.53125 | AD |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.52500 | AE |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.51875 | AF |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.51250 | B0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.50625 | B1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.50000 | B2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF | FE |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF | FF |

| Parameter | Test Condition | TYP | MAX | Units |
|---|---|---|---|---|
| **VR10 DAC** | | | | |
| System Voltage Accuracy | 1.0 V < DAC < 1.6 V | – | ±0.5 | % |
| | 0. 83125 V < DAC < 1.0 V | – | ±5 | mV |

8. Internal DAC voltage is centered 19 mV below the listed Voltage. For VR11.1/VR11.0/VR10 No DAC offset is implemented for AMD operation.

| $V_{ID4}$ 400 mV | $V_{ID3}$ 200 mV | $V_{ID2}$ 100 mV | $V_{ID1}$ 50 mV | $V_{ID0}$ 25 mV | $V_{ID5}$ 12.5 mV | $V_{ID6}$ 6.25 mV | Voltage (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.60000 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.59375 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.58750 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.58125 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.57500 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.56875 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.56250 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.55625 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.55000 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.54375 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.53750 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.53125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.52500 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.51875 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.51250 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.50625 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.50000 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.49375 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.48750 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.48125 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.47500 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.46875 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.46250 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.45625 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.45000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.44375 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.43750 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.43125 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.42500 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.41875 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.41250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.40625 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.40000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.39375 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.38750 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.38125 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.37500 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.36875 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.36250 |

**Table 3. DAC CODES FOR VRM 10**

| $V_{ID4}$ 400 mV | $V_{ID3}$ 200 mV | $V_{ID2}$ 100 mV | $V_{ID1}$ 50 mV | $V_{ID0}$ 25 mV | $V_{ID5}$ 12.5 mV | $V_{ID6}$ 6.25 mV | Voltage (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.35625 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.35000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.34375 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.33750 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.33125 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.32500 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.31875 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.31250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.30625 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.30000 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.29375 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.28750 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.28125 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.27500 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.26875 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.26250 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.25625 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1.25000 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.24375 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1.23750 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1.23125 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1.22500 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1.21875 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1.21250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1.20625 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1.20000 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1.19375 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1.18750 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1.18125 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1.17500 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1.16875 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1.16250 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1.15625 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1.15000 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1.14375 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1.13750 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1.13125 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1.12500 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1.11875 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1.11250 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1.10625 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1.10000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1.09375 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF |

**Table 3. DAC CODES FOR VRM 10**

| $V_{ID4}$ 400 mV | $V_{ID3}$ 200 mV | $V_{ID2}$ 100 mV | $V_{ID1}$ 50 mV | $V_{ID0}$ 25 mV | $V_{ID5}$ 12.5 mV | $V_{ID6}$ 6.25 mV | Voltage (V) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.08750 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.08125 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.07500 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.06875 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.06250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.05625 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.05000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.04375 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.03750 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.03125 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.02500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.01875 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.01250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.00625 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.00000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.99375 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.98750 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.98125 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.97500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.96875 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.96250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.95625 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.95000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.94375 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.93750 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.93125 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.92500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.91875 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.91250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.90625 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.90000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.89375 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.88750 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.88125 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.87500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.86875 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.86250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.85625 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.85000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.84375 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.83750 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.83125 |

| Parameter | Test Condition | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| **AMD DAC** | | | | | |
| System Voltage Accuracy | 1.0 V < DAC < 1.55V | – | – | ±0.5 | % |
| | 0.6 V ≤ DAC < 1.0V | – | – | ±1.0 | % |
| | 0.375 V < DAC < 0.6V | – | – | ±2.0 | % |

9. NOTE: No DAC offset is implemented for AMD operation. DAC should be equal to the Nominal $V_{out}$ shown in the table.

**Table 4. AMD PROCESSOR 6−BIT $V_{ID}$ CODE**

| ($V_{ID}$) Codes | | | | | | Nominal | |
|---|---|---|---|---|---|---|---|
| $V_{ID5}$ | $V_{ID4}$ | $V_{ID3}$ | $V_{ID2}$ | $V_{ID1}$ | $V_{ID0}$ | $V_{out}$ | Units |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.550 | V |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.525 | V |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.500 | V |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.475 | V |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.450 | V |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.425 | V |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.400 | V |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.375 | V |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.350 | V |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.325 | V |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.300 | V |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.275 | V |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.250 | V |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.225 | V |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.200 | V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.175 | V |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.150 | V |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.125 | V |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.100 | V |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.075 | V |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.050 | V |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.025 | V |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.000 | V |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.975 | V |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.950 | V |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.925 | V |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.900 | V |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.875 | V |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.850 | V |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.825 | V |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.800 | V |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.775 | V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 | V |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.7500 | V |

**Table 4. AMD PROCESSOR 6−BIT $V_{ID}$ CODE**

| ($V_{ID}$) Codes | | | | | | Nominal $V_{out}$ | Units |
|---|---|---|---|---|---|---|---|
| $V_{ID5}$ | $V_{ID4}$ | $V_{ID3}$ | $V_{ID2}$ | $V_{ID1}$ | $V_{ID0}$ | | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 | V |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.7250 | V |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 | V |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7000 | V |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.6875 | V |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.6750 | V |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.6625 | V |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.6500 | V |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.6375 | V |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.6250 | V |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.6125 | V |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.6000 | V |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.5875 | V |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.5750 | V |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5625 | V |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.5500 | V |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.5375 | V |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.5250 | V |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.5125 | V |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.5000 | V |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.4875 | V |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.4750 | V |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.4625 | V |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.4500 | V |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.4375 | V |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.4250 | V |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.4125 | V |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4000 | V |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.3875 | V |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.3750 | V |

## FUNCTIONAL DESCRIPTIONS

### General

The NCP5395 dual edge modulated multiphase PWM controller is specifically designed with the necessary features for a high current CPU system. The IC consists of the following blocks: Precision Flexible DAC, Differential Remote Voltage Sense Amplifier, High Performance Voltage Error Amplifier, Differential Current Feedback Amplifiers, Precision Oscillator and Saw−tooth Generator, and PWM Comparators with Hysteresis. The controller also supports power saving mode as per Intel VR11.1 by accurately monitoring the current and switching between multi−phase and single phase operations as requested by the microprocessor system. Protection features include: Undervoltage Lockout, Soft−Start, Overcurrent Protection, Overvoltage Protection, and Power Good Monitor.

### Precision Programmable DAC

A precision flexible DAC is provided. The DAC will conform to 2 different specifications: AMD or VR11.1. The VID7/AMD pin is provided to determine which DAC specification will be used and which soft−start mode the part will use for power up. There are two soft−start modes. If VID7/AMD is above it's threshold the device will soft−start and ramp directly to the DAC code present on the VID inputs. The following truth table describes the functionality:

| VID7/AMD Pin | VID7 | Enable Pin Mode | Soft Start Mode |
|---|---|---|---|
| Above AMD Threshold | Not active | AMD Threshol ds | Ramp to VID |
| Below AMD Threshold | Active | VR11.1 Threshol ds | Ramp to Vboot |

### VID INPUTS

VID0−VID7 control the target regulation voltage during normal operation. In AMD mode the VID capture is enabled just before soft start. In VR11 mode the VID capture is enabled at the end of the $V_{BOOT}$ waiting period. If the VID is valid the DAC will track to it. If an invalid VID occurs it will be ignored for 10 μs before the controller shuts down.

### Remote Sense Amplifier

A high performance differential amplifier is provided to accurately sense the output voltage of the regulator. The non−inverting input should be connected to the regulator's output voltage. The inverting input should be connected to the return line of the regulator. Both connection points are intended to be at a remote point so that the most accurate reading of the output voltage can be obtained. The amplifier is configured in a very unique way. First, the gain of the amplifier is internally set to unity. Second, both the inverting and non−inverting inputs of the amplifier are summing nodes. The inverting input sums the output voltage return voltage with the DAC voltage. The non−inverting input sums the remote output voltage with a 1.3 V reference. The resulting voltage at the output of the remote sense amplifier is:

$$V_{Diffout} = V_{out} + 1.3\ V - V_{dac} - V_{outreturn}$$

This signal then goes through a standard compensation circuit and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is also connected to the 1.3 V reference. The 1.3 V reference then is subtracted out and the error signal at the comp pin of the error amplifier is as normally expected:

$$V_{comp} = V_{dac} - V_{out}$$

The non−inverting input of the remote sense amplifier is pulled low through a small current sink during a fault condition to prevent accidental charging of the regulator output.

### 2/3/4 Phase Operation

The part can be configured to 2−, 3−, or 4−phase mode. In 2− or 3−phase mode, the internal drivers will be used. In 4−phase mode, an external driver must be used to drive phase 4. The NCP5359 driver is suggested to be used with the controller. The input to G4 pin will decide which phase mode the system is in operation. Please refer to the Application Schematics for more information.

### High Performance Voltage Error Amplifier

A high performance voltage error amplifier is provided. The error amplifier's inverting input is VFB and its output is COMP. A standard type 3 compensation circuit is used compensate the system. This involves a 3 pole, 2 zero compensation network. The comp pin is pulled to ground before soft−start for smooth start up.

### Differential Current Sense

Four differential amplifiers are provided to sense the output current of each phase. These current sense amplifiers sense the current through the corresponding phase. A voltage is generated across a current sense element such as an inductor or sense resistor. The sense element should be between 0.5 mΩ and 1.5 mΩ. It is possible to sense both negative and positive going current. The information is used to create the signal CSSUM and provide feedback for current sharing.

### Precision Oscillator

A programmable precision oscillator is provided. This oscillator is programmed by the summed resistance of an oscillator resistor and a current limit resistor. The output voltage of this pin is used as the reference for the current limit. The oscillator frequency range is 125 KHz/phase to 1000 KHz/phase. The oscillator frequency is proportional to the current drawn out of the OSC pin.

### PWM Comparators

Four PWM comparators are incorporated within the IC. The non−inverting input of the comparators is connected to the output of the error amplifier. The inverting input is connected to a summed output of the phase current and the oscillator ramp voltage with an offset. The output of the comparator generates the PWM control signals.

During steady state operation, the duty cycle will center on the valley of the saw−tooth waveform. During a transient event, the controller will operate somewhat hysteretic, with the duty cycle climbing along either the down ramp, up ramp, or both.

### Soft−Start

Soft−start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. There are 2 possible soft start modes: VR11 and AMD. AMD mode simply ramps $V_{core}$ from 0 V directly to the DAC setting. The VR11 mode ramps DAC to 1.1 V, pauses for 500 μs, reads the DAC setting, then ramps to the final DAC setting.

### Digital Slew Rate Limiter / Soft Start Block

The slew rate limiter and the soft−start block are to be implemented with a digital up/down counter controlled by an oscillator that is synchronized to VID line changes. During soft start the DAC will ramp at the soft−start rate, after soft start is complete the ramp rate will follow either the Intel or the AMD slew rate depending on the mode.

### Under Voltage Lockouts

An under voltage circuit senses the $V_{CC}$ input of the controller and the $V_{CCP}$ input of the driver. During power up the input voltage to the controller is monitored. The PWM outputs and the soft start circuit are disabled until the input voltage exceeds the threshold voltage of the comparators. Hysteresis is incorporated within the comparators.

The DRVON is held low until $V_{CCP}$ reaches the start threshold during startup. If $V_{CCP}$ decreases below the stop threshold, the output gate will be forced low unit input voltage $V_{CCP}$ rises above the startup threshold.

### Over Current Latch

A programmable over current latch is incorporated within the IC. The oscillator pin provides the reference voltage for this pin. A resistor divider from the OSC pin generates the ILIM voltage. The latch is set when the current information on $V_{droop}$ exceeds the programmed voltage plus a 1.3 V offset. DRVON is immediately set low. To recover the part must be reset by the EN pin or by cycling $V_{CC}$.

### UVLO Monitor

If the output voltage falls greater than 300 mV below the DAC voltage for more than 5 μs the UVLO comparator will trip sending the VR_RDY signal low.

### Over Voltage Protection

The output voltage is monitored at the input of the differential amplifier. During normal operation, if the output voltage exceeds the DAC voltage by 185 mV, or 285 mV if in AMD mode, the VR_RDY flag will transition low the high side gate drivers set to low, and the low side gate drivers are all brought to high until the voltage falls below the OVP threshold. If the over voltage trip 8 times the output voltage will shut down. The OVP will not shut down the controller if it occurs during soft−start. This is to allow the controller to pull the output down to the DAC voltage and start up into a pre−charged output.

### $V_{CCP}$ Power ON Reset OVP

The $V_{CCP}$ power on reset OVP feature is used to protect the CPU during start up. When $V_{CCP}$ is higher than 3.2 V, the gate driver will monitor the switching node SW pin. If SWNx pin higher than 1.9 V, the bottom gate will be forced to high for discharge of the output capacitor. This works best if the 5 volt standby is diode OR'ed into $V_{CCP}$ with the 12 V rail. The fault mode will be latched and the DRVON pin will be forced to low, unless $V_{CCP}$ is reduced below the UVLO threshold.

### Power Saving Mode

The controller is designed to allow power saving mode to maintain a maximum efficiency. When a low PSI signal from microcontroller is received, the controller will keep one phase operating while shedding other phases. The active one phase will operate in diode emulation mode, minimizing power losses in light load. When the low PSI signal is de−asserted, the dropped phases will be pulled back in to be ready for heavy load.

### Adaptive Non−overlap

The non−overlap dead time control is used to avoid shoot through damage to the power MOSFETs. When the PWM signal pull high, DRVL will go low after a propagation delay, the controller monitors the switching node (SWN) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high−side MOSFET. When the PWM pull low, gate DRVH will go low after the propagation delay (tpdDRVH). The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

### Layout Guidelines

Layout is very important thing for design a DC−DC converter. Bootstrap capacitor and $V_{in}$ capacitor are most critical items, it should be placed as close as to the controller IC. Another item is using a GND plane. Ground plane can provide a good return path for gate drives for reducing the ground noise. Therefore GND pin should be directly connected to the ground plane and close to the low−side MOSFET source pin. Also, the gate drive trace should be considered. The gate drives has a high di/dt when switching, therefore a minimized gate drives trace can reduce the di/dv, raise and fall time for reduce the switching loss.

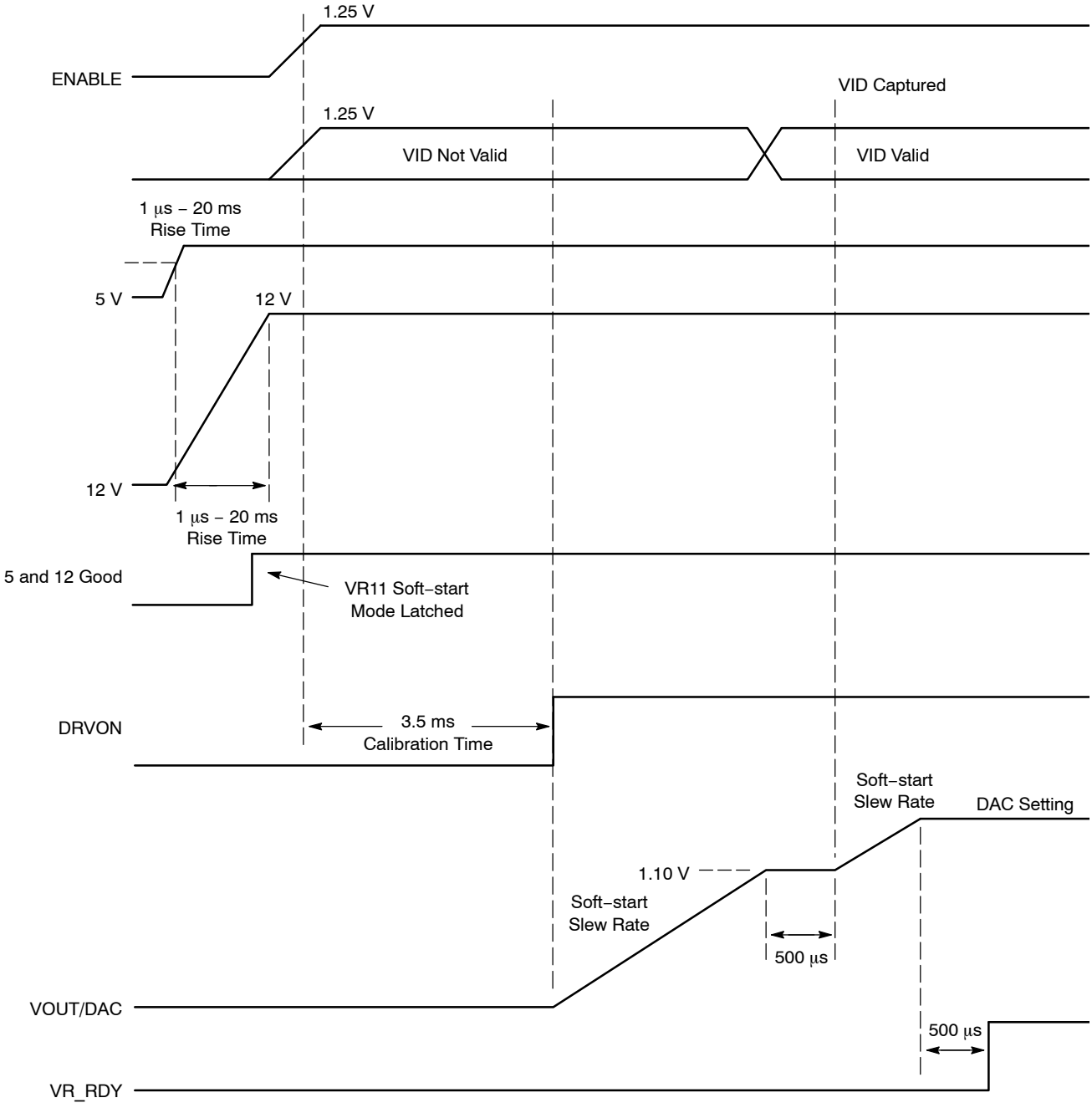



**Figure 6. VR11.1 Start Up Timing Diagram**

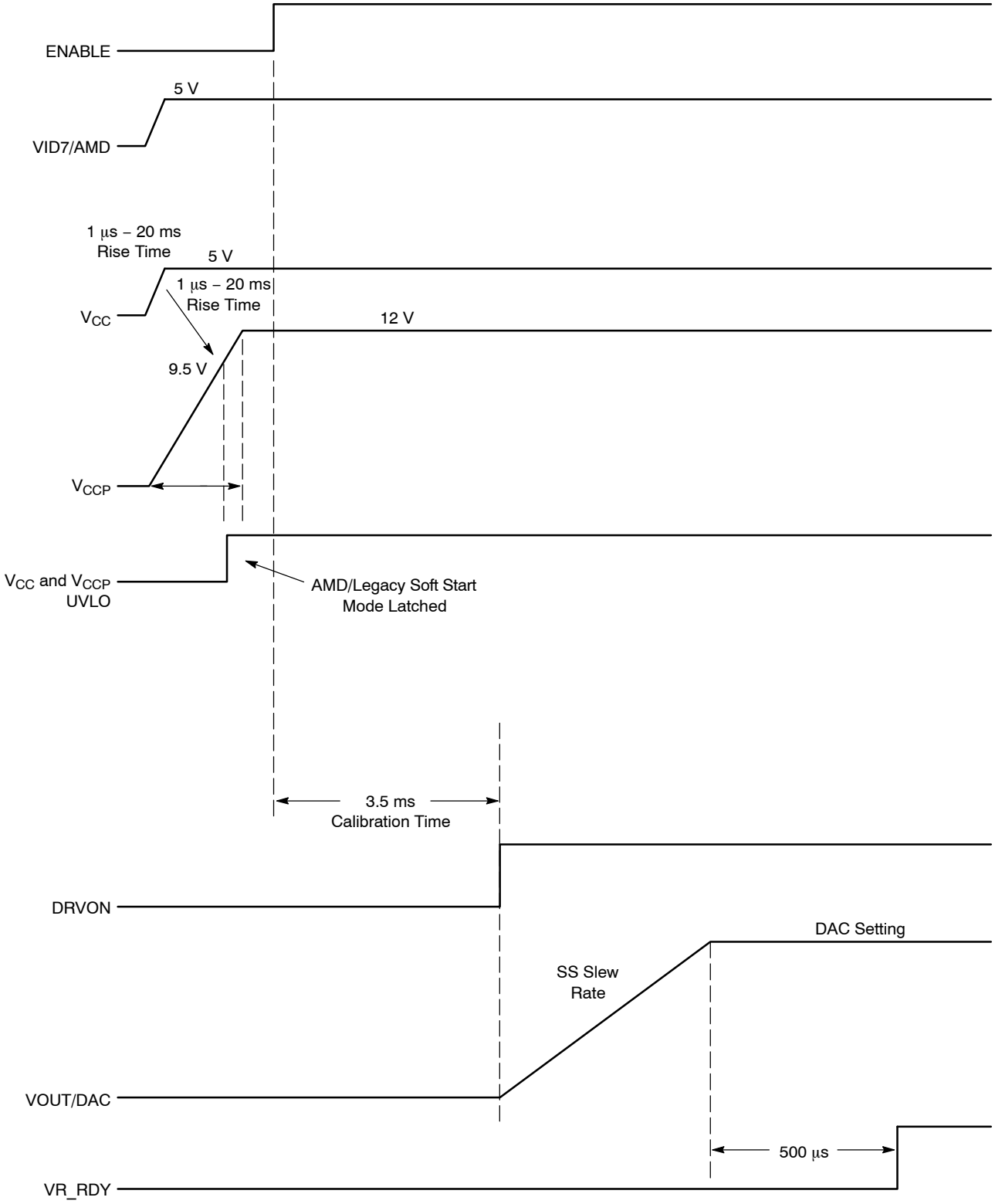
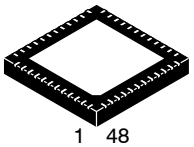



**Figure 7. AMD / Legacy Start Up Timing Diagram**

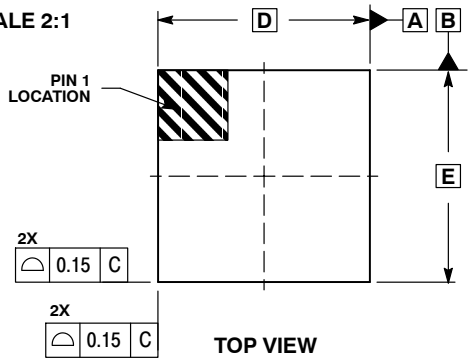
The products described herein (NCP5395), may be covered by one or more of the following U.S. patents; US07057381.There may be other patents pending.

**QFN48 7x7, 0.5P**
CASE 485AJ−01
ISSUE O

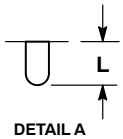
DATE 27 APR 2007



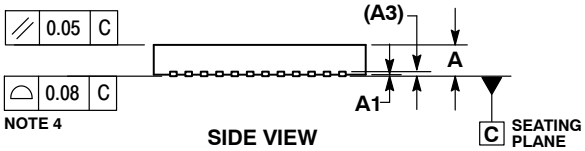

SCALE 2:1



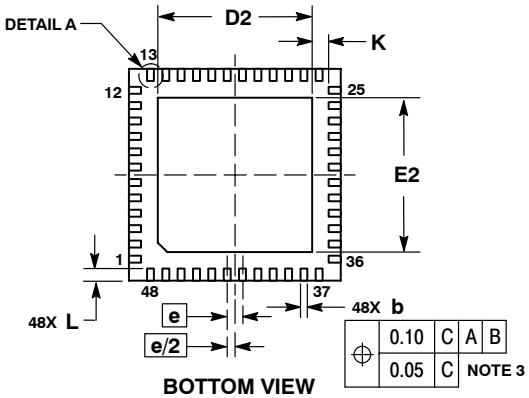

TOP VIEW




DETAIL A
OPTIONAL CONSTRUCTION
2X SCALE




SIDE VIEW

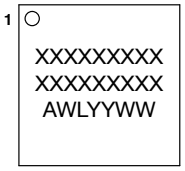



BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 7.00 BSC | |
| D2 | 5.00 | 5.20 |
| E | 7.00 BSC | |
| E2 | 5.00 | 5.20 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |

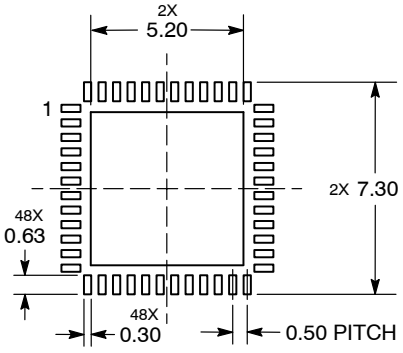
**GENERIC MARKING DIAGRAM***




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON24490D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **QFN48 7X7, 0.50P** | | **PAGE 1 OF 1** |

**onsemi** and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2007

**onsemi**, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales