NCP5230

Low Voltage Synchronous Buck Controller with Power Saving Mode

The NCP5230 is a simple single phase solution with differential phase current sensing, power saving operation, and gate drivers to provide accurately regulated power.

The adaptive non overlap gate drive and power saving operation circuit provide a low switching loss and high efficiency solution for server, notebook, and desktop systems. A high performance operational error amplifier is provided to simplify compensation of the system. The NCP5230 features also include soft−start sequence, accurate overvoltage and over current protection, UVLO for VCC and VCCP, and thermal shutdown.

Features

- High Performance Operational Error Amplifier
- Internal Soft−Start/Stop
- ±0.5% Internal Voltage Accuracy, 0.8 V voltage reference
- OCP accuracy, Four Re−entry Times Before Latch
- “Lossless” Differential Inductor Current Sensing
- Internal High Precision Current Sensing Amplifier
- Oscillator Frequency Range of 100 kHz − 1000 kHz
- 20 ns Adaptive FET Non−overlap Time of Internal Gate Driver
- 5.0 V to 12 V Operation
- Support 1.5 V to 19 V V_{in}
- V_{out} from 0.8 V to 3.3 V (5 V with 12 V_{CC})
- Chip Enable through OSC pin
- Latched Over Voltage Protection (OVP)
- Internally Fixed OCP Threshold
- Guaranteed Startup Into Pre−Charged Loads
- Thermally Compensated Current Monitoring
- Thermal Shutdown Protection
- Integrated MOSFET Drivers
- Integrated BOOST Diode with internal R_{bst} = 2.2 Ω
- Automatic Power Saving Mode to Maximize Efficiency During Light Load Operation
- Sync Function
- Remote Ground Sensing
- This is a Pb−Free Device*

Applications

- Desktop and Server Systems

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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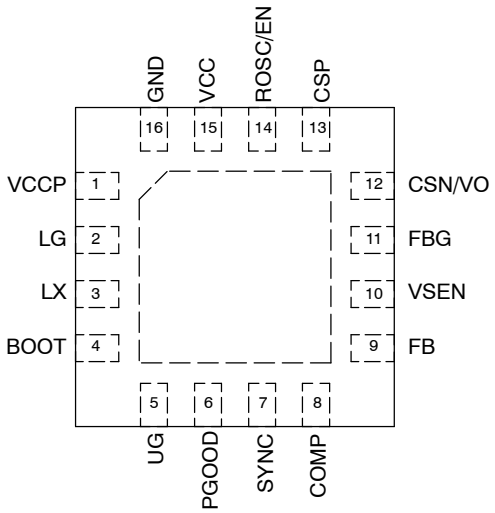
MARKING DIAGRAMS

QFN16
CASE 485G

5230	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP5230MNTWG	QFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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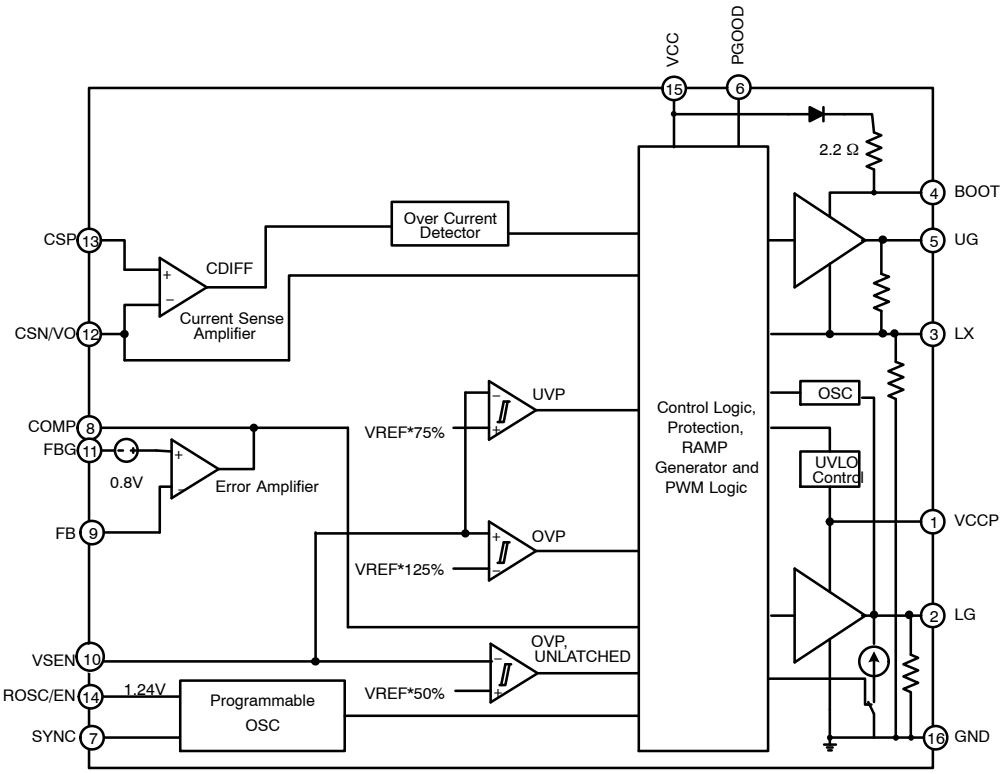

Figure 1. NCP5230 BLOCK DIAGRAM

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	VCCP	Power supply for bottom gate MOSFET drivers
2	LG	Bottom gate MOSFET driver pin
3	LX	Switch node
4	BOOT	Supply rail for the floating top gate driver
5	UG	Top gate MOSFET driver pin
6	PGOOD	Power Good. It is an open−drain output, set free after SS (with 3x clock delay) as long as the output voltage monitored through VSEN is within specifications.
7	SYNC	Synchronization Pin. The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used.
8	COMP	Output of the error amplifier
9	FB	Inverting input to the error amplifier
10	VSEN	Output Voltage Sense
11	FBG	Remote Ground Sense
12	CSN/VO	Inductor differential sense inverting input
13	CSP	Inductor differential sense non−inverting input
14	ROSC/EN	Programs the switching frequency; EN: Pull−low to disable the device
15	VCC	Supply rail for the controller internal circuitry
16	GND	Ground reference
	THERMAL PAD	Connects with the silicon substrate for good thermal contact with the PCB. Connect to GND plane.

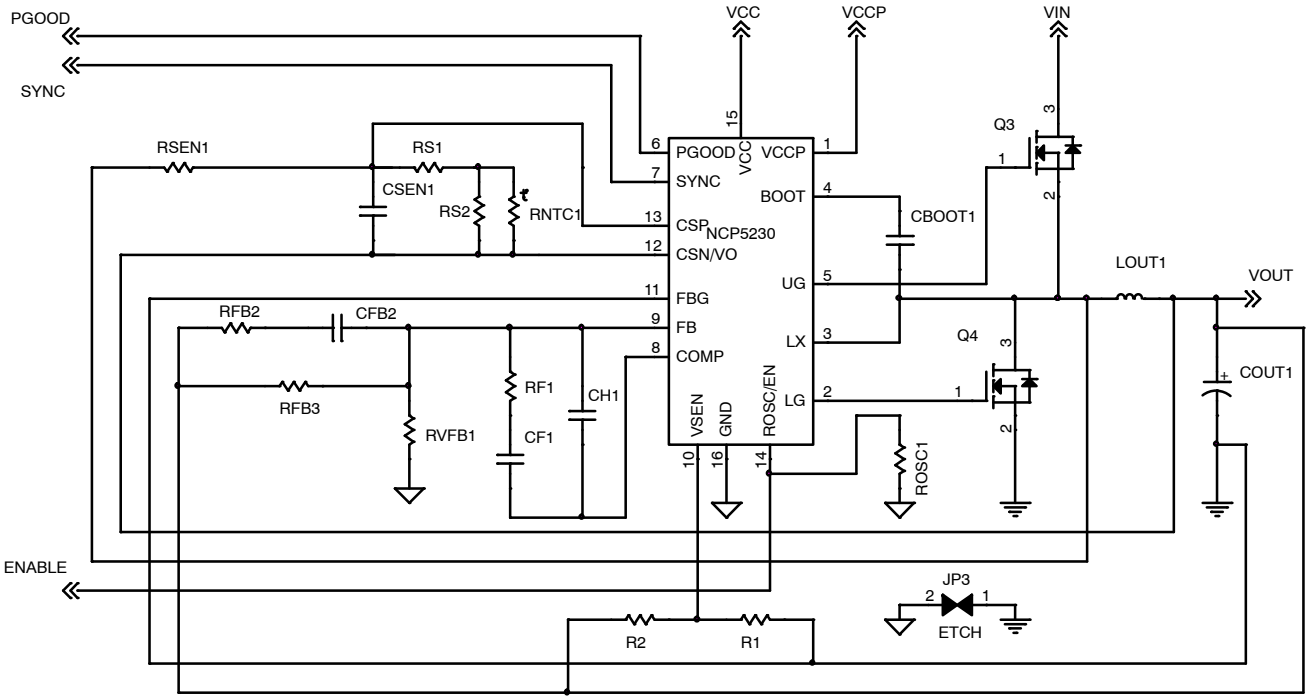

Figure 2. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	V_{MAX}	V_{MIN}	Unit
Controller Power Supply Voltages to GND	VCC, VCCP	15	−0.3	V
Boost Supply Voltage Input	BOOT	35V wrt/GND 40 V <100 ns wrt/GND 15 wrt/LX	−0.3	V
High−Side Driver Output (Top Gate)	UG	35 40 V ≤ 50 ns wrt/GND 15 wrt/LX	−0.3 wrt/LX −5 V < 200 ns	V
Switching Node (Bootstrap Supply Return)	LX	35 40 < 100 ns	−5 −10 V < 200 ns	V
Low−Side Driver Output (Bottom Gate)	LG	15	−0.3 −5 V < 200 ns	V
All Other Pins		6	−0.3, −1 V < 1 μs	V
PGOOD	PGOOD	7	−0.3, −1 V < 1 μs	V
SYNC	SYNC	7	−0.3, −1 V < 1 μs	V
Current Sense Amplifier	CSP, CSN/VO with V_{CC} = 12 V	10	−0.3, −1 V < 1 μs	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Rating	Symbol	Typ	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	60	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	18	°C/W
Operating Junction Temperature Range	T_J	0 to 125	°C
Operating Ambient Temperature Range	T_A	0 to 85	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	−

ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY OPERATING CONDITIONS					
VCC Voltage Range		4.5		13.2	V
VCCP Voltage Range		4.5		13.2	V
dV/dt on VCC (Note 1)		−10		10	V/μs
dV/dt on VCCP (Note 1)		−10		10	V/μs
VCC AND BOOT INPUT SUPPLY CURRENT					
VCC Operating Current	V_{CC} = 5 V, EN = High V_{CC} = 12 V, EN = High			5.0	mA
VCC Supply Current	V_{CC} = 5 V, EN = Low V_{CC} = 12 V, EN = Low			400	uA
VCCP INPUT SUPPLY CURRENT					
VCCP Operating Current UG and LG Open	V_{CCP} = 5 V, EN = High V_{CCP} = 12 V, EN = High		3.5	5.0	mA
VCCP Supply Current	V_{CCP} = 5 V, EN = Low V_{CCP} = 12 V, EN = Low			200	μA
VCC SUPPLY VOLTAGE					
VCC UVLO Start Threshold	V_{CC} Rising			4.50	V
VCC UVLO Hysteresis	V_{CC} Rising or Falling		300		mV
VCCP SUPPLY VOLTAGE					
VCCP UVLO Start Threshold				4.2	V
VCCP UVLO Hysteresis			200		mV
ERROR AMPLIFIER COMP					
Open Loop DC Gain (Note 1)			120		dB
Open Loop Unity Gain Bandwidth (Note 1)		15	18		MHz
Slew Rate (Note 1)	COMP pin to GND with 100 pF load		8.0		V/μs
VREF					
Internal Reference Voltage			0.800		V
Output Voltage Accuracy	V_{out} to FBG excluding external resistor divider tolerance	−0.5		0.5	%
CURRENT SENSE AMPLIFIERS					
Common Mode Input Voltage Range (Note 1, GNG, output within 10mV)	$V_{CC} \leq$ 7.5 V	−0.3		3.5	V
Common Mode Input Voltage Range (Note 1, GNG, output within 10 mV)	V_{CC} > 7.5 V	−0.3		5.5	V

1. Guaranteed by design.
2. For propagation delays, ”tpdh” refers to the specified signal going high ”tpdl” refers to it going low. Reference Gate Timing Diagram.

ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR (with no ROSC Resistor Defaults to 200 kHz)					
Switching Frequency Accuracy	R_{OSC} open	−10		10	%
OSC Gain (Note 1)			10		kHz / μA
Disable threshold	R_{OSC}/EN pin, V_{dis_th}			0.75	V
MODULATORS (PWM Comparators)					
Minimum Pulse Width	F_{sw} = 200 kHz, OSC open		90		ns
Minimum Turn Off Time (LG on)	F_{sw} = 200 kHz, OSC open	250	350	450	ns
Magnitude of the PWM Ramp	V_{IN} = 5 V or 12 V		1.50		V
Maximum Duty Cycle	OSC/EN = OPEN	80		95	%
Minimum Skip mode frequency	In light load, maximum time for LG to turn on after HG turns off	30			kHz
SOFT−START					
Soft Start Time @ 200 kHz	1024 clock cycles, OSC/EN open		5.12		ms
SOFT−OFF					
Soft OFF bleeding resistor	R_{dis}		120		Ω
OVER CURRENT PROTECTION					
First Over Current Threshold	CSP−CSN, 4xMasking	17	20	23	mV
Second Over Current Threshold	CSP−CSN, Immediate action		30		mV
SYNC PIN					
Synchronization Input	VIL, square wave			1.0	V
Synchronization Input	VIH, square wave	2.5			V
PROTECTION AND PGOOD					
Output Voltage	Logic Low, Sinking 4 mA			0.4	V
OVP Threshold	VSEN rising above 1.25 * V_{ref}	117	125	130	%
UVP Threshold	VSEN falling below 0.75 * V_{ref}	70	75	80	%
Unlatched Overvoltage Threshold	V_{th_disoff} with respect to 0.5 V_{ref}	40	50	60	%
Power Good High Delay (Note 1)				50	μs
Power Good Low Delay (Note 1)				1	μs
ZERO CURRENT DETECTION (LX Pin)					
Blanking Time before Zero Current Detection (Note 1)	Blanking Time after LG is < 1.0 V			40	ns
Capture Time for LX Voltage (Note 1)	Time to capture LX voltage once LG is < 1.0 V (must be within dead time limits)			20	ns
Negative LX detection voltage	V_{bdls}	150	300	450	mV
Positive LX detection voltage	V_{bdhs}	0.2	0.5	1.0	V
Time for V_{th} adjustment and settling time (Note 1)	300 kHz	3.0		3.7	μs
Initial Negative Current Detection Threshold Voltage Set Point (Note 1)	LX−GND, Includes ± 2 mV Offset Range		1.0		mV
V_{th} adjustable Range (Note 1)		−16	0	15	mV

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ELECTRICAL CHARACTERISTICS Unless otherwise stated: 0°C < T_A < 85°C; 4.5 V < VCC < 13.2 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
HIGH SIDE DRIVER UG					
R_{H_TG} Output Resistance, Sourcing	V_{BOOT} − V_{LX} = 12 V, C_{load} = 3 nF		2.5	5	Ω
R_{H_TG} Output Resistance, Sinking	V_{BOOT} − V_{LX} = 12V		2.0	2.5	Ω
Tr_{DRVH} Transition Time	C_{LOAD} = 2 nF		16		ns
Tf_{DRVH} Transition Time	C_{LOAD} = 2 nF		11		
$Tpdh_{DRVH}$ Propagation Delay (Notes 1, 2)	Driving High, C_{LOAD} = 3 nF, V_{CC} = 12 V, V_{CCP} =12 V		15	30	ns
UG Internal Resistor to LX	Unbiased, BOOT − LX = 0		45		kΩ
LOW SIDE DRIVER LG					
R_{H_BG} Output Resistance, Sourcing	V_{LX} = GND, C_{load} = 3 nF		2.0	3.0	Ω
R_{L_BG} Output Resistance, Sinking	V_{LX} = V_{CC}		1.0	1.5	Ω
Tr_{DRVL} Transition Time	C_{LOAD} = 3 nF		16		ns
Tf_{DRVL} Transition Time	C_{LOAD} = 3 nF		11		
$Tpdh_{DRVL}$ Propagation Delay (Notes 1, 2)	Driving High, C_{LOAD} = 3 nF, V_{CCP} = 12 V, V_{CCP} = 12 V	10	20	35	ns
LX Internal Resistor to GND			45		kΩ
THERMAL SHUTDOWN					
T_{sd} Thermal Shutdown (Note 1)		150	180		°C
T_{sdhys} Thermal Shutdown Hysteresis (Note 1)			50		°C

1. Guaranteed by design.
2. For propagation delays, ”tpdh” refers to the specified signal going high ”tpdl” refers to it going low. Reference Gate Timing Diagram.

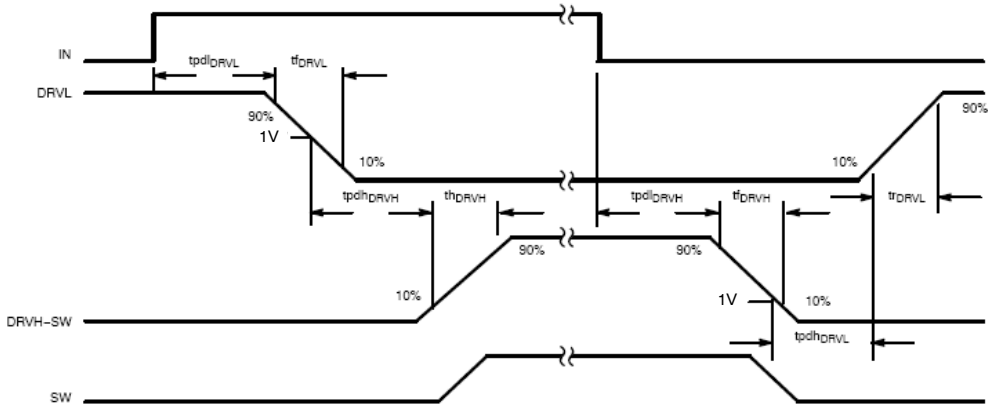


Figure 3. Gate Timing Diagram

Switching Frequency

Connecting a resistor from ROSC/EN to an external voltage source V_{pu} will configure the switching frequency. Normal range would be 100 kHz to 1 MHz. With no resistor connected to the pin, the oscillator frequency is 200 kHz. The switching frequency will follow the relationship:

$$F_{SW} = 200\ \text{kHz} - \frac{V_{pu} - 1.240}{R_{OSC}} \cdot 10\frac{\text{kHz}}{\mu\text{A}} \qquad \text{(eq. 1)}$$

When R_{osc} = infinity (no resistor connected), F_{sw} = 200 kHz; when V_{pu} = ground, the frequency programmed will be higher than 200 kHz. Pulling R_{osc}/EN pin to ground solidly with a less than 10 kΩ resistor will result in the part being disabled.

Soft−Start

Soft−Start will begin if VCC, VCCP are both above their UVLO thresholds and EN pin is set free. IC initially waits a fixed delay time and then ramps the reference in 5.12 ms (1024 clock cycles when R_{osc} open) in closed−loop regulation. After soft−start, PGOOD signal will be released with 3 clock cycles delay.

Protection active during soft−start:

- Overvoltage Protection always enabled;
- Undervoltage Protection is enabled after reference voltage ramps up to 80% of the final value. During soft−start, a UVP fault will initiate a complete soft restart.

Synchronization Function

Synchronize through the SYNC pin. Synchronization function allows different converters to share the same input filter reducing the resulting RMS current and reducing the need for total caps to sustain the load. Synchronized systems also exhibit higher EMI noise immunity and better regulation.

The device synchronizes to the Falling edge of the SYNC pin external input signal (eg. high side gate signal, switch node signal, distribution clock signal), and locks the phase of an internal ramp signal correspondingly with a fixed delay time. The external signal has to sit within a 0-40% frequency window above the local frequency configured by the R_{osc} resistor to allow the synchronization function working properly.

Power Good

The PGOOD pin is an open drain connection with no internal pullup resistor. An active high output signals the normal operation of the converter. PGOOD is pulled low during soft-start cycle, and if there is an overvoltage or undervoltage fault. If the voltage on the VSEN pin is within ±10% of Vref (0.8 V) then the PGOOD pin will not be pulled low.

Overvoltage Protection (OV)

If the voltage on the VSEN pin exceeds the overvoltage threshold (1000 mV or 125% Vref), the NCP5230 will latch an overvoltage fault. During an overvoltage fault event the UG pin will be pulled low, and the LG pin will stay high until the voltage on the VSEN pin goes below 400 mV or 50% V_{ref}, then a soft-bleeding resistor will be connected from switch node to ground to continuously discharge the output voltage softly. To clear the overvoltage fault, toggling VCC or EN is needed.

Undervoltage Protection (UV)

If the voltage on the FB pin falls below the undervoltage threshold after the softstart cycle completes, the NCP5230 will latch an undervoltage fault. During an undervoltage fault, both the UG and LG pins will be pulled low. Toggling VCC power or EN will reset the undervoltage protection.

PreOVP Protection

If the NCP5230 is powered on but not enabled, the VSEN pin will be monitored for preOVP condition. If the VSEN exceeds the preset threshold, the device will force LG pin high to protect the load. The PreOVP function will be disabled when the device is enabled and the normal OV function will operate instead.

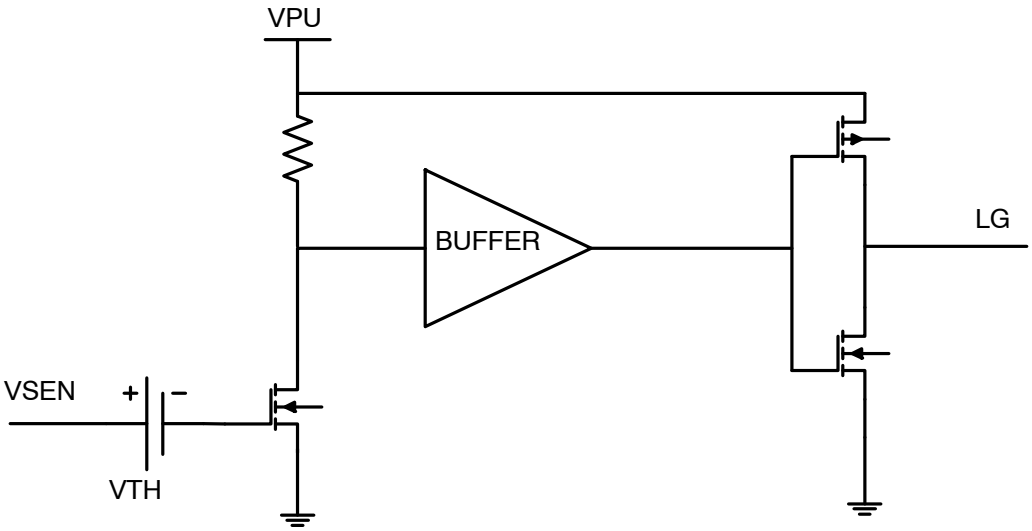


Figure 4. PreOVP circuit

Vin Detection

During the soft start after the VSEN pin exceeds 80% V_{ref}, UV protection will be enabled; If a UV fault is triggered in the softstart, it will restart SS after a fixed delay. The UV protection is to avoid IC to startup without Vin or with insufficient Vin voltage.

Overcurrent Protection

NCP5230 measures the differential current sensing signal through CSP and CSN/VO pin. There are two current protection levels: OCP1 and OCP2. If the differential voltage across pin CSP and CSN/VO is over 20 mV (but below 30 mV) for four consecutive cycles, OCP1 will be tripped. Both UG and LG will be forced to low to turn off the high side and low side FETs, it is a latched condition; If the differential voltage across pin CSP and CSN is over 30 mV, OCP2 will be tripped, the UG and LG will be pulled low and latched immediately. Toggling VCC power or EN will reset the Overcurrent protection.

The current sensing R/C network should be selected to match the inductor time constant as below,

$$(RCS1//RCS2) \cdot C = \frac{L}{DCR}$$

(Notes: the actual RC network time constant may be slightly higher)

Thus, OCP1 and OCP2 levels can be configured as,

$$OCP1 = \frac{20\ mV}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$

$$OCP2 = \frac{30\ mV}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$

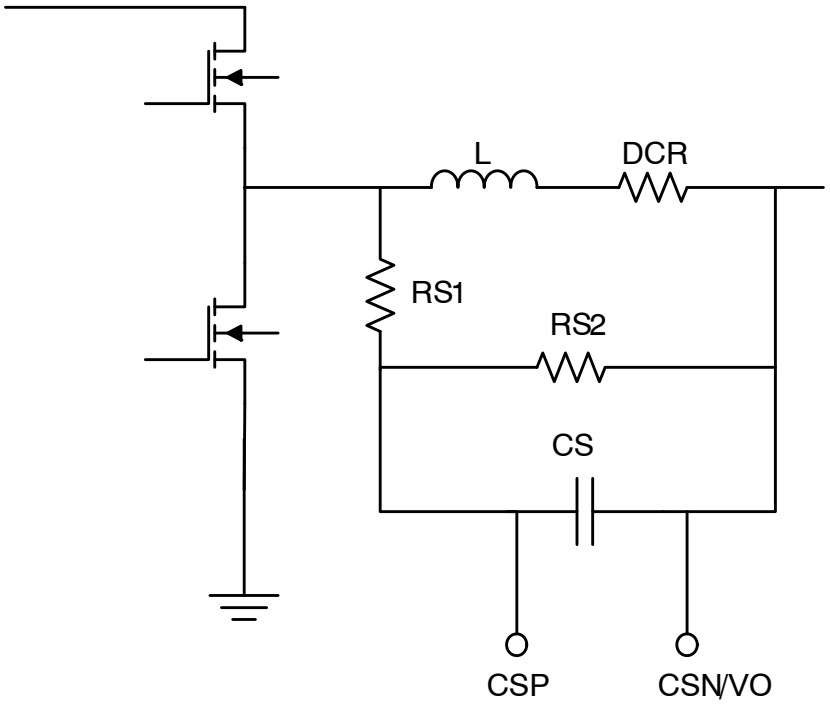


Figure 5. Differential Current Sense Network

Light Load Operation

In the light load condition, NCP5230 will work in a diode emulation mode with bottom gate turning off if the inductor current is below zero. The system therefore works in discontinuous conduction mode (DCM). The zero current detection is done by sensing switch node and automatically adjusted to minimize the low side FET body diode conduction time (right after LG turns off) in diode emulation mode.

If the load reduces further, COMP signal will be close or below the internal ramp bottom triggering minimum on time operation, the system will start skipping pulses, working in a reduced frequency range. NCP5230 has an internal ultrasonic timer to keep the device from working in an audio frequency and below. This timer initiates after high side gate off signal and expires after ~30 μs.

Normally high side gate signal will reset this ultrasonic timer repeatedly before it expires. In a very light load or load release, if there is no high side gate pulses until the timer expires, the low side MOSFET(s) will be forced to turn on to discharge the output. Through properly compensated network the comp signal will climb up to generate next burst of switching pulses and the converter will regulate the output voltage to its target level. This can last a few cycles or continuously depending on the system load level.

In light load operation, if synchronization is enabled, NCP5230 will also check the SYNC pin input signal cycle by cycle. If the external sync signal is within the synchronization frequency range, the NCP5230 will interleave its switching pulses with it after a proper delay. In this way, the ripple variation during transition between the discontinuous and continuous current mode can be minimized.

Voltage Feedback

The NCP5230 allow the output voltage to be adjusted from 0.8 V to 5 V via an external resistor divider network (R1, R2). The controller will regulate the output voltage to maintain the FB pin voltage to 0.8 V reference voltage. The relation between the resistor divider network and the output voltage is as below;

$$R2 = R1 \cdot \left(\frac{0.8\ V}{V_{out} - 0.8\ V} \right)$$

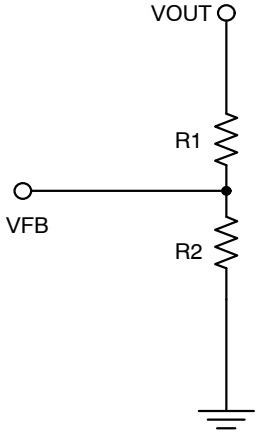


Figure 6. Feedback Voltage

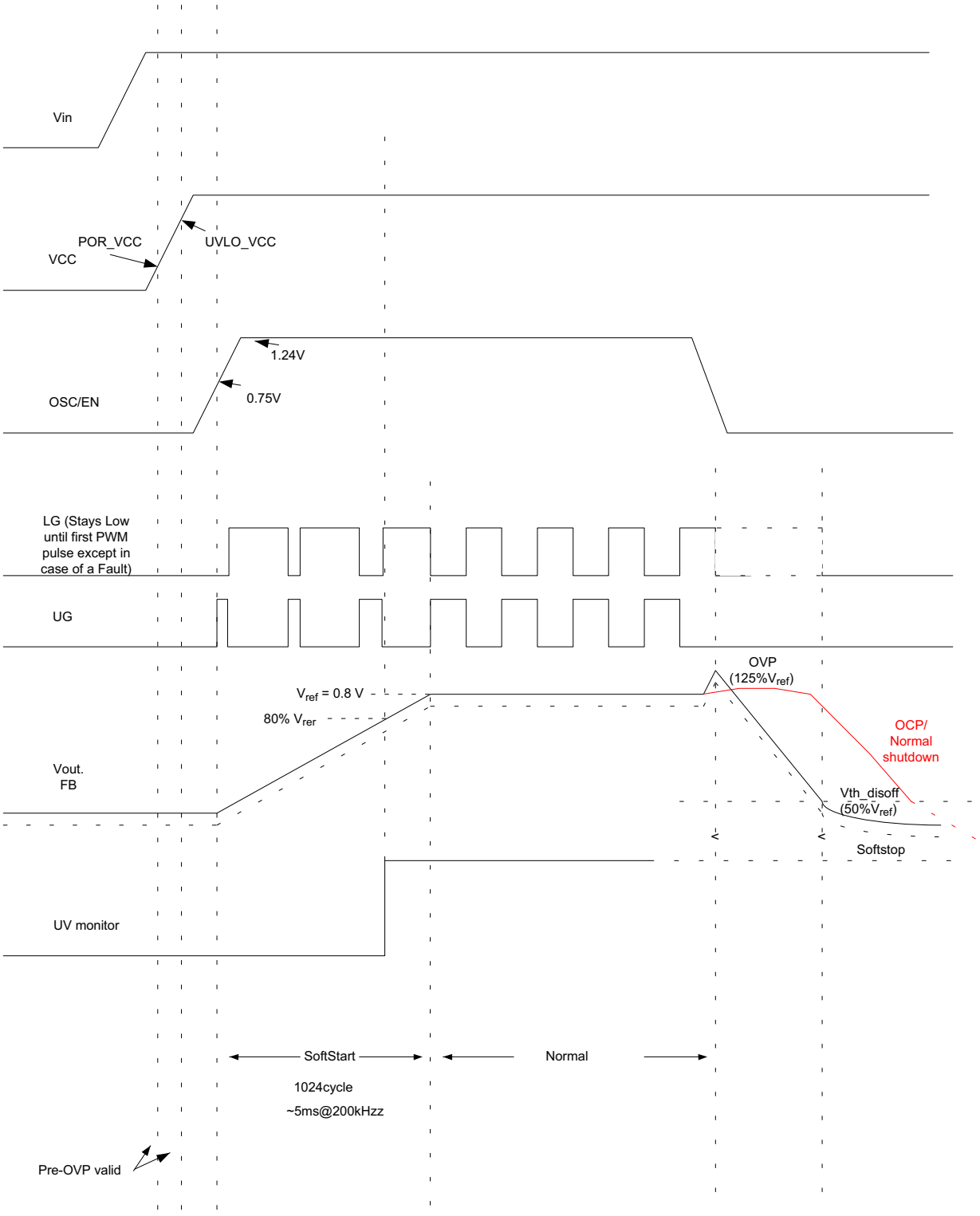


Figure 7. Start Up and Shutdown Timing Diagram

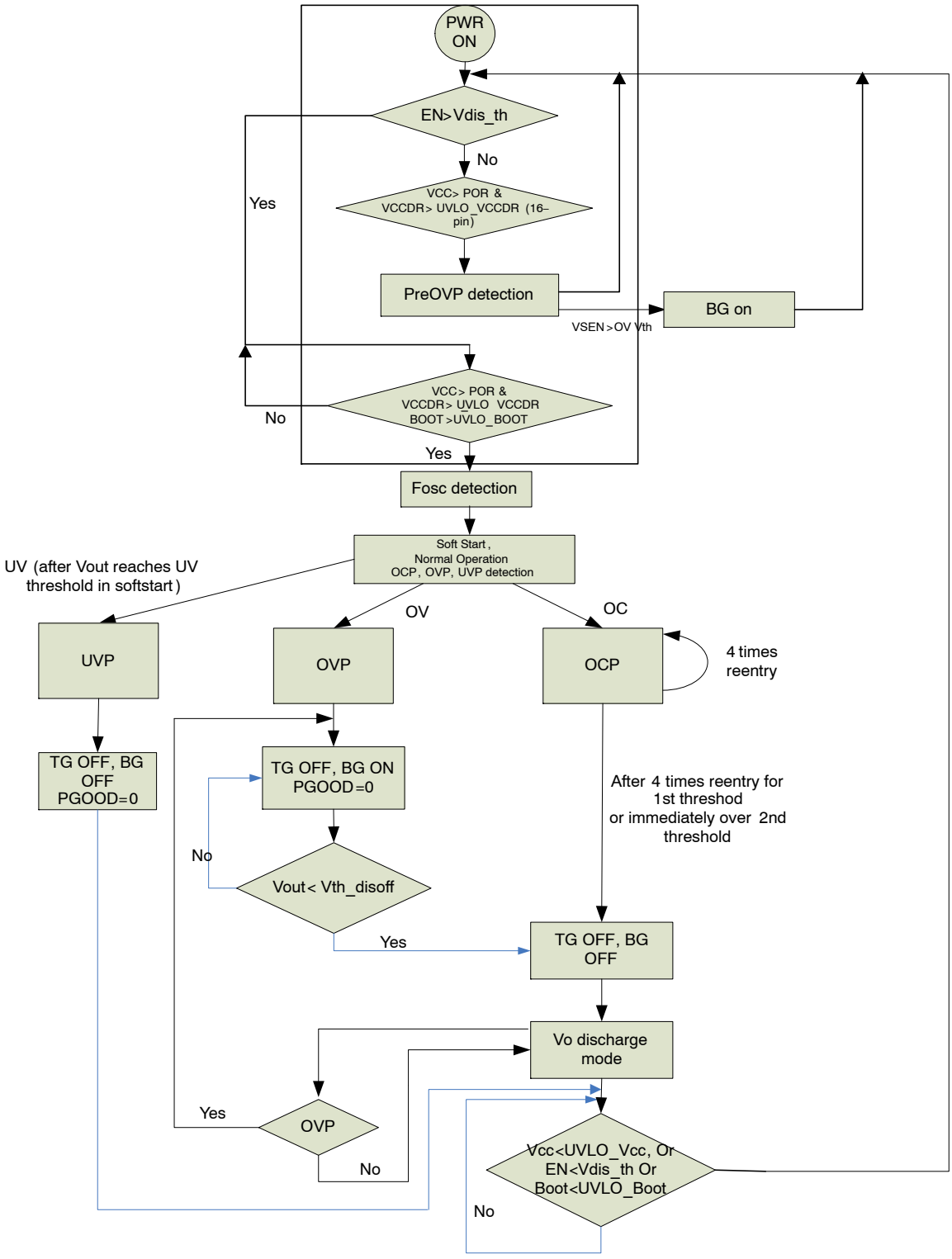
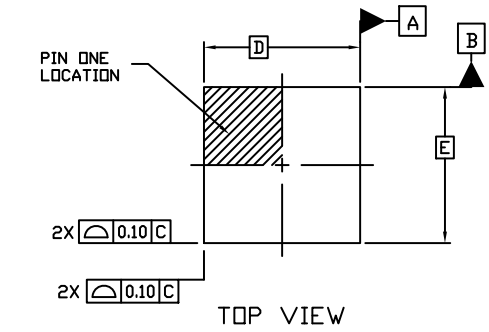


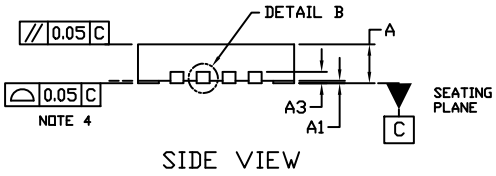
Figure 8. State Diagram

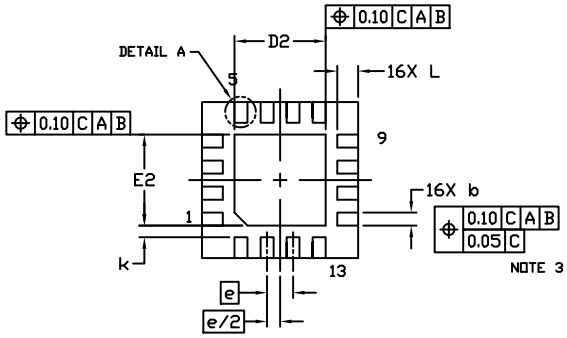
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

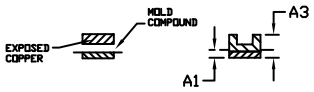
SCALE 2:1



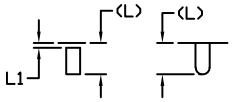




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



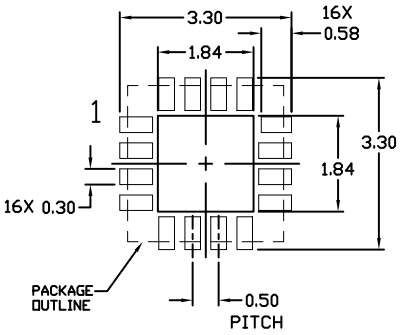
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
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(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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